Art of Engineering: CE / CS Dept. Project Policies

Introduction

In this part of the syllabus, I have outlined important course policies and expectations. Please read before our first synchronous meeting, at which time we will discuss any questions or suggestions for improvement.

Instructor

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Please call me Caleb - I am an Electrical Engineering PhD student and my research focuses on neural interface design. I created this department project in Fall 2019 and have been developing it ever since.

General Expectations

Over the years I have put a lot of work into developing this project, choosing the structure and content intentionally to create a fun, interesting, and challenging learning experience. During the project, I am committed to helping every student get the most out of it (see more information about instructor support below). If at any point you identify an area in which I can do better, please don't hesitate to let me know (there will also be a mid-project survey for anonymous feedback).

Since you may select the department project of your choice, I expect that if you choose this one, you are ready to participate fully and enthusiastically. This means that you are willing to carefully read and follow assignment directions, actively engage in in-person classwork, and seek out instructor support when necessary. Most students do not have prior experience with the topics & techniques that make up this project, so you should be prepared to persevere through the process of debugging your designs and building your understanding through independent and instructor-supported work.

As in all parts of the Art of Engineering, your grade is primarily based on participation; if you satisfy the project requirements, you will get an A. However, it is important to understand what qualifies as successful participation in this project. Therefore, **if you are interested in choosing this project to fulfill the department project requirement, please read all policies first.** If you neglect to do so, you may find that you are unable to satisfy the participation requirements, and you will be asked to join a different project.

In general, the timeline of this project is longer than that of many other department project options, and you are expected to put in steady work throughout the middle of the semester in order to complete the project. Each individual module, lesson, or assignment is designed to be manageable, but if you are not paying attention early, you may fall behind. If you do find yourself in this situation, do not panic – I hold office hours every week, and I will be happy to help you make a plan to catch up.

Sign-Up and Synchronous Session Attendance

To participate in the project, you must **sign up by Feb 17**. In addition, you must be available to attend synchronous meetings in-person in **Fayerweather 313 on Fridays between 1:30pm and 3:00pm**. See more information about attendance grading below, and consult the project description for a detailed schedule.

Assessment & Feedback
There are many intermediate deadlines, each of which is for a small section of the final project. The purpose of all these intermediate deliverables is to ensure that you are making steady progress throughout the semester. Each of these will be graded on a 1/0 basis (after all, this is a digital design project).

Specifically, for each of the independent design assignments not including the final report (ALU, register file, and program), the work can be "incomplete," but you must follow all assignment directions. I will then provide you with qualitative feedback, focusing on areas of improvement that will help you create a fully-functional processor for the final assignment. I generally complete grading & feedback roughly one week after an assignment is due, giving you enough time to incorporate my feedback into your next assignment. If you have any questions about comments I make on your assignments, please discuss with me during office hours or on Ed Discussion (see below).

For the final report, I will assess your work based on evidence of clear effort and exploration of the important concepts (see detailed point breakdown below). In general, I will be looking for whether you have made use of abstraction and design hierarchy to simplify your design process, and whether you have run appropriate simulations to characterize your design. I would rather see you submit an "incomplete" project that is carefully designed and analyzed than a complete microprocessor implemented without knowing what is going on!

Detailed Grading Breakdown

Required: ALU Report turned in	+1
Required: Register File Report turned in	+1
Required: Program Report turned in	+1
Required: Final Report turned in	+1
Required: Attendance at 2 synchronous sessions	+1
Attendance at each additional session	+0.5 each
Final report: follows all directions	+1
Final report: processor contains all sub-blocks	+1
Final report: effort made to debug wiring issues	+1
Final report: demonstration of working program	+1
Total	**+10**
Bonus: Extra functionality and/or very cool program	+1

Score	Dept Project Grade
11	A+
7-10	A
5-6.5	C
<5	No Credit

To get any credit for completing the department project (grade of C or higher), you must sign up by the deadline (Feb 17), turn in all 4 required reports, and attend at least 2 synchronous sessions in person.

Instructor Support
Please do not hesitate to ask me questions **on the Ed Discussion (through courseworks)**; you can do so anonymously if you choose to, and your classmates will also benefit from the answers. I will generally respond within 24 hours. Asking questions on the shared discussion board, where everyone can see the question and the answer, means that I don't have to spend time answering the same question several times via email. **If you email me a question about the project, I will respond by asking you to repost your question on Ed Discussion.**

I will have an office hour on Monday from 12pm - 1pm eastern (NYC) time. The zoom link is here. Please stop by! I love talking about circuit design, programming, and electrical/computer engineering in general, and it makes my life more interesting to find new ways of explaining difficult concepts to students, who often have different backgrounds, perspectives, and education goals.

Many first-year students are hesitant to attend office hours, viewing this as a sign of weakness. Instead, I would encourage you to view the instructor support options as opportunities to "work smart": you could spend hours struggling to understand something on your own, or spend 5 minutes clarifying the topic in office hours. Later in your college career, you will likely find that many of the most successful students attend office hours regularly to maximize their learning experience in a course. Even if you don't have specific questions, you will likely learn something new from discussing problems with me and with your peers.

Class Conduct
Please be friendly and respect your fellow classmates during synchronous class time and office hours. This means listening to and making space for others' opinions and ways of thinking that may be different from your own. In addition, while I always welcome questions during class, if I find that one or more students are *answering questions* too often, I may take a break from calling on those students to encourage others to participate. For those who are less comfortable sharing thoughts in front of the class, there are other ways to participate, including group work and writing notes in the collaborative document.

Textbook, Logisim Documentation, and Other Resources
You are NOT required to use a textbook for this project. However, if you are looking for a useful reference, check out *Computer Organization and Design, RISC-V Edition*, by Patterson and Hennessy. Not to be confused with the other computer architecture book, by Hennessy and Patterson. You do NOT need to buy this book; I assure you there are other ways of finding it.

As you use Logisim, which is most likely an unfamiliar tool, you will undoubtedly encounter unexpected issues or questions. Part of being a good engineer is learning how to use documentation to acquire new CAD tool skills; thus, you'll probably want to consult the Logisim documentation at least once during the course of this project.

You are also encouraged to consult other online resources, including Wikipedia, StackExchange, and any other conceptual tutorials. You should not, however, be looking for Logisim solutions for the independent design assignments.

Although synchronous classwork is done in small groups, and you are encouraged to discuss your asynchronous work with your peers, all independent design assignment work that you turn in must be individual.