1. Description

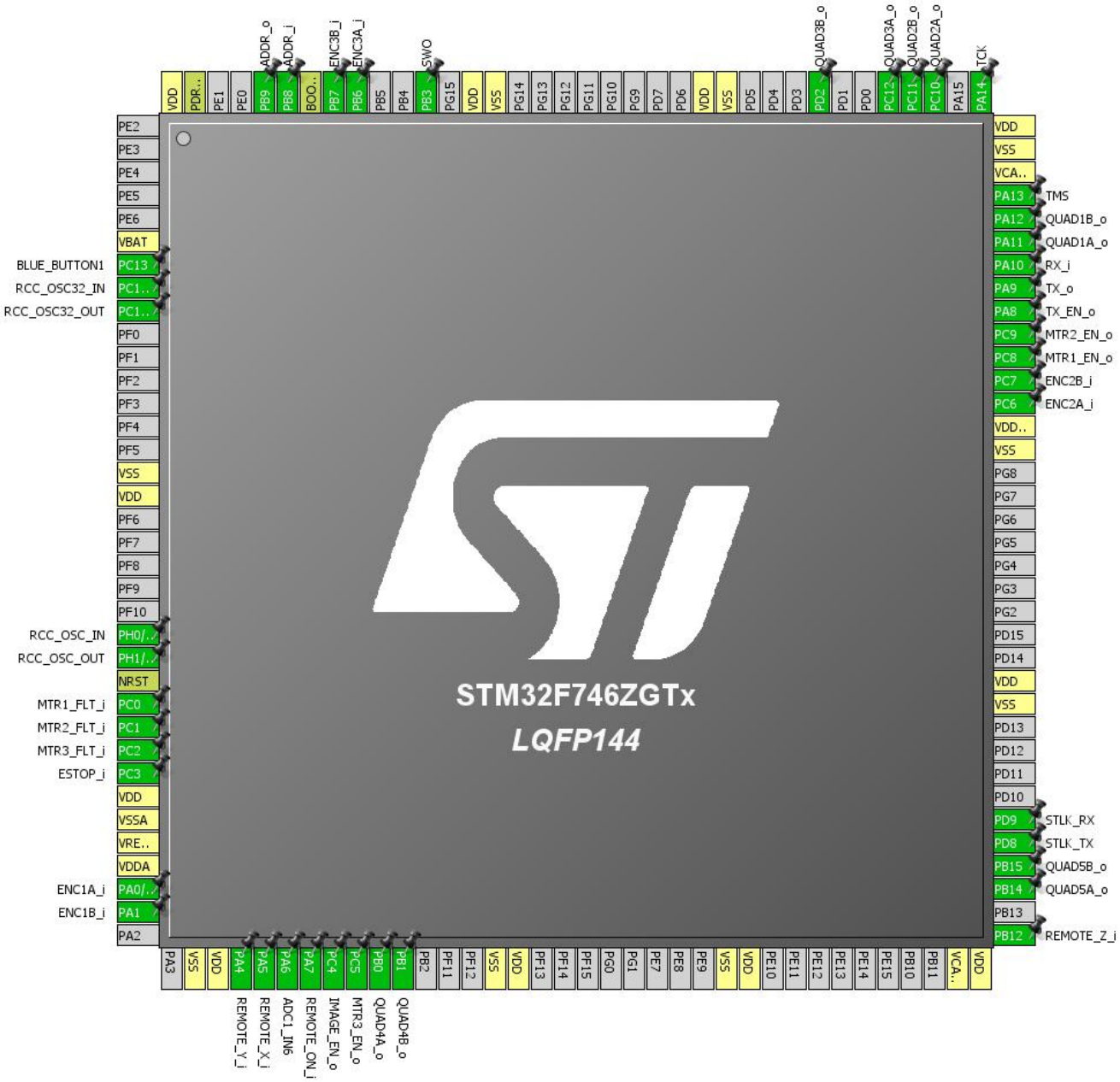
1.1. Project

Project Name	MCU16
Board Name	NUCLEO-F746ZG
Generated with:	STM32CubeMX 4.13.1
Date	05/20/2016

1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x6
MCU name	STM32F746ZGTx
MCU Package	LQFP144
MCU Pin number	144

2. Pinout Configuration



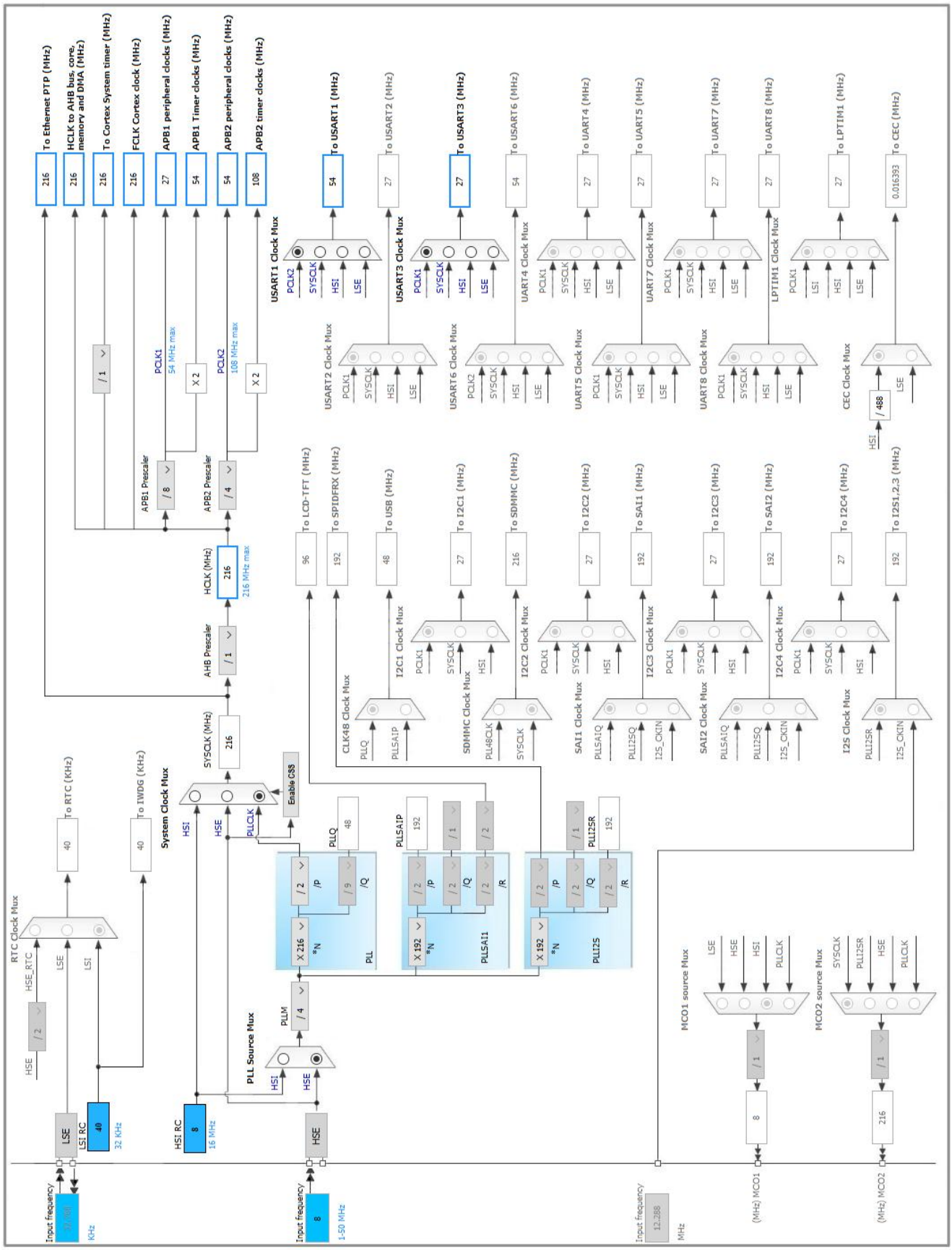
3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
7	PC13 *	I/O	GPIO_Input	BLUE_BUTTON1
8	PC14/OSC32_IN	I/O	RCC_OSC32_IN	
9	PC15/OSC32_OUT	I/O	RCC_OSC32_OUT	
16	VSS	Power		
17	VDD	Power		
23	PH0/OSC_IN	I/O	RCC_OSC_IN	RCC_OSC_IN
24	PH1/OSC_OUT	I/O	RCC_OSC_OUT	RCC_OSC_OUT
25	NRST	Reset		
26	PC0 *	I/O	GPIO_Input	MTR1_FLT_i
27	PC1 *	I/O	GPIO_Input	MTR2_FLT_i
28	PC2 *	I/O	GPIO_Input	MTR3_FLT_i
29	PC3 *	I/O	GPIO_Input	ESTOP_i
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
34	PA0/WKUP	I/O	TIM2_CH1	ENC1A_i
35	PA1	I/O	TIM2_CH2	ENC1B_i
38	VSS	Power		
39	VDD	Power		
40	PA4 *	I/O	GPIO_Input	REMOTE_Y_i
41	PA5 *	I/O	GPIO_Input	REMOTE_X_i
42	PA6	I/O	ADC1_IN6	
43	PA7 *	I/O	GPIO_Input	REMOTE_ON_i
44	PC4 *	I/O	GPIO_Output	IMAGE_EN_o
45	PC5 *	I/O	GPIO_Output	MTR3_EN_o
46	PB0 *	I/O	GPIO_Output	QUAD4A_o
47	PB1 *	I/O	GPIO_Output	QUAD4B_o
51	VSS	Power		
52	VDD	Power		
61	VSS	Power		
62	VDD	Power		
71	VCAP_1	Power		
72	VDD	Power		
73	PB12 *	I/O	GPIO_Input	REMOTE_Z_i

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
75	PB14 *	I/O	GPIO_Output	QUAD5A_o
76	PB15 *	I/O	GPIO_Output	QUAD5B_o
77	PD8	I/O	USART3_TX	STLK_TX
78	PD9	I/O	USART3_RX	STLK_RX
83	VSS	Power		
84	VDD	Power		
94	VSS	Power		
95	VDDUSB	Power		
96	PC6	I/O	TIM3_CH1	ENC2A_i
97	PC7	I/O	TIM3_CH2	ENC2B_i
98	PC8 *	I/O	GPIO_Output	MTR1_EN_o
99	PC9 *	I/O	GPIO_Output	MTR2_EN_o
100	PA8 *	I/O	GPIO_Output	TX_EN_o
101	PA9	I/O	USART1_TX	TX_o
102	PA10	I/O	USART1_RX	RX_i
103	PA11 *	I/O	GPIO_Output	QUAD1A_o
104	PA12 *	I/O	GPIO_Output	QUAD1B_o
105	PA13	I/O	SYS_JTMS-SWDIO	TMS
106	VCAP_2	Power		
107	VSS	Power		
108	VDD	Power		
109	PA14	I/O	SYS_JTCK-SWCLK	TCK
111	PC10 *	I/O	GPIO_Output	QUAD2A_o
112	PC11 *	I/O	GPIO_Output	QUAD2B_o
113	PC12 *	I/O	GPIO_Output	QUAD3A_o
116	PD2 *	I/O	GPIO_Output	QUAD3B_o
120	VSS	Power		
121	VDD	Power		
130	VSS	Power		
131	VDD	Power		
133	PB3	I/O	SYS_JTDO-SWO	SWO
136	PB6	I/O	TIM4_CH1	ENC3A_i
137	PB7	I/O	TIM4_CH2	ENC3B_i
138	BOOT0	Boot		
139	PB8 *	I/O	GPIO_Input	ADDR_i
140	PB9 *	I/O	GPIO_Output	ADDR_o
143	PDR_ON	Reset		
144	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

mode: IN6

5.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 2
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 6
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.2. RCC

High Speed Clock (HSE): BYPASS Clock Source
Low Speed Clock (LSE) : Crystal/Ceramic Resonator

5.2.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	7 WS (8 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled

Power Parameters:

Power Over Drive	Enabled
Power Regulatror Voltage Scale	Power Regulator Voltage Scale 1

5.3. SYS

Debug: SWD and Asynchronous Trace

Timebase Source: SysTick

5.4. TIM2

Combined Channels: Encoder Mode

5.4.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**0x0FFFFFFFF ***
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	**Encoder Mode TI1 and TI2 ***
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	**4 ***
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	**4 ***

5.5. TIM3

Combined Channels: Encoder Mode

5.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**0x0FFFF ***
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	**Encoder Mode TI1 and TI2 ***
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	**4 ***
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	**4 ***

5.6. TIM4

Combined Channels: Encoder Mode

5.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**0x0FFFF ***

Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	**Encoder Mode TI1 and TI2 ***
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	**4 ***
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	**4 ***

5.7. TIM5

mode: Clock Source

5.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**54 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**0x0FFFFFFF ***
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

5.8. TIM9

mode: Clock Source

5.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**108 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**0x0FFFF ***
Internal Clock Division (CKD)	No Division

5.9. TIM10

mode: Activated

5.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**108 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**0x0FFFF ***
Internal Clock Division (CKD)	No Division

5.10. TIM11

mode: Activated

5.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**108 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**0x0FFFF ***
Internal Clock Division (CKD)	No Division

5.11. TIM12

mode: Clock Source

5.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**54 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**0x0FFFF ***
Internal Clock Division (CKD)	No Division

5.12. TIM13

mode: Activated

5.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**54 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**0x0FFFF ***
Internal Clock Division (CKD)	No Division

5.13. TIM14

mode: Activated

5.13.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**54 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**0x0FFFF ***
Internal Clock Division (CKD)	No Division

5.14. USART1

Mode: Asynchronous

5.14.1. Parameter Settings:

Basic Parameters:

Baud Rate	**19200 ***
Word Length	**8 Bits (including Parity) ***
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

5.15. USART3

Mode: Asynchronous

5.15.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	7 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable

RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA6	ADC1_IN6	Analog mode	No pull-up and no pull-down	n/a	
RCC	PC14/OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15/OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	RCC_OSC_IN
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	RCC_OSC_OUT
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	TMS
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	TCK
	PB3	SYS_JTDO-SWO	n/a	n/a	n/a	SWO
TIM2	PA0/WKUP	TIM2_CH1	Alternate Function Push Pull	**Pull-up ***	**Fast ***	ENC1A_i
	PA1	TIM2_CH2	Alternate Function Push Pull	**Pull-up ***	**Fast ***	ENC1B_i
TIM3	PC6	TIM3_CH1	Alternate Function Push Pull	**Pull-up ***	**Fast ***	ENC2A_i
	PC7	TIM3_CH2	Alternate Function Push Pull	**Pull-up ***	**Fast ***	ENC2B_i
TIM4	PB6	TIM4_CH1	Alternate Function Push Pull	**Pull-up ***	**Fast ***	ENC3A_i
	PB7	TIM4_CH2	Alternate Function Push Pull	**Pull-up ***	**Fast ***	ENC3B_i
USART1	PA9	USART1_TX	Alternate Function Push Pull	Pull-up	**High ***	TX_o
	PA10	USART1_RX	Alternate Function Push Pull	Pull-up	**High ***	RX_i
USART3	PD8	USART3_TX	Alternate Function Push Pull	Pull-up	**High ***	STLK_TX
	PD9	USART3_RX	Alternate Function Push Pull	Pull-up	**High ***	STLK_RX
GPIO	PC13	GPIO_Input	Input mode	**Pull-up ***	n/a	BLUE_BUTTON1
	PC0	GPIO_Input	Input mode	**Pull-up ***	n/a	MTR1_FLT_i
	PC1	GPIO_Input	Input mode	**Pull-up ***	n/a	MTR2_FLT_i
	PC2	GPIO_Input	Input mode	**Pull-up ***	n/a	MTR3_FLT_i
	PC3	GPIO_Input	Input mode	**Pull-up ***	n/a	ESTOP_i
	PA4	GPIO_Input	Input mode	**Pull-up ***	n/a	REMOTE_Y_i
	PA5	GPIO_Input	Input mode	**Pull-up ***	n/a	REMOTE_X_i

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PA7	GPIO_Input	Input mode	**Pull-up ***	n/a	REMOTE_ON_i
	PC4	GPIO_Output	Output Push Pull	**Pull-up ***	Low	IMAGE_EN_o
	PC5	GPIO_Output	Output Push Pull	**Pull-up ***	Low	MTR3_EN_o
	PB0	GPIO_Output	Output Push Pull	**Pull-up ***	**Medium ***	QUAD4A_o
	PB1	GPIO_Output	Output Push Pull	**Pull-up ***	**Medium ***	QUAD4B_o
	PB12	GPIO_Input	Input mode	**Pull-up ***	**n/a**	REMOTE_Z_i
	PB14	GPIO_Output	Output Push Pull	**Pull-up ***	**Medium ***	QUAD5A_o
	PB15	GPIO_Output	Output Push Pull	**Pull-up ***	**Medium ***	QUAD5B_o
	PC8	GPIO_Output	Output Push Pull	**Pull-up ***	Low	MTR1_EN_o
	PC9	GPIO_Output	Output Push Pull	**Pull-up ***	Low	MTR2_EN_o
	PA8	GPIO_Output	Output Push Pull	**Pull-down ***	Low	TX_EN_o
	PA11	GPIO_Output	Output Push Pull	**Pull-up ***	**Medium ***	QUAD1A_o
	PA12	GPIO_Output	Output Push Pull	**Pull-up ***	**Medium ***	QUAD1B_o
	PC10	GPIO_Output	Output Push Pull	**Pull-up ***	**Medium ***	QUAD2A_o
	PC11	GPIO_Output	Output Push Pull	**Pull-up ***	**Medium ***	QUAD2B_o
	PC12	GPIO_Output	Output Push Pull	**Pull-up ***	**Medium ***	QUAD3A_o
	PD2	GPIO_Output	Output Push Pull	**Pull-up ***	**Medium ***	QUAD3B_o
	PB8	GPIO_Input	Input mode	**Pull-up ***	**n/a**	ADDR_i
	PB9	GPIO_Output	Output Push Pull	**Pull-up ***	Low	ADDR_o

6.2. DMA configuration

nothing configured in DMA service

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
System tick timer	true	0	0
TIM1 break interrupt and TIM9 global interrupt	true	2	0
TIM1 update interrupt and TIM10 global interrupt	true	1	0
TIM1 trigger and commutation interrupts and TIM11 global interrupt	true	1	0
USART1 global interrupt	true	1	0
TIM8 break interrupt and TIM12 global interrupt	true	1	0
TIM8 update interrupt and TIM13 global interrupt	true	0	0
TIM8 trigger and commutation interrupts and TIM14 global interrupt	true	1	0
Non maskable interrupt	unused		
Hard fault interrupt	unused		
Memory management fault	unused		
Pre-fetch fault, memory access fault	unused		
Undefined instruction or illegal state	unused		
Debug monitor	unused		
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 global interrupts	unused		
TIM2 global interrupt	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		
USART3 global interrupt	unused		
TIM5 global interrupt	unused		

*** User modified value**

7. Power Plugin report

7.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x6
MCU	STM32F746ZGTx
Datasheet	027590_Rev3

7.2. Parameter Selection

Temperature	25
Vdd	3.6

8. Software Project

8.1. Project Settings

Name	Value
Project Name	MCU16
Project Folder	C:\Users\atcop\OneDrive\Documents\0KL MCU16\MCU16_SW\MCU16
Toolchain / IDE	EWARM
Firmware Package Name and Version	STM32Cube FW_F7 V1.3.1

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Add necessary library files as reference in the toolchain project configuration file
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No