Only signals that are being asserted are shown

Arrows with no signal name labeled are unconditional transitions

IDLE
b0000

rst

Start

Latch multiplicand from Z into Reg1
wr_en[0] = 1
b0001

Latch Multiplier from Z into Reg2
wr_en[1] = 1
b0010

Latch 0x0000 from Z into Reg4
wr_en[3] = 1
b0011

Latch 0x0001 from Z into Reg5
wr_en[4] = 1
count16_init = 1
b0100

!Start

Start

put result in R4 out on A
done = 1
rd_enA[3] =1
b1001

count16_out ==

Shift MPLIER
R1 <- LSL R1 by R5
wr_en[0] = 1
rd_enA[4]=1
rd_enB[0]=1
shift_en = 1
left_right = 0
b1000

count16_out != 15

generate PP
R3<- R1 & 32{R2[0]}
wr_en[2] = 1
rd_enA[0]=1
rd_enB[1]=1
ppgen_en=1
count16_inc = 1
b0101

Shift MCAND
R2 <- LSR R2 by R5
wr_en[1] = 1
rd_enA[4]=1
rd_enB[1]=1
shift_en = 1
left_right = 1
b0111

Accumulate
R4<- R3 +R4
wr_en[3] = 1
rd_enA[2]=1
rd_enB[3]=1
add_en = 1
b0110