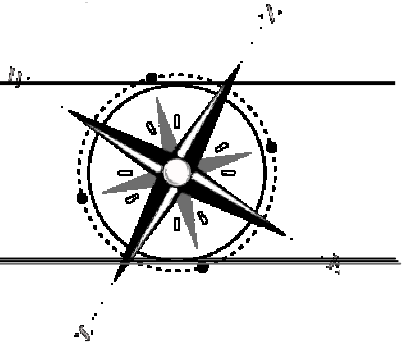
ECE551 Fall 2010 Doc Version 1.00

Design Project Overview



Summary

In this project you will design and synthesize a Router for use in a 2-Dimensional Mesh Network. Using your design, you will create a 2-dimensional routing network composed of an array of your routers, with each router connected to its North, South, East, and West neighbors. Each router will be interfaced to a simulated processor node, which will inject packets into your network. Your router must be capable of transmitting these messages across the network to their recipient nodes.

Purpose

The design project will allow you to learn more about the design and synthesis process and develop skills for use in your future career. The project will give you experience in:

- Working on the design of a complex system in a team environment
- The Planning, Design Entry, Synthesis, and Verification stages of digital design
- Designing a system component to be compatible with a specified interface
- Evaluating trade-offs and justifying design decisions
- Using an industry-standard synthesis tool to meet area and performance objectives
- Creating a test suite and validating synthesized logic
- Documenting and communicating your work to your boss (i.e. me)

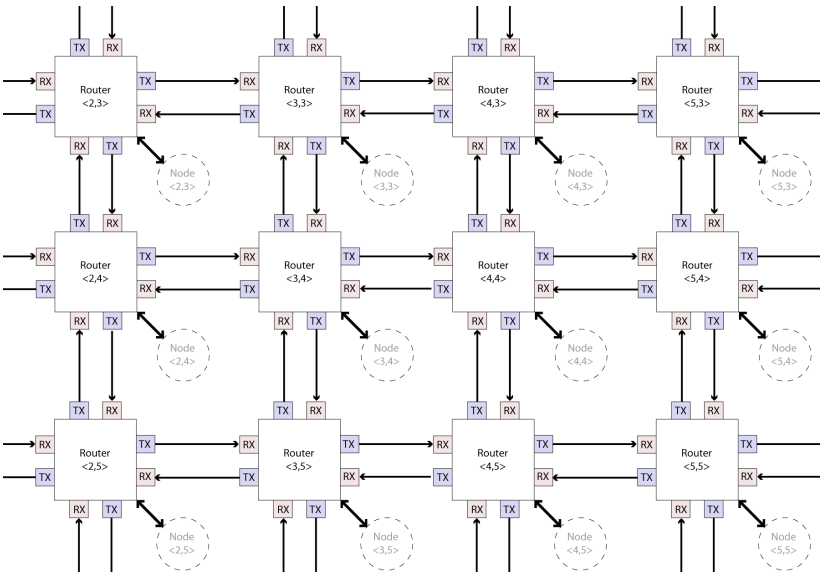


Fig 1: A 2-dimensional Mesh network of routers.

Components

The router you create for this project can be divided into two major components:

- **Transmitter & Receiver Units (TX & RX)** – These units perform serial communication between routers.
    - The **TX** is responsible for loading packets from the router core, computing a parity bit, serializing data, and sending it across a unidirectional transmission line.
    - The **RX** is responsible for receiving and de-serializing data, checking parity, and supplying error-free packets to the router core.
    - Full details on the TX/RX interfaces and their communication protocols are available in the TX/RX specification document.
- **Router Core –** The router core is the brain of the router.
    - It interfaces with 4 sets of TX/RX units (N, S, E, W) and with one Processing Node.
    - It must load packets received from the RX units, examine each packet's destination address, and then either send the packet to the Processing Node (if the destination is the current router) or send it to one of the TX units (if the destination is some other router).
    - The router core must also be able to load messages from the Processing Node, some of which will be new packets for transmission and some of which will contain configuration information for the core.
    - More details will be available in the Router Core specification document.

The **Processing Node** does *not* have to be synthesized as part of this project. The processing node interfaces on your routers will serve as the primary inputs and outputs to the network once you have connected a group of your routers into a mesh. Although you are not required to build a processing node module, you may find that building a HDL-based model will make it easier to write your testbenches. If you do design a processing node module, you are allowed to use non-synthesizable Verilog constructs (like delays, implicit state machines, etc.) in it.

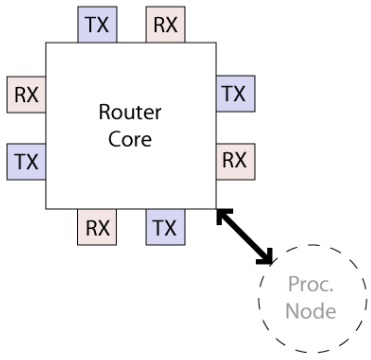


Fig. 2: A single router in isolation. The router is composed for 4 serial TX/RX pairs and router core. The router interfaces with a simulated processing node via a parallel bus.

Design Metrics

There are two key metrics for evaluating the quality of most on-chip routers: Performance and Power Consumption.

- Performance
    - Thoughput – That is, the rate at which your router network can accept and deliver packets. The throughput is dependent on factors such as the frequency of your TX/RX and router core, the design of your router core's state machine and buffering system, and the efficiency of your routing algorithm.
    - Drop Rate – Unlike most on-chip networks, your network will be considered a "**best-effort**" network. This means that you do not provide a guarantee that every packet will be delivered. This makes the design of the router and communication protocol much simpler. The drop rate is a measure of the fraction of packets that don't reach their destination.

We will not be measuring Power Consumption directly because our tools are not particularly accurate for calculating power. Instead we will use **Area** as a proxy for power, since the static power of a circuit is proportional to its area.

Project Timeline

The project will consist of two design milestones, a demonstration of the finished design, and a project report. The tentative schedule is as follows:

- (11/03) Milestone 1 – Functional (pre-synthesis) versions of your TX & RX module
- (11/21) Milestone 2 – Functional version of your Router Core
- (Approx. 12/13-12/17) – Project demo (post-synthesis) in B555 lab
- (12/21) Final report due

Special Comment: The reason we are giving you 3 weeks between your 2nd milestone and the full project demo is because the process of ensuring that post-synthesis results match pre-synthesis results is often very difficult, particularly for complex state machines like the one in the router core. Do not underestimate the work involved in synthesizing and verifying a large project.

Design Testing & Evaluation

The testing of your Milestone 1-2 and final synthesized router will be done using testbenches designed by the TA & Instructor. These testbenches will not be released to you. It is your job to read the design specifications carefully and create thorough testbenches to verify that your design conforms to our specifications before you submit it to us for grading. A document giving a general description of our router performance tests will be released later in the semester.

Grading

Grade distribution for the project is as follows:

- 10% - Milestone 1 – Functional correctness test of TX & RX units
- 10% - Milestone 2 – Functional correctness test of Router Core
- 40% - Post-synthesis correctness test of Final Design
- 05% - Synthesis Area results
- 10% - Routing Performance (throughput & drop rate)
- 15% - Project Report
- 10% - Extras (see section on Extras)

Area and routing performance will be judged relative to the results of the rest of the class. You should keep in mind that adding greater complexity to your router may increase your router performance at the cost of increased area. This will be one of the primary trade-offs you will need to evaluate when planning your design.

Additionally, the teams that achieve the lowest area, highest throughput, and lowest drop rate will each receive a 5% extra credit bonus to their project. (Note: In order to be eligible for the Area competition, your router must pass all post-synthesis correctness tests).

Report

The project report will be due at the time of the Final Exam. The printed project report must include the following sections:

- Executive Summary – A concise summary of your goals and the results of the project
    - Include a table listing the area, frequency, throughput, and drop rate
- Design Description – Include a high-level description of each module in your design.
- Routing Algorithm – Describe the routing algorithm you chose and justify your decision to use that algorithm.
    - Include a Flowchart or Pseudo-code description of the algorithm
- Test Plan – Include a detailed outline of the tests you used to verify your final design.
    - Enumerate each test you used and explain its purpose
- Synthesis Reports – Attach your Timing and Area Reports
    - Include a printout of the synthesis script you used to generate the reports.
- Extras – List any extra features in your design or report that go beyond the basic requirements

Code Submission: You do not need to include code printouts with your report. Instead you should place all HDL code, synthesis scripts, and other resources used in the project in a ZIP file and upload it to the Drop Box on the course website. Include a Readme.txt file that lists each file in the archive and briefly explains each file's purpose.

Extra Features

10% of the project grade is designated for “extras”, that is, any extra work you do in the project design or report that goes above and beyond the baseline requirements. A few potential ideas are listed below, but you are free to come up with others. As in the real world, it’s up to you to convince me, your boss, of the merits of your project.

- Use self-checking testbenches (***Required for groups of 3 – no bonus***)
- Use file-based testing (***Required for groups of 3 – no bonus***)
- Write a Test Plan for every module
- Implement Deadlock detection & recovery
- Implement Deadlock avoidance
- Create an Area/Frequency histogram for the synthesized project
- Use more complex routing algorithms
- Detect & avoid paths with high error rates
- Specific measures you have taken to reduce area or frequency
- Specific measures you have taken to increase throughput

Document History

v1.00 – Initial release

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