ECE 551 Homework #1

Due: Sept. 9th @ 11:00 am

This homework assignment is to be completed individually.

Please Note: To receive full credit, you should use the following best practices in your homework assignments**:**

- Use meaningful names for modules, ports, and wires when possible.
- Use underscores to break up long binary and hex numbers into groups of 4 digits to make them more readable. Ex: 12'b1001_0011_1101
- Show your work if you wish to receive partial credit.
- Make port connections *by name* unless using gate primitives.
- Explicitly declare any nets you use.
- All figures & graphs should include a number and caption (handwritten is OK).
- When printing waveforms, ensure that the relevant signal transitions are clearly visible.
- *All code should be typed*. Please do not submit handwritten code.

[1] Create a DOC file (using MS Word, Open Office, etc.) containing the following:

- Your name (and a hint on pronunciation if necessary)
- A photograph of yourself
- Your year in school (Junior, Senior, Grad Student, …)
- Your department/major
- If you have had experience using Verilog or another HDL in a previous course or job, briefly mention it.

Save the file as *yourname_profile.doc* and submit it to the Dropbox on the Learn@UW website. Additionally, complete the Discussion and Exam time surveys on the Learn@UW site if you have not already done so.

[2] (8pts)

Complete the ModelSim tutorial posted on the Learn@UW site and fill in the following statement.

I assert that I have completed the ModelSim tutorial. If I had any problems, I discussed them with the TA.

_____ *(sign or type your name here)*

Also, print out and attach a copy of the wave window (similar to the one shown in Figure 8.2 of the tutorial) using the directions given in Appendix B.

[3] (6pts)

Complete the following problems and give your answers in the specified base. Assume that values are in *signed, 2's complement* format.

8'b0101_1111	4'b1101	8'h2A
+ 4'o16	+ 6'b000101	- 8'h81
9'd_____	16'h_____	10'b_____

[4] (8 pts)

Implement the master-slave edge-trigger D flip-flop shown in Fig. 1 using only *structural* Verilog and only NAND gates and wires (you must replace the inverter in the diagram with equivalent logic using NAND gates).

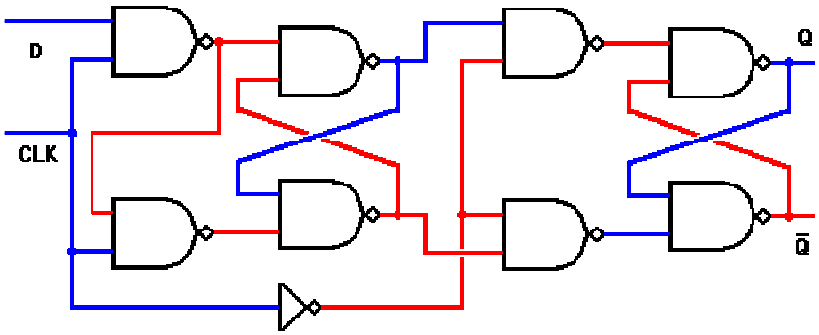

Fig. 1: Edge-triggered DFF