一、

（1）10；（2）上拉电阻；（3）5；（$A+B)\overline{B+C+D}$；（5）CMOS，CMOS；（6）10 位，40kHz；

（7）R+S=1；（8）c；（9）d；（10）bcd。

二、

（1）F1 = $\overline{A}B+A\overline{B}+\overline{A}D\left(或\overline{B}D\right)+AC\left(或BC\right)$　　$\overline{F_2} = \overline{A}\overline{B}CD+\overline{A}B\overline{D}+B\overline{C}$

AB\CD	00	01	11	10
00		1	1	
01	1	1	1	1
11			1	1
10	1	1	1	1

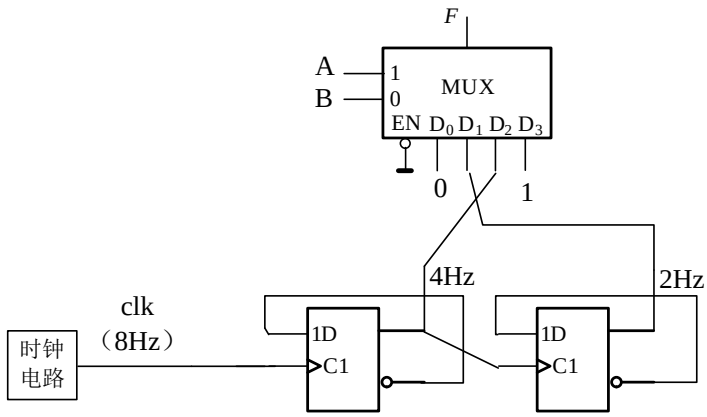
AB\CD	00	01	11	10
00	1	1	0	1
01	0	0	1	0
11	0	0	1	1
10	X	X	1	X

（2）

C_1 为高电平，C_2 为低电平时，V_1 = ____1.4_____V，　V_2 = _____1.4_____V；

C_1 为低电平，C_2 为高电平时，V_1 = ____3.6_____V，　V_2 = _____1.4_____V。

三、



四、

（1）

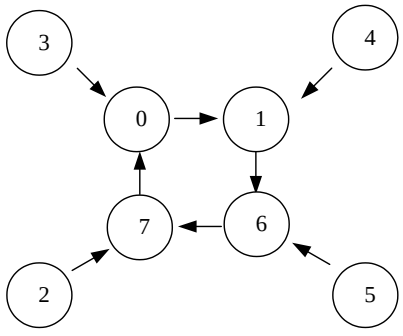
1) 增加异步清零功能，改成 always@(posedge clk or negedge rst)

2) Q 改成

output [3:0] Q;

reg [3:0] Q;

（2）

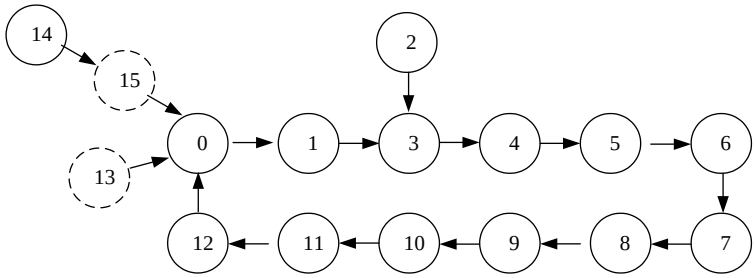


五、

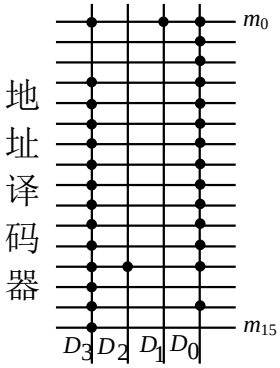
D0 = $\sum$(m0,*m*1,*m*2,*m*3,m4,m5,m6,m7,m8,m9,m10,m11,m12,m14) = $\overline{\sum(m13,m15)}$

D3 = $\sum$(m0,*m*3,m4,m5,m6,m7,m8,m9,m10,m11,m12,m13,m14,m15) = $\overline{\sum(m1,m2)}$

状态转换图：

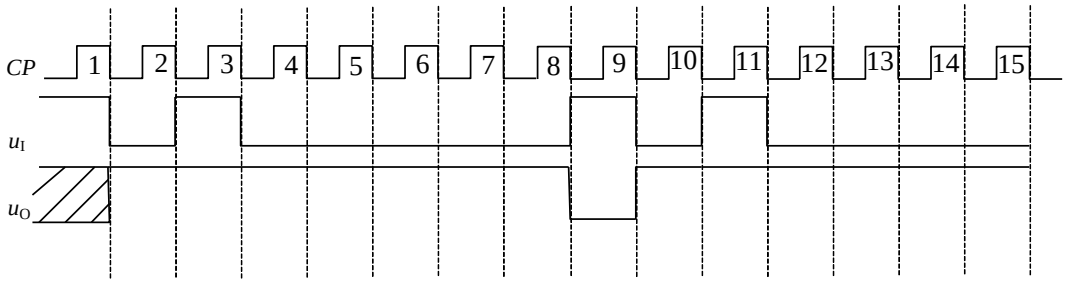


D1 和 D2 阵列如图：



六、单稳触发器

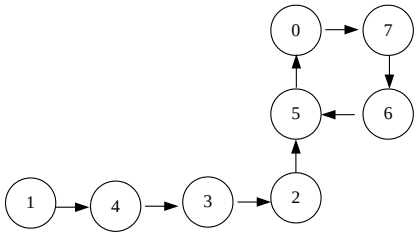
tw=1.1RC=0.22ms



七、 $Q_0^{n+1}=\overline{Q_0^n}$

$Q_1^{n+1}=Q_0^n \cdot Q_1^n$

$Q_2^{n+1}=\overline{Q_0^n Q_1^n} \cdot \overline{Q_2^n}+Q_1^n Q_2^n=\overline{Q_0^n} \cdot \overline{Q_2^n}+Q_1^n \cdot Q_2^n$



四进制减计数。

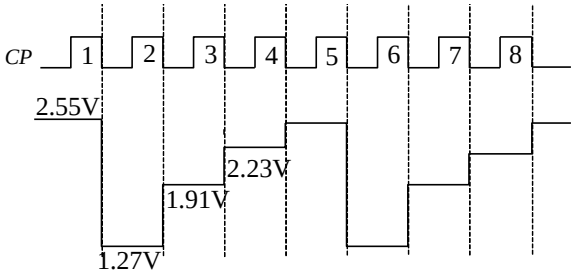
DAC 输出最大值为 255*10mV=2.55V

Q=0 时，uo=2.55-0.01 =2.54V

Q=7 时，uo=2.55-1.28 = 1.27V

Q=6 时，uo=2.55-0.64 = 1.91V

Q=5 时，uo=2.55-0.32 = 2.23V



八、

表 A 过程 A 状态转换表

态序	Q_0	Q_1	Q_2
0	*0*	*0*	0
1	*1*	*0*	0
2	*1*	*1*	0
3	*1*	*1*	1
4	*0*	*1*	1
5	*0*	*0*	1
6	*1*	*0*	0
7	*1*	*1*	0
8	*1*	*1*	1
9	*0*	*1*	1

表 B 过程 B 状态转换表

态序	Q_0	Q_1	Q_2
0	*0*	*1*	0
1	*0*	*0*	1
2	*1*	*0*	0
3	*1*	*1*	0
4	*1*	*1*	1
5	*0*	*1*	1
6	*0*	*0*	1
7	*1*	*0*	0
8	*1*	*1*	0
9	*1*	*1*	1

表C过程C状态转换表

态序	Q_0	Q_1	Q_2
0	*1*	*0*	1
1	*1*	*1*	0
2	*1*	*1*	1
3	*0*	*1*	1
4	*0*	*0*	1
5	*1*	*0*	0
6	*1*	*1*	0
7	*1*	*1*	1
8	*0*	*1*	1
9	*0*	*0*	1

$Q_0\backslash Q_1Q_2$	00	01	11	10
0	1	1	0	0
1	1	1	0	1

$d=Q_0\overline{Q_2}+\overline{Q_1}$