Main program

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity labtestModule is
    Port ( a0 : in  STD_LOGIC;
           a1 : in  STD_LOGIC;
           b0 : in  STD_LOGIC;
           b1 : in  STD_LOGIC;
           c0 : out  STD_LOGIC;
           c1 : out  STD_LOGIC;
           c2 : out  STD_LOGIC;
           c3 : out  STD_LOGIC);
end labtestModule;

architecture Behavioral of labtestModule is

begin

 c0 <= (a0 and b0);
 c1 <= ((a0 and b1) xor (a1 and b0));
 c2 <= ((a1 and b1) xor (a1 and a0 and b0 and b1));
 c3 <= (a1 and a0 and b0 and b1);

end Behavioral;
```

Test bench

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.std_logic_unsigned.all;
USE ieee.numeric_std.ALL;

ENTITY lol_vhd IS
END lol_vhd;

ARCHITECTURE behavior OF lol_vhd IS
```

```
    -- Component Declaration for the Unit Under Test (UUT)
    COMPONENT aaa
    PORT(
        a0 : IN std_logic;
        a1 : IN std_logic;
        b0 : IN std_logic;
        b1 : IN std_logic;
        c1 : OUT std_logic;
        c2 : OUT std_logic;
        c3 : OUT std_logic;
        c0 : OUT std_logic
        );
    END COMPONENT;

    --Inputs
    SIGNAL a0 :  std_logic := '0';
    SIGNAL a1 :  std_logic := '0';
    SIGNAL b0 :  std_logic := '0';
    SIGNAL b1 :  std_logic := '0';

    --Outputs
    SIGNAL c1 :  std_logic;
    SIGNAL c2 :  std_logic;
    SIGNAL c3 :  std_logic;
    SIGNAL c0 :  std_logic;

BEGIN

    -- Instantiate the Unit Under Test (UUT)
    uut: aaa PORT MAP(
        a0 => a0,
        a1 => a1,
        b0 => b0,
        b1 => b1,
        c1 => c1,
        c2 => c2,
        c3 => c3,
        c0 => c0
    );

    tb : PROCESS
    BEGIN

        a0 <= '0';
```

```
a1 <= '0';
b0 <= '0';
b1 <= '0';
wait for 100 ns;

a0 <= '0';
a1 <= '0';
b0 <= '0';
b1 <= '1';
wait for 100 ns;

a0 <= '0';
a1 <= '0';
b0 <= '1';
b1 <= '0';
wait for 100 ns;

a0 <= '0';
a1 <= '0';
b0 <= '1';
b1 <= '1';
wait for 100 ns;

a0 <= '0';
a1 <= '1';
b0 <= '0';
b1 <= '0';
wait for 100 ns;

a0 <= '0';
a1 <= '1';
b0 <= '0';
b1 <= '1';
wait for 100 ns;

a0 <= '0';
a1 <= '1';
b0 <= '1';
b1 <= '0';
wait for 100 ns;

a0 <= '0';
a1 <= '1';
b0 <= '1';
```

```
b1 <= '1';
wait for 100 ns;


a0 <= '1';
a1 <= '0';
b0 <= '0';
b1 <= '0';
wait for 100 ns;

a0 <= '1';
a1 <= '0';
b0 <= '0';
b1 <= '1';
wait for 100 ns;

a0 <= '1';
a1 <= '0';
b0 <= '1';
b1 <= '0';
wait for 100 ns;

a0 <= '1';
a1 <= '0';
b0 <= '1';
b1 <= '1';
wait for 100 ns;

a0 <= '1';
a1 <= '1';
b0 <= '0';
b1 <= '0';
wait for 100 ns;

a0 <= '1';
a1 <= '1';
b0 <= '0';
b1 <= '1';
wait for 100 ns;

a0 <= '1';
a1 <= '1';
b0 <= '1';
b1 <= '0';
```

```
        wait for 100 ns;

        a0 <= '1';
        a1 <= '1';
        b0 <= '1';
        b1 <= '1';
        wait for 100 ns;


    END PROCESS;

END;
```

Output