2010 NSF EAPSI Project Synopsis and Timeline

Paul Pham

1 Synopsis

My proposed project is to construct an electronic pulse programmer to provide high-fidelity quantum control for trapped ion experiments in the laboratory of Dr. Michael Biercuk. In particular, the pulse programmer will operate at 100 MHz (corresponding to a 10 ns time resolution) and have modules for radiofrequency analog generation, arbitrary analog waveforms, and input counting.

The project will be documented in real-time on the website http://pulse-programmer.org as a resource to the larger ion trap community. Each week of the timeline below will include documentation of that week's work with a blog update and uploaded photos. All related designs, software, and documentation will be released as open source.

The circuit boards, electronic components, chassis, and all materials and supplies will be paid for out of Dr. Biercuk's funding, independently of the EAPSI fellowship.

2 Timeline

- Week 0: Before arriving in Australia

  Discuss logistics of commercial boards to order and design parameters for custom boards to design. Begin custom board design, choose components.

- Week 1: June 14-20, 2010

  Set up laboratory workbench, test all boards and components brought from the U.S. Finish custom board designs, send out for fabrication. Design system and wiring scheme for controlling all board from FPGA sequencer, including clock system. Physically lay out rackmount chassis to store entire pulse programmer, including faceplate design.

- Week 2: June 21-27, 2010

  Order parts and chassis. Write software/firmware to control the boards from the FPGA sequencer.

- Week 3: June 28 - July 4, 2010

  Receive custom boards back from fabrication. Receive parts and chassis. Construct rackmount chassis and faceplate. Test physical layout in rackmount chassis. Assemble custom boards (or outsource).

- Week 4: July 5 - July 11, 2010

  Wire together existing boards, screw into chassis. Mid-project checkpoint.

- Week 5: July 12 - 18, 2010

  Receive back assembled custom boards. Add to chassis. Test generating TTL and arbitrary analog waveforms.

- Week 6: July 19 - July 25, 2010

  Test generating RF waveforms using DDS with specified phase, frequency, and amplitude.

- Week 7: July 26 - August 1, 2010

  Test PMT input counting.

- Week 8: August 2 - August 8, 2010

  Integrate into laboratory setup. Hand over keys / control codes.