

Performing Quantum Computing Experiments in the Cloud

Simon J. Devitt

Center for Emergent Matter Science, RIKEN, Wakoshi, Saitama 315-0198, Japan.

(Dated: May 19, 2016)

Quantum computing technology has reached a second renaissance in the past five years. Increased interest from both the private and public sector combined with extraordinary theoretical and experimental progress has solidified this technology as a major advancement in the 21st century. As anticipated by many, the first realisation of quantum computing technology would occur over the cloud, with users logging onto dedicated hardware over the classical internet. Recently IBM has released the *Quantum Experience* which allows users to access a five qubit quantum processor. In this paper we take advantage of this online availability of actual quantum hardware and present four quantum information experiments that have never been demonstrated before. We utilise the IBM chip to realise protocols in Quantum Error Correction, Quantum Arithmetic, Quantum graph theory and Fault-tolerant quantum computation, by accessing the device remotely through the cloud. While the results are subject to significant noise, the correct results are returned from the chip. This demonstrates the power of experimental groups opening up their technology to a wider audience and will hopefully allow for the next stage development in quantum information technology.

I. INTRODUCTION

The accelerated progress of quantum information technology in the past five years has resulted in a substantial increase in investment and development of active quantum technology. As expected, access to the first prototypes for small quantum computers have occurred over the cloud, with hardware groups opening up access to their hardware through the classical internet. The first case was the Center for Quantum Photonics (CQP) at the university of Bristol that connected a two-qubit optical chip to the internet and invited people to design and test their own experiments [1]. This was a remarkable achievement at the time, but suffered from the disadvantage that there was very few experiments in quantum computing that could occur with their cloud based hardware.

Recently IBM did the same thing, and allowed access to a five qubit superconducting chip to the internet community through an interactive platform called the *Quantum Experience* (QE) [2]. This approach is substantially more advanced as it allows access to a five qubit, reprogrammable device and allowed for circuit design, simulation, testing and actual execution of an algorithm on a physical device. The size of the IBM chip now allows for demonstration of quantum protocols out of the reach of people not associated with advanced experimental groups. It has already been used by researchers to violate a more general version of Bells inequalities [3].

In this paper we present four separate quantum protocol experiments, designed and executed independently of the IBM team. We treat the QE website, interface and chip as essentially a black box and run experiments related to four main areas of quantum information; Error Correction [4], Quantum Arithmetic [5], Quantum Graph Theory [6] and Fault-Tolerant circuit design [7]. We detail the motivation and design of each experiment, restrict our analysis to the simple output coming from the IBM chip and show that each individual protocol pro-

duces valid answers (at low fidelity). This work will hopefully motivate more people to get involved in cloud based quantum interfaces and encourage experimental groups to open up their hardware for interaction with the general public to increase innovation and development of a quantum technology sector. We designed, simulated and implemented protocols over an array of five qubits and in each experiment we present simulations provided by the QE interface and the resultant experimental data from the five qubit chip. In each case we observe results consistent with the theory and the intended output of each protocol.

II. ERROR CORRECTED RABI OSCILLATIONS

The first experiment implemented on the IBM chip is a basic Rabi oscillation spectra across a *logically* encoded qubit using a distance two surface code. Surface code quantum computing [4], is now the standard model used for large-scale quantum computing development [8–17] and results from superconducting and other technologies show extraordinary promise [18–22]. The five qubit surface code has already been investigated by the IBM team themselves [19], but in this experiment, the goal is not to artificially inject errors into the system, but rather to conduct a standard protocol used in the initial demonstration of a two-level controllable quantum system and see if an error corrected version of the protocol shows some advantage.

A distance two surface code consists of an array of five qubits, illustrated in Figure 1a) stabilised by the four operators in Figure 1b). With a fifth stabiliser $K_5 = Z_1Z_2$ ($K_5 = X_1X_4$) used to specify the logical Z (X) state of the encoded qubit. The Z -stabilisers ($\{K_1, K_2\}$) are used to detect bit flip errors while the X -stabilisers (K_3, K_4) are used to correct phase errors. Being distance two, this code can only detect errors (there is insufficient information to determine location of any detected bit or

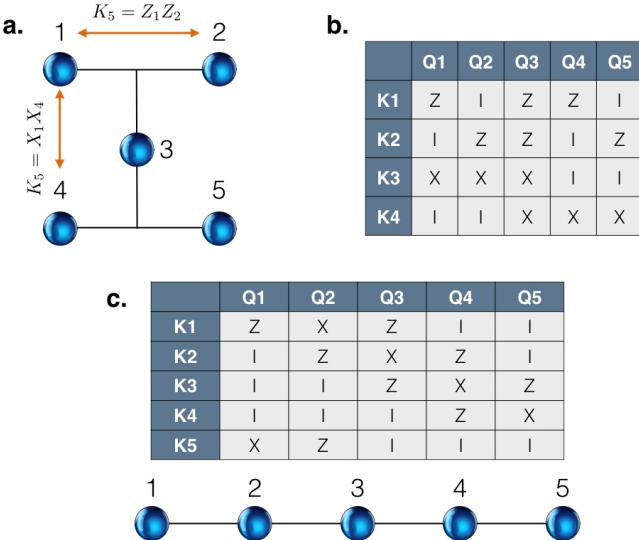


Figure 1: Distance two surface code. Figure a.) illustrates the code structure, with two plaquette and two vertex stabilisers. Logical operators run left to right (Z_L) or top to bottom (X_L). Figure b.) is the stabiliser set for the distance two surface code. Figure c.) is the structure and stabiliser set for a linear cluster state. Once a Hadamard is performed on qubits 1,3,5, the state is equivalent to a distance two surface code initialised in the $|0\rangle_L$ state.

phase error, with certainty).

Initialising a distance two surface code in the $|0\rangle_L$ state is equivalent to preparing a five qubit linear cluster. The five qubit linear cluster has stabiliser set illustrated in Figure 1c). After a Hadamard is applied to qubits one, three and five we can identify K'_5 as the $+1$ -eigenstate of the logical Z operator and after multiplying stabilisers $K'_2 K'_5 = K_1$ and $K'_2 K'_4 = K_2$ we regain the stabiliser set for the distance two surface code.

To perform an error correction version of a Rabi oscillation experiment, we instead require the ability to encode a rotated logical state of the form $e^{i\theta X_L} |0_L\rangle$ which cannot be directly prepared in the encoded space. Therefore we prepare a single qubit in the rotated state and encode. This is not a fault-tolerant operation and the fidelity of this initial rotated state will bound the error on the final state (even if every other gate in the circuit was perfect). The direct encoding is shown in Figure 2a), where we prepare the state $\alpha|+++_{1,3,5}\rangle + \beta|---_{1,3,5}\rangle$ and then create the linear cluster state from this initial state. This places the surface code into the state $\alpha|0\rangle_L + \beta|1\rangle_L$.

As with a single qubit Rabi experiment, we measure the probability of measuring a $|0\rangle_L$ state after rotating the input with successively larger angles, θ . In the QE interface, only Clifford + T gates are available, and constructing rotations smaller than $R_x(\pi/4)$ would require decompositions into Clifford + T sets [24, 25]. But for this experiment we instead use successive $\pi/4$ rotations (T -gates) around the Bloch sphere where an eight gate

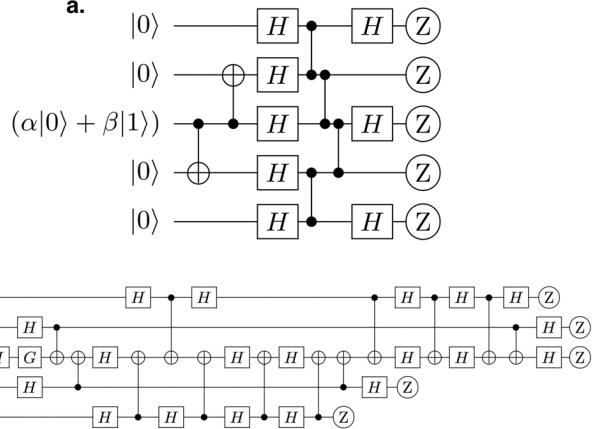


Figure 2: Circuits to encode arbitrary states into the surface code. Figure a) is the general circuit, where the state $\alpha|+++_{1,3,5}\rangle + \beta|---_{1,3,5}\rangle$ is first prepared and then a linear cluster state is created afterwards. Following the last three Hadamard gates, the logic state $|0\rangle_L + |1\rangle_L$ is prepared. Figure b) is the circuit implementation in the QE interface. Only the third qubit in the IBM chip can be coupled to via a CNOT (and it always acts as the target qubit), hence various SWAP gates (decomposed into CNOTs and Hadamards [23] are used). The gate G is the set of successive T rotations used to sequentially rotate the qubit into the state, $e^{i(\pi n/4)X_L}|0\rangle$ for $n \in \{0, \dots, 7\}$. After the state is prepared it is immediately measured in the Z -basis.

cycle will oscillate the state from $|0\rangle_L \rightarrow |1\rangle_L$ and back to $|0\rangle_L$.

As the QE chip only allows for CNOT gates to operate with the central qubit in their star geometry, additional SWAP operations are needed, which are also decomposed into CNOT and Hadamard. The full circuit implemented is illustrated in 2b), Where the gate G is each successive step in the rotation, $G \in \{T^0, \dots, T^8\}$.

Once the state is prepared, we can measure in the Z -basis on each of the five qubits and calculate the parity of K_5 to determine the logical state. Since when measuring in the Z -basis, results are modified by the presence of bit flip errors, we can use the parity of the Z -stabilisers, to post-select from the 8192 runs allowed by the QE interface only instances where K_1 and K_2 return even parity results.

Once the state is prepared we first simulated the expected output using the master equation solver included with the QE interface and the simulation results are illustrated in Figure 3a). On this plot there are three curves. The first is the theoretical optimal, where the Rabi oscillations follow a $\cos^2(\theta)$ function. The second curve, with the lowest visibility, is when we run the circuit in Figure 2 but *do not* post-select on trivial syndrome results for K_1 and K_2 . The visibility in this case is clearly lower than the ideal case, due to errors accumulating in the

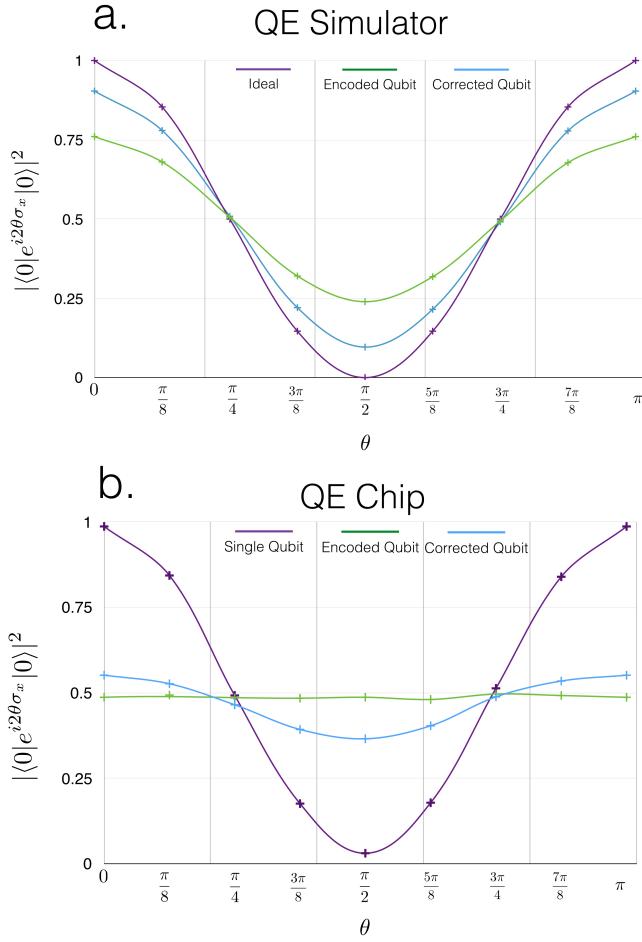


Figure 3: Simulation and Experimental result from the QE device. In Figure a) we have simulated plots for the ideal Rabi curve (purple), the encoded but *un-corrected* code (green) and the post-selected, error-corrected results (blue). An improvement when correction is applied is clearly seen. In Figure b) we have the results directly from the QE chip. For the *corrected* state, a low visibility oscillation is observed. The purple curve now represents successive rotations on an *individual* qubit and so has high visibility (but still is not perfect). Each data point was obtained using the maximum sampling in the QE interface of 8192 shots, and a sampling error for each point (omitted) can be calculated as $SE = \sqrt{P_c(1 - P_c)} / \sqrt{8192}$, where P_c is the probability of each measurement.

larger circuit. The third curve, which sits between the two, is where post-selection occurs and we are discarding any results where a non-trivial syndrome is detected. In simulations, this gives clearly better performance than the non-error-corrected case, but is still far from ideal.

Illustrated in Figure 3b) is the actual experimental data returned from the QE interface. Each data point (representing successive rotations of the input state between $|0\rangle_L$ and $|1\rangle_L$ and the rotation angle is 2θ , such that a rotation from $|0\rangle_L \rightarrow |0\rangle$ occurs for $\theta = \pi$) was

taken using the maximum sampling instances of the QE chip (8192). For the purple illustrated in Figure 3b), we performed a Rabi experiment using a bare single qubit (via repeated rotations by T and then immediate measurement), this showed unsurprisingly the highest visibility. The data when we encoded into the surface code and did not perform the corrective operations, is essentially random (showing a 50% probability of measuring $|0\rangle_L$ or $|1\rangle_L$). Once the data is post-selected on trivial syndrome results, we again see a non-zero visibility, indicating that the error correction properties of the code are helping to restore the oscillation. The standard error can be calculated as $SE = \sqrt{P_c(1 - P_c)} / \sqrt{8192}$, where P_c is the probability of a given measurement result. The SE is not illustrated in Figure 3.

The complexity of the circuit to perform the encoding and the fact that the QE chip does not have sufficient control or accuracy to perform a fault-tolerant experiment, means that the error-corrected version *does not outperform* a non-error corrected version of the same experiment. But active decoding of the information does result in a better results when compared to the same circuit without active decoding. Additionally, the simulator bundled with the QE interface overestimates the performance of the chip, compared with the actual experimental data.

III. FOURIER ADDITION

Our second experiment is programmable quantum arithmetic [5]. We design a circuit that performs addition between two quantum registers, $|a\rangle$ and $|b\rangle$ by performing a Fourier transform on register $|a\rangle \otimes |b\rangle \rightarrow |a\rangle \otimes \psi(|b\rangle)$, controlled phase rotations taking $|a\rangle \otimes \psi(|b\rangle) \rightarrow |a\rangle \otimes \psi(|a\rangle + |b\rangle)$ and an inverse Fourier transform, giving, $|a\rangle \otimes \psi(|a + b\rangle) \rightarrow |a\rangle \otimes |a + b\rangle$. The addition naturally occurs modulo 4 as the registers $|a\rangle$ and $|b\rangle$ are only each 2-qubit registers.

Even though the QE system has the ability to operate over five qubits, a Quantum Fourier Transform (QFT) over anymore than two qubits require \sqrt{T} gates, which would need to be approximated via Clifford + T sequences, for which there are insufficient resources. Two qubit Fourier addition is possible as the smallest rotation needed for circuit decompositions are T -gates, available in the QE interface.

In Figure 4a) we illustrate the addition circuit, the decomposition circuits used for controlled phase rotations [Figure 4b)] and the actual circuit implemented in the QE interface [Figure 4c)]. Once again, all CNOTs need to involve the central qubit in the architecture (Q_3) as the target, in accordance with the geometry of the QE hardware. The gates G_i , $i \in \{1, \dots, 4\}$ are used to prepare the input states from the initial $|0\rangle$ states in the QE chip, and at the end of the circuit everything is measured in the Z -basis.

As with the error corrected Rabi oscillation, the final

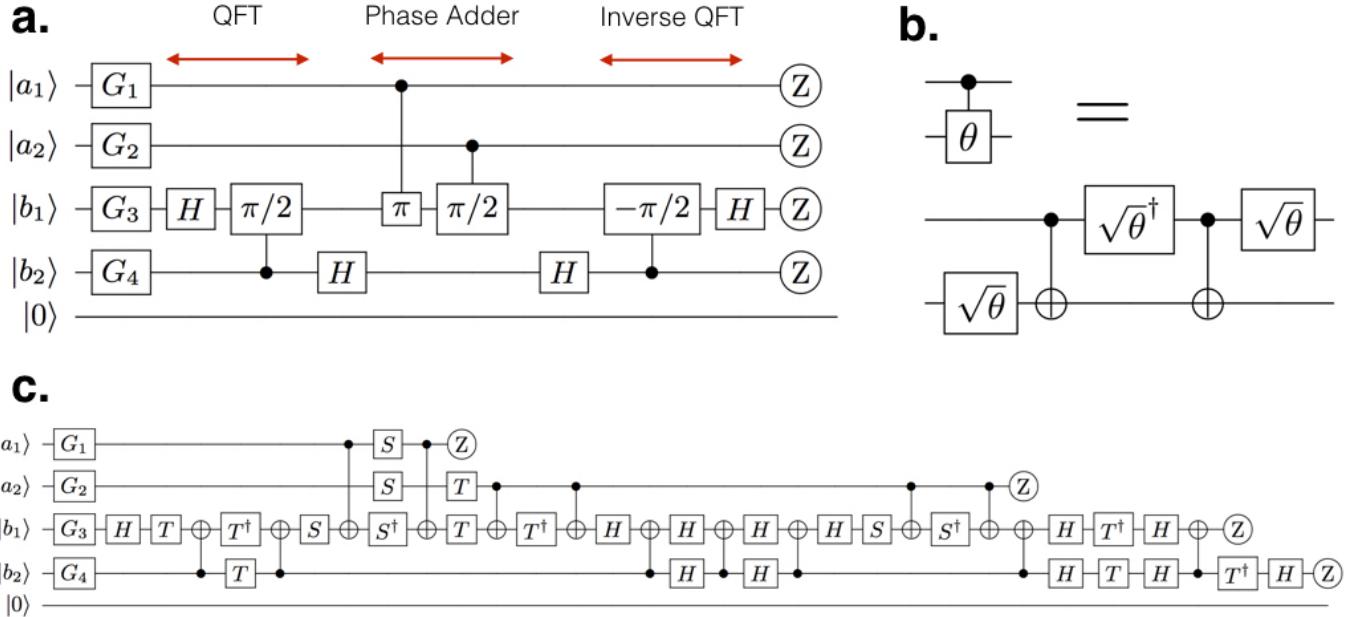


Figure 4: Fourier addition circuits. In Figure a) we illustrate the Fourier addition circuit on two registers. First a QFT is performed on the target register, after which controlled phase rotations are used to perform the addition. An inverse QFT then returns the target register to the computational basis. The gates G_i , $i \in \{1, \dots, 4\}$ are used to program in various inputs used in the simulations. Figure b) shows controlled rotation decompositions. For rotations smaller than $\pi/2$, the decomposition requires gates of the form ${}^n\sqrt{T}$, which are not available in the QE interface without performing Clifford +T decompositions [24, 25]. In Figure c) we illustrate the circuit implementation for the QE chip.

circuit is quite large and hence errors will accumulate and the probability of observing successful output will drop. We again ran these circuits in both the QE simulator and the actual QE chip for comparison. Shown in Figure 6 are the simulation results and Figure 5 the experimental results for a selection of the 16 possible binary inputs of $|a\rangle$ and $|b\rangle$, along with various superposition and entangled inputs. The simulations and experimental results were averaged over 8192 runs and the standard error (SE) omitted from the plots. The simulations and experiments show similar levels of noise in their outputs. The difference between the two is not as clear as the error-corrected Rabi oscillations shown earlier.

The size of the addition circuit is larger than the error corrected Rabi experiment, hence noise in the QE chip is stronger. However, again we see the *right* answer returned a plurality of the time, from the 8192 runs performed. The only exception is when we used an entangled input on the target register. Illustrated in Figure 5 on the bottom right plot, when the transformation should be $(|0100\rangle + |0111\rangle)/\sqrt{2} \rightarrow (|0101\rangle + |0100\rangle)/\sqrt{2}$. In this case, the correct answer couldn't be inferred from the experimental output.

We expect that experimental refinement of the chip itself will lead to less noise accumulation such that desired results are returned with much higher probability. As experimental error rates go down, these experiments would be useful as a benchmark to ascertain if performance with

large circuits increases over time.

IV. LOCAL COMPLEMENTARITY IN QUANTUM GRAPH STATES

The third experiment performed with the QE platform is a unique property of quantum graph states called local complementarity [6]. Local complimentary is where the structure of a quantum graph can be changed via *only* local operations. We demonstrate the creation of a five qubit graph state (by measuring appropriate graph stabilisers and confirming measuring even parity of each operator), we then permute this graph using local operations and confirm, through the measurement of the new stabilisers, that the underlying state has changed. A minimum of four qubits is required to perform any type of graph complementarity experiment (as all graphs containing two or three qubits have only a single local-equivalence class [6]) and five qubits give a large number of non-equivalent classes that we could test. The first example is creating a GHZ state (star graph) and through local complementarity, perturb this to a completely connected graph and then perturb it back to another star graph with a different qubit acting as the star node.

A quantum graph state is easily defined from the classical graph that describes it. A classical (undirected, finite) graph, $G = (V, E)$, is a set of N nodes, $V \in \{1, \dots, N\}$

Experimental Output

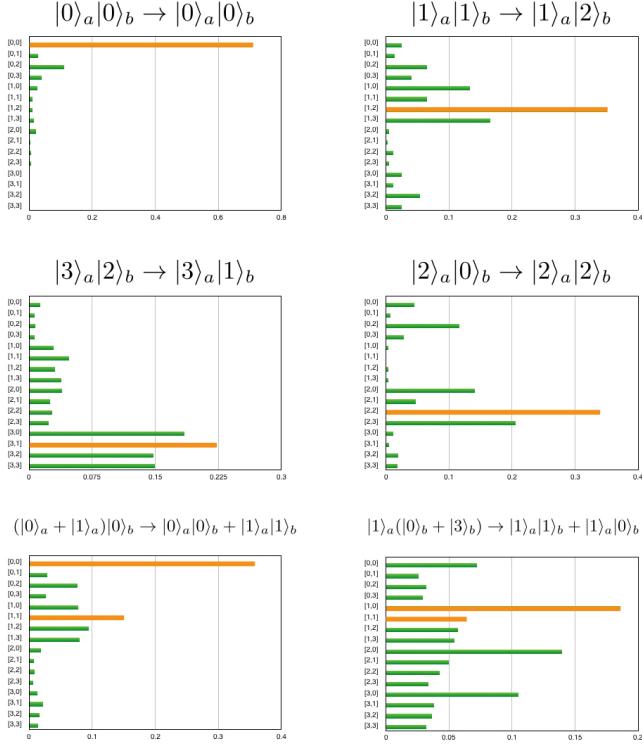


Figure 5: **Experimental Fourier addition.** Each plot shows the 32 possible binary outputs. The input/output mapping for each plot is specified, and the *correct* binary outputs are illustrated in Orange on each plot. For all experiments (except where a Bell state is created on the target register), the correct output is observed a plurality of the time.

connected by sets of edges, $E \subset V^2$ such that $E_{i,j} = 1$ for any two connected nodes, $V_{i,j}$ and $E_{i,j} = 0$ if $V_{i,j}$ are not connected. To convert this classical graph state to a quantum graph state, we use the adjacency matrix of the classical graph to form a set of stabiliser operators that are used to specify the quantum graph. The conversion of a star graph to the stabiliser set is illustrated in Figure 7.

Once a graph is written, an adjacency matrix can be formed that contain a 1 for each edge, $E_{i,j} = 1$ and 0 everywhere else. To convert an adjacency matrix into a list of stabilisers for the quantum graph state requires taking each row of the adjacency matrix, replace the 0 on the diagonal with the Pauli X -operator, any 1 entry with the Pauli Z -operator and the Identity matrix everywhere else. For an N -qubit graph, there will be N -operators corresponding to the N -rows of the classical adjacency matrix. Creating a quantum state simultaneously stabilised by these N -operators will produce the required quantum state.

Local complementarity operators are quite simple, and consist of choosing one of the qubits of the quantum

Simulation Output

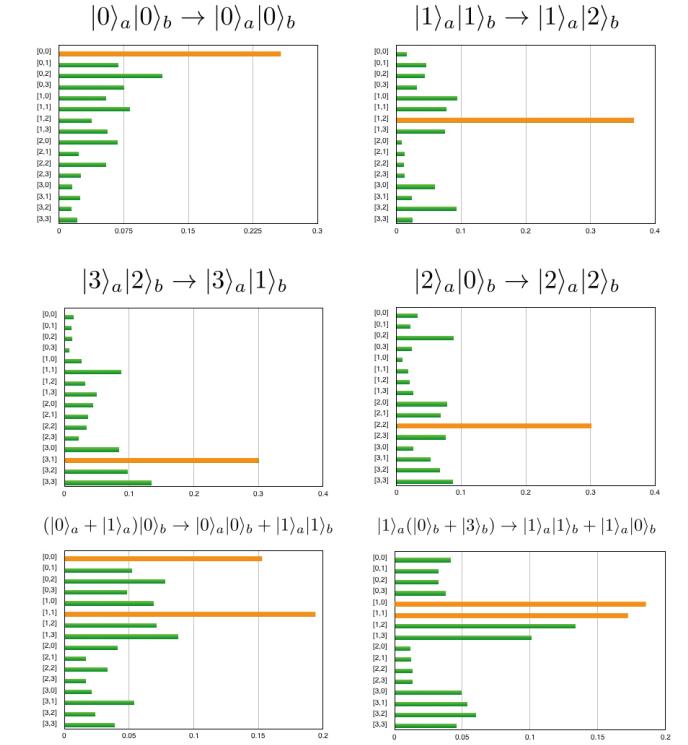


Figure 6: **Simulated Fourier Addition.** We use the QE interface to first simulate the addition circuit. Results are closer to experimental output than the error-corrected Rabi experiment, and in some cases show more noise than what was output from the chip itself.

graph, denoted the *node*, applying a $\sqrt{X} = HSH$ operator to that qubit, and a $\sqrt{Z} \equiv S$ operator to any qubit it is connected to (*leaf*). This has the effect of creating an edge directly between the leaves or deleting an edge if it originally existed. These local complementarity rules create what is known as an *orbital* and forms a closed set of locally equivalent quantum graphs. Different orbital groups are not locally equivalent to each other and the number of different orbital groups grows as the total number of qubits increase. Our first experiment is illustrated graphically in Figure 8 along with its required quantum circuit.

We first create a 5-qubit star graph that is stabilised by the operators in Figure 7, and then through the local gates G_i , $i \in \{1, \dots, 5\}$ we are either measuring the stabiliser of the star graph or through local complementarity we first convert the graph and measure the parity of the stabilisers associated with the new graph. The experimental results from the QE chip is illustrated in Figures 8-11, and the simulated results are illustrated in Figures 12-14. Again, each plot was generated using 8192 experimental runs, and the SE is omitted from each plot.

As expected, the calculated parities for each stabiliser

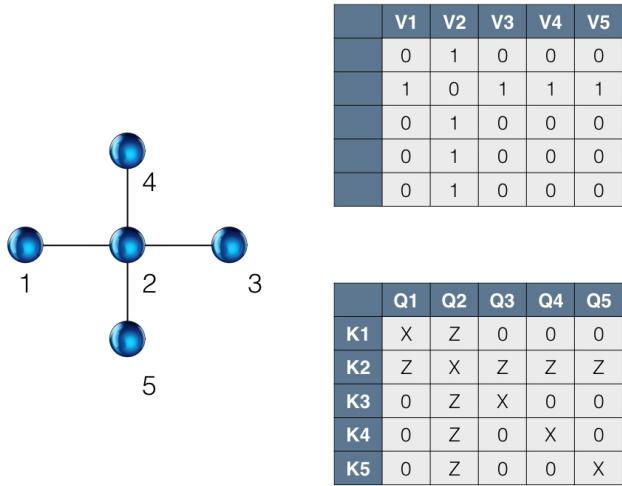


Figure 7: **The link between a classical graph and the corresponding quantum graph.**.. The classical star graph can be represented as an adjacency matrix, with ones present to indicate the four bonds from the central node to each leaf. To convert this to the equivalent quantum graph state, we construct a stabiliser table by replacing each 1 with a Z operator, X operators on the diagonal and I everywhere else. Each row of the adjacency matrix is now one of the five stabilisers of the quantum star graph.

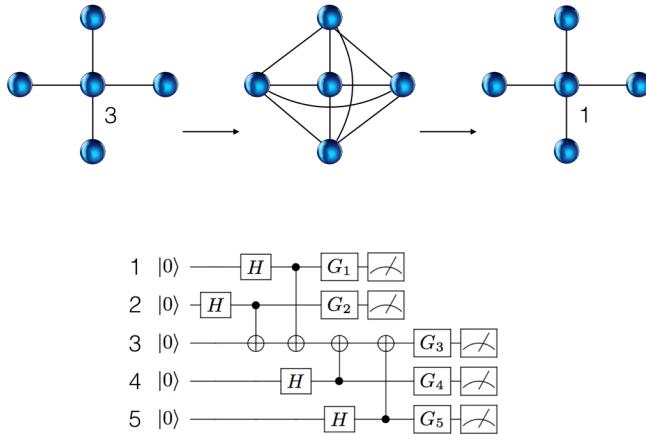


Figure 8: **Circuits to implement graph complementarity and stabiliser measurements.** In the experiment we initially prepare a five qubit star graph, use local complementarity to convert this to a completely connected graph and then permute again to reconver to a star graph with a different qubit acting as the central node. After each conversion we measure the five associated stabilisers. Illustrated is the quantum circuit necessary to do this in the QE interface. The initial part of the circuit creates the star graph. The gates G_i , $i \in \{1, \dots, 5\}$ allow us to perform the graph complementarity operations (with S - and T -gates) and/or to measure in either the X or Z -basis.

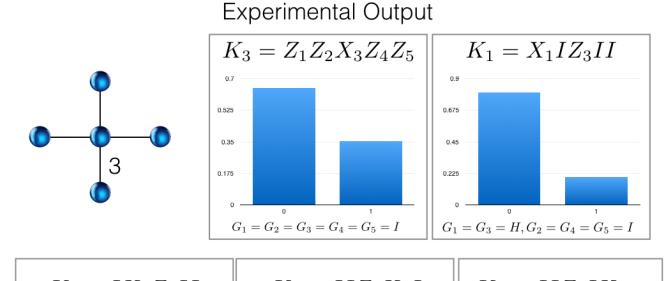


Figure 9: **Experimental results for the initial star graph.** For each plot, we measure the parity of the associated stabiliser. The settings for each of the $G_{i \in 5}$ gates are illustrated for each.

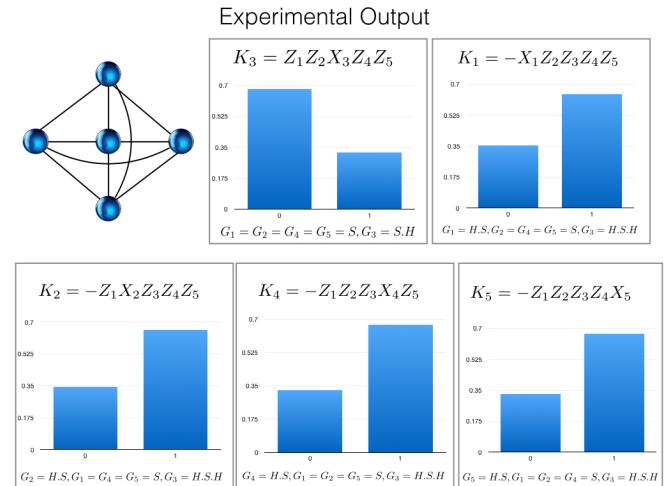


Figure 10: **Experimental results for the completely connected graph.** The completely connected graph is constructed by performing a HSH gate on qubit one and an S gate on every other qubit. The permutation of the stabiliser set after this operation can cause some eigenvalues to flip between $+1$ and -1 . For each plot, we measure the parity of the associated stabiliser. The settings for each of the $G_{i \in 5}$ gates are illustrated for each.

match what is measured. Some parities flip during the graph complementarity operations, but these flips could be reversed by applying appropriate Pauli operations. As the circuit is quite small compared to other experiments, the degree to which we see nearly 100% probability of the correct parity is high. This experiment showed how to use local complementarity to permute the structure of a quantum graph. In this case we went from a star-

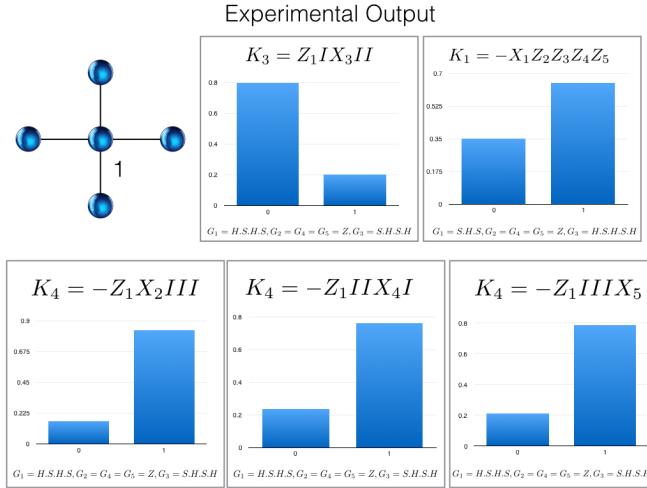


Figure 11: Experimental results for the final star graph. We construct the final star graph (with qubit one acting as the node) by performing HSH to qubit one and S to every other qubit. This permutation does not change the eigenvalue of any of the stabilisers. For each plot, we measure the parity of the associated stabiliser. The settings for each of the $G_{i \in 5}$ gates are illustrated for each.

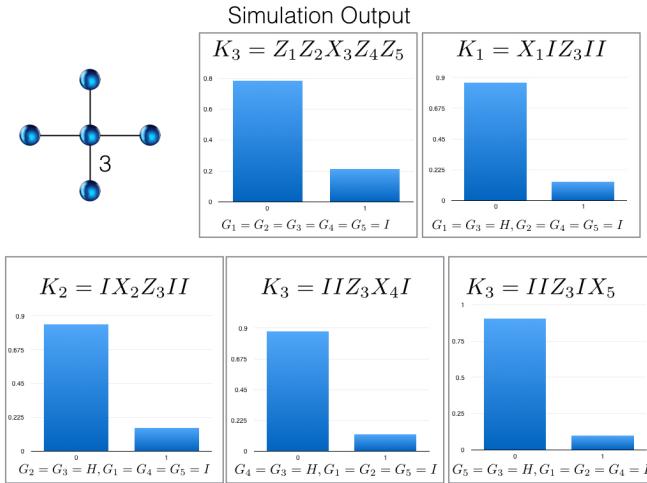


Figure 12: Simulated results for Figure. 9.

graph with qubit 3 acting as the node, to a completely connected graph and back to a star-graph with now qubit one acting as the node.

This type of experiment for all non-equivalent five qubit graphs is fairly simple to perform in the QE interface. Preparing any five qubit graph state does not require as many gates as either error-corrected Rabi oscillations *or* Fourier addition and hence the QE chip should produce the correct state (with reasonably high fidelity). Investigating the structure of these locally-equivalent graphs and how they can be utilised as communications links has the potential to open up an area

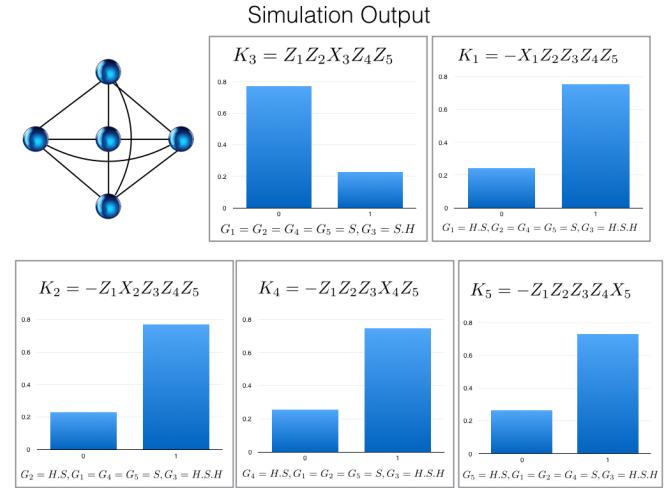


Figure 13: Simulated results for Figure. 10.

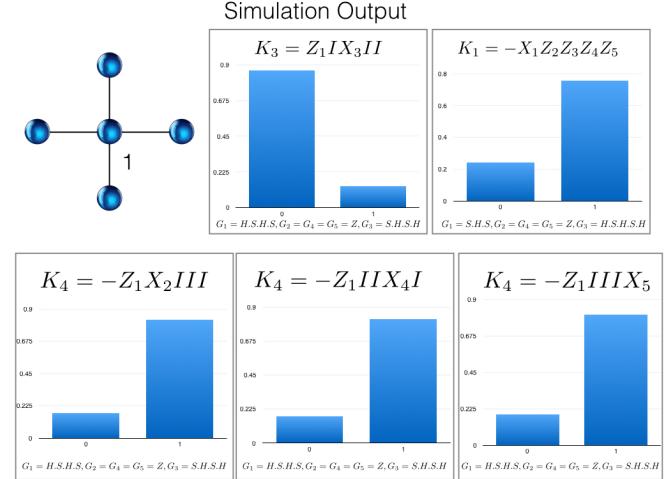


Figure 14: Simulated results for Figure. 11.

of quantum network analysis that is not available in the classical world.

V. DETERMINISTIC T-GATES

Our final experiment is comparatively quite simple but highly relevant to the construction of Fault-tolerant quantum circuits [7]. When designing high level quantum circuits, the universal gate library of choice is the Clifford + T set. There has been significant work in both compiling and optimising circuits of this form [26–31]. In fault-tolerant models, T -gates are generally applied using teleportation circuits with an appropriate ancillary state that is prepared using complicated protocols such as state distillation [32]. These circuits are intrinsically probabilistic, and for the T -gate, corrections need

to involve the active application of a subsequent S -gate. Hence there was the potential that high level circuit construction would need to be dynamic, adjusting itself every time a T -gate is applied in the hardware. However, recent work has shown how to construct *deterministic circuitry* for any high-level algorithm [7, 33]. Sub-circuits known as selective source and selective destination teleportation [33] are used to patch in correction operations for each T -gate via choosing to measure certain qubits in either the X - or Z basis. This deterministic T -gate is illustrated in Figure 15

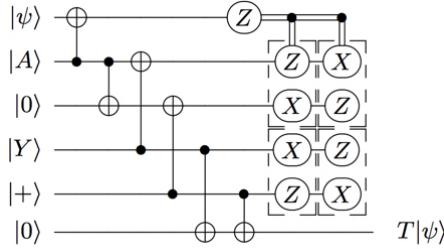


Figure 15: **Teleported T -gate with deterministic circuitry.** Built using selective source and destination circuits [33], this circuit will first apply the T -gate, through a teleportation circuit with an $|A\rangle = |0\rangle + e^{i\pi/4}|1\rangle$ ancilla. A possible S -correction may be needed, requiring the ancilla $|Y\rangle = |0\rangle + i|1\rangle$. By selecting one of two-choices of X - and Z -basis measurements (based on the top Z measurement), the S correction is applied or not. Hence the output is always the T -gate operating on the input state, $|\psi\rangle$.

The operations on the first two qubits are the teleported T -gate, which utilises an ancilla, $|A\rangle = |0\rangle + e^{i\pi/8}|1\rangle$, a subsequent CNOT and Z -basis measurement to enact the gate. The logical result of the Z -measurement determines if a T -gate or a T^\dagger -gate is applied (the T -gate occurs when a $|0\rangle$ result is measured). Depending on this measurement result, a possible S -gate correction needs to be applied, which is a second teleportation circuit utilising a second ancilla, $|Y\rangle = |0\rangle + e^{i\pi/4}|1\rangle$. The S -gate correction can also require a correction, but this correction is a Pauli Z -gate and hence does not need to be actively applied.

The circuit in Figure 15 uses two circuits known as selective source and selective destination teleportation [33] to put the T -gate into a form called ICM [7]. An ICM form of a quantum circuit consists of a layer of qubit (I)initialisations, an array of (C)NOT operations and a time staggered series of X - and Z -basis (M)measurements. The choices of X - and Z -basis measurements are determined by the initial Z -basis measurement in the T -gate teleportation circuit and can dynamically *patch* in the correction circuit (or not).

We can simulate this circuit in the QE interface, but since the original circuit requires 6-qubits, we instead emulate the application of the T - or T^\dagger -gate directly and then based on which gate we choose, measure the four

other qubits in the appropriate basis to teleport a T -gate to the output regardless of whether we choose T - or T^\dagger at input. Unfortunately while the QE interface does allow for qubit tomography to be performed, it does not allow both standard basis measurements and tomographic mapping on the same circuit run. Therefore, to confirm the application of the T -gate, we simply reverse the initial circuit and confirm that $|0\rangle_{in} \rightarrow |0\rangle_{out}$. The circuit implemented in the QE chip is shown in Figure 16.

Extra SWAP operations are needed in Figure 16 because of the restrictions of the QE architecture. On the top qubit we apply either the $G = T$ or $G = T^\dagger$ and dependent on that choice the four subsequent measurements are either in the $\{Z, Z, X, X\}$ basis or the $\{X, X, Z, Z\}$ basis. Once classical Pauli corrections based on measurements are taken into account [Table I, which we will discuss more shortly] and tracked, the inverse gate T^\dagger (as the output should *deterministically* be $T|+\rangle$ regardless of the choice for G) is applied and we measure the output qubit in the X -basis. In the absence of circuit errors, the X -basis measurement should always return $|0\rangle$, indicating that the circuit dynamically applies the S -correction and the output is always a T -rotation. Simulations and experiments with the QE interface is illustrated in Figure 17, again using 8192 instances with the SE omitted from the plot. The requirement for us to *undo* the initial gates to confirm the circuit introduces interesting behaviour related to Pauli tracking [34] that is highly relevant for large scale operations of a quantum computer.

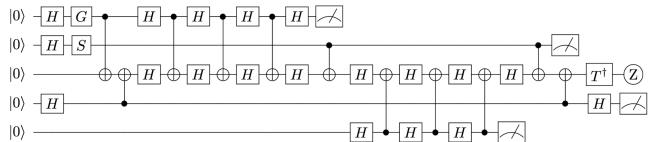


Figure 16: **Implementation of the deterministic T -gate in the QE chip.** The gate G can be chosen to be either T or T^\dagger and the circuit will output the same. SWAP operations are again needed due to the QE architecture, at which point the four measurements are either in the basis $Z_1X_2X_4Z_5$ or $X_1Z_2Z_4X_5$, depending on the initial choice for G . The output qubit is rotated by HT^\dagger and measured, the result should always be $|0\rangle$.

Looking at both the simulation and experimental results, we observe the correct answer with a probability much less than one. This is not only caused by experimental noise. In Figure 18 we illustrate the results for an ideal application of the circuit (again performed within the QE interface). Even in ideal circumstances, the correct result is only observed (after Pauli correction) 75% of the time. The other 25% is where the wrong answer is reported and X -corrections are required due to the teleportation operations. This is because the T^\dagger -gate used to invert the circuit for verification does not commute with this corrective bit-flip gate and the QE chip does

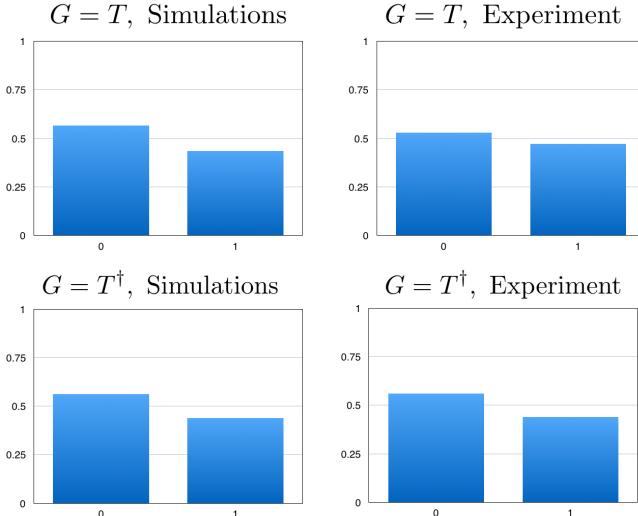


Figure 17: **Simulation and Experimental results for $G = \{T, T^\dagger\}$.** For both simulations and experiments there is only a slightly higher probability of measuring the expected result ($|0\rangle$), again quantum errors for a large circuit in the QE chip is likely to blame. However, as explained in the main text, this circuit only has a maximum probability of success of 0.75% in the ideal case.

Measurement Basis	Results	Corrections
$XZZX(ZXXZ)$	(0,0,0,0)	I (I)
	(1,0,0,0)	Z (X)
	(0,1,0,0)	X (Z)
	(1,1,0,0)	ZX (ZX)
	(0,0,0,1)	Z (X)
	(1,0,0,1)	I (I)
	(0,1,0,1)	ZX (ZX)
	(1,1,0,1)	X (Z)
	(0,0,1,0)	X (Z)
	(1,0,1,0)	XZ (XZ)
	(0,1,1,0)	I (I)
	(1,1,1,0)	Z (X)
	(0,0,1,1)	XZ (XZ)
	(1,0,1,1)	X (Z)
	(0,1,1,1)	Z (X)
	(1,1,1,1)	I

TABLE I: **Pauli corrections for each of the four measurements in the deterministic T -gate.** For each of the sixteen possible measurement results in Figure 16, an appropriate Pauli correction to the output is needed. This correction needs to be *known* before subsequent gates are applied (as they may need to be altered).

not allow us to do *dynamic feedforward*, i.e. change circuits based upon classical measurement result obtained earlier.

In a real operating quantum computer, the result of the four teleportation measurements (particularly the Z-measurements that induce X-corrections) need to be known *before* the application of the next gate. In this case, the second T^\dagger -gate. If an X-correction is present,

the fact that $TX = XT^\dagger$ implies that we would need to interchange a desired T^\dagger gate with a T and visa versa if a bit-flip correction is present on the input. This bit-flip correction may come from circuits such as the deterministic T -gate, but they can also come from other sources such as the error-correction underlying the circuit [4] or corrections coming from the tracking of information from a topological quantum circuit [35].

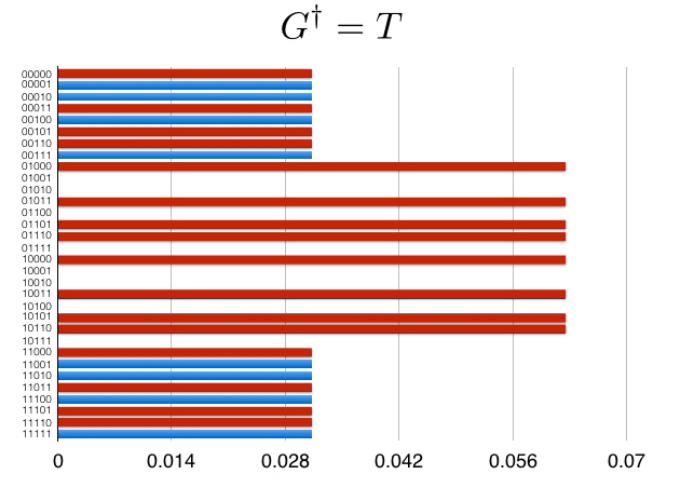
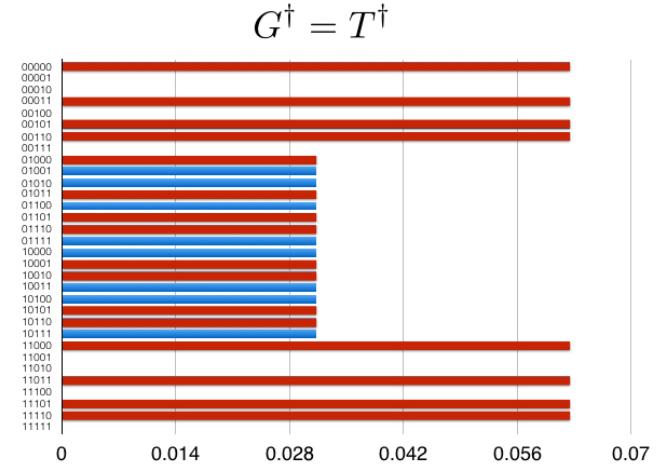


Figure 18: **Output distribution for an ideal application of the deterministic T -gate.** We show the output distribution for an ideal application of the deterministic T -gate for $G = T$. Because Pauli X-corrections arising from the teleportation circuits do not commute with the T^\dagger gate used to invert the circuit and confirm output, the success probability has a maximum of 75%. The red bars show the binary outputs that, when corrected, are used to infer a $|0\rangle$ state output. If we change the T^\dagger gate used at the end of the circuit to T , the probabilities invert, since now the output will be wrong when *no* X-correction from the teleportation circuit is needed.

In Figure 18 we can reverse the distribution of probabilities by changing the gate to we use to invert the original T -gate to a from T^\dagger to T . In this case, if X -

corrections are not required the inverse gate is wrong and the output does not go back to $|0\rangle$. In Figure 18 we illustrate all 32 possible outputs where the red are results that after appropriate Pauli corrections and tracking, result in the output measuring $|0\rangle$. The basis states with approximately 3% probability of being observed have X -corrections from the teleportation circuits that interfere with the function of the final HT^\dagger gate needed to invert the circuit. In a circuit that would be *dynamically* changed dependent on measurement results, this would not occur and the output probability of $|0\rangle$ in the circuit would be 100%.

The results of this experiment directly demonstrate the notion of why T -depth is an important concept [33], the fact that certain results need to be known which prevents us from building all circuits with a T -depth of one (even though from a purely circuit perspective, this should look possible [7]). If dynamic circuit changes were possible within the QE interface, we could demonstrate a fully deterministic T -gate.

VI. DISCUSSION

In all four experiments we are simply looking at the output of the IBM chip rather than examining in detail the error behaviour caused by noise in the chip, hence we have not included any significant analysis of the error properties of each qubit and/or gate (which is available from the QE interface for each run). Analysing the detailed output from each experiment against the error data characterised for the QE chip would be interesting further work to try and refine simulation models to more accurately model how the actual device would behave given the input circuit and error characteristics of the chip.

Even without performing rigorous error analysis on the output, in all four experiments we do see the expected results, with some experiments more susceptible to noise than others. The simulation feature in the QE interface also shows variability depending on the experiment we conducted. Out of the four experimental results, only the error correction Rabi experiment, showed significant deviation between the simulations and experiment. Each of the four QE experiments allowed us to investigate the subtleties of implementing an actual quantum circuit on

viable hardware and therefore required us to focus on details that were important to achieving the correct output that is often overlooked in more theoretical analysis. The results obtained for the deterministic T -gate were particularly illustrative as it demonstrated the importance of having a real time, up to date Pauli frame when programming a quantum device (something that is very often overlooked).

VII. CONCLUSIONS

In this work, we performed four separate experiments utilising the IBM QE chip and interface, demonstrating protocols in error correction, quantum arithmetic, quantum graph theory and fault-tolerant circuit design that has not been achievable so far with an active quantum processor. By utilising the cloud interface, these experiments could be specified, tested (in both the ideal case and with simulated errors) and then run to output noisy (but expected) results. Each of these four protocols have direct relevance to quantum error correction, communications, algorithmic design and fault-tolerant computation and the ease of the QE interface makes subtle investigation into small quantum protocols straightforward.

Ideally, this work will help motivate others to make use of the online hardware produced by IBM and encourage other experimental groups to make their devices accessible to other researchers for testing and theoretical development. The five qubit quantum processor already showed significant flexibility to run tests on a large-class of quantum information protocols and increased fidelities and qubit numbers will hopefully spawn new and interesting protocols for small scale quantum computing processors.

VIII. ACKNOWLEDGEMENTS

We acknowledge support from the JSPS grant for challenging exploratory research and the JST ImPACT project. We are extremely grateful to the team at IBM and the IBM Quantum Experience project. This work does not reflect the views or opinions of IBM or any of its employees.

-
- [1] for Quantum Photonics, C. Quantum in the Cloud. URL <https://cnotmz.appspot.com/>.
 - [2] IBM. The Quantum Experience. URL <http://www.research.ibm.com/quantum/>.
 - [3] D. Alsina and J. I. Latorre. Experimental test of Mermin inequalities on a 5-qubit quantum computer. *arxiv:1605.04220* (2016).
 - [4] Fowler, A., Mariantoni, M., Martinis, J. & Cleland, A. Surface codes: Towards practical large-scale quantum computation. *Phys. Rev. A* **86**, 032324 (2012).
 - [5] Draper, T. Addition on a quantum computer. *quant-ph/0008033* (2000).
 - [6] Hein, M., Eisert, J. & Briegel, H. Multi-party entanglement in graph states. *Phys. Rev. A* **69**, 062311 (2004).
 - [7] Paler, A., Polian, I., Nemoto, K. & Devitt, S. A Compiler for Fault-Tolerant High Level Quantum Circuits. *arxiv:1509.02004* (2015).
 - [8] Devitt, S. *et al.* Architectural design for a topological cluster state quantum computer. *New. J. Phys.* **11**, 083032 (2009).

- [9] Jones, N. C. *et al.* A Layered Architecture for Quantum Computing Using Quantum Dots. *Phys. Rev. X* **2**, 031007 (2012).
- [10] Yao, N. *et al.* Scalable Architecture for a Room Temperature Solid-State Quantum Information Processor. *Nature Communications* **3**, 800 (2012).
- [11] Nemoto, K. *et al.* Photonic architecture for scalable quantum information processing in NV-diamond. *arXiv:1309.4277* (2013).
- [12] Monroe, C. *et al.* Large Scale Modular Quantum Computer Architecture with Atomic Memory and Photonic Interconnects. *Phys. Rev. A* **89**, 022317 (2014).
- [13] Ahsan, M., Meter, R. V. & Kim, J. Designing a Million-Qubit Quantum Computer Using Resource Performance Simulator. *arxiv:1512.00796* (2015).
- [14] Lekitsch, B. *et al.* Blueprint for a microwave ion trap quantum computer. *arxiv:1508.00420* (2015).
- [15] Li, Y., Humphreys, P., Mendoza, G. & Benjamin, S. Resource Costs for Fault-Tolerant Linear Optical Quantum Computing. *Phys. Rev. X* **5**, 041007 (2015).
- [16] Hill, C. *et al.* A surface code quantum computer in silicon. *Science Advances* **1**, e1500707 (2015).
- [17] O’Gorman, J., Nickerson, N., Ross, P., Morton, J. & Benjamin, S. A silicon-based surface code quantum computer. *npj Quantum Information* **2**, 16014 (2016).
- [18] Barends, R. *et al.* Logic gates at the surface code threshold: Superconducting qubits poised for fault-tolerant quantum computing. *Nature (London)* **508**, 500–503 (2014).
- [19] Corcoles, A. D. *et al.* Demonstration of a quantum error detection code using a square lattice of four superconducting qubits. *Nat Commun* **6** (2015). URL <http://dx.doi.org/10.1038/ncomms7979>.
- [20] Brown, K., Kim, J. & Munro, C. Co-Designing a Scalable Quantum Computer with Trapped Atomic Ions. *arxiv:1602.02840* (2016).
- [21] Dolde, F. *et al.* Room-temperature entanglement between single defect spins in diamond. *Nat Phys* **9**, 139–143 (2013). URL <http://dx.doi.org/10.1038/nphys2545>.
- [22] Dehollain, J. P. *et al.* Bell’s inequality violation with spins in silicon. *Nat Nano* **11**, 242–246 (2016). URL <http://dx.doi.org/10.1038/nano.2015.262>.
- [23] Nielsen, M. & Chuang, I. *Quantum Computation and Information* (Cambridge University Press, 2000), second edn.
- [24] Ross, N. & Selinger, P. Optimal ancilla-free Clifford+T approximation of z-rotations. *arXiv:1403.2975* (2014).
- [25] Gosset, D., Kliuchnikov, V., Mosca, M. & Russo, V. An algorithm for the T-count. *Quant. Inf. Comp.* **14**, 1277–1301 (2014).
- [26] Gay, S. Quantum Programming Languages. *Mathematical Structures in Computer Science* **16**, 581–600 (2006).
- [27] Wecker, D. & Svore, K. LIQUi—*λ*: A Software Design Architecture and Domain-Specific Language for Quantum Computing. *arXiv:1402.4467* (2014).
- [28] Green, A., Lumsdaine, P., Ross, N., Selinger, P. & Valiron, B. Quipper: A Scalable Quantum Programming Language. *ACM SIGPLAN Notices* **48**, 333–342 (2013).
- [29] Wecker, D., Bauer, B., Clark, B. K., Hastings, M. B. & Troyer, M. Gate-count estimates for performing quantum chemistry on small quantum computers. *Physical Review A* **90**, 022305– (2014). URL <http://link.aps.org/doi/10.1103/PhysRevA.90.022305>.
- [30] Devitt, S., Stephens, A., Munro, W. & Nemoto, K. Requirements for fault-tolerant factoring on an atom-optics quantum computer. *Nature Communications* **4**, 2524 (2013).
- [31] Paler, A., Devitt, S. & Fowler, A. Synthesis of Arbitrary Quantum Circuits to Topological Assembly. *arxiv:1604.08621* (2016).
- [32] Bravyi, S. & Kitaev, A. Universal Quantum Computation with ideal Clifford gates and noisy ancillas. *Phys. Rev. A* **71**, 022316 (2005).
- [33] Fowler, A. Time Optimal quantum computation. *arxiv:1210.4626* (2012).
- [34] Paler, A., Devitt, S., Nemoto, K. & Polian, I. Software Pauli Tracking for Quantum Computation. *Design, Automation and Test In Europe Conference and Exhibition (DATE’2014)* (2014).
- [35] Paler, A., Devitt, S. J., Nemoto, K. & Polian, I. Mapping of topological quantum circuits to physical hardware. *Scientific reports* **4** (2014).