Unconventional Monolithic Electronics in a Conventional Silicon Photonics Platform

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***Abstract*— To enrich state-of-the-art optical chips with electronic functionalities, we present the integration of unconventional transistors and circuits in a standard silicon photonics platform, with no modifications to the conventional fabrication process employed by photonic foundries. This approach allows us to include on-chip electronic building blocks to support the optical functionality at zero additional cost while maintaining optical excellence and foundry interoperability. To showcase the benefits of monolithic electronics, we integrated a transconductance amplifier and an analog multiplexer for sequential readout of 16 photodetectors, distributed in a large-scale architecture of Mach–Zehnder interferometers (MZIs). The circuits, successfully validated in optical experiments, allow the reduction of electrical input-output lines of a photonic chip without any optical penalty, thus targeting one of the main bottlenecks that limit further scaling of photonic circuits.**

***Index Terms*— CMOS electronics, electronic-photonic codesign, monolithic integration silicon photonics.**

I. Introduction

THE success of silicon-integrated photonics relies both on the excellent optical properties of silicon and on the opportunity to leverage the microelectronic manufacturing processes to fabricate optical chips of high complexity, integrating hundreds of photonic devices. The choice of silicon as an optical material is attractive because it is transparent to the near-infrared telecom wavelengths and it allows the miniaturization of waveguides (WGs) by exploiting the refractive index difference with silicon dioxide. The possibility of sharing the microelectronic production technologies and facilities has thus stimulated the investigation of monolithic electronic-photonic chips, where the two technologies are merged to obtain high-performance electro-optical systems. When the electronic functionalities needed in a photonic chip are prevailing, as, for example, in high-speed transceivers for optical communications operating at hundreds of Gbit/s, the option of integrating the photonic devices into a standard microelectronic stack has been successfully pursued [1], [2], [3], [4].

In many other cases, such as optical computers, neuromorphic systems, and quantum photonic processors [5], [6], [7], photonic functionalities prevail and excellent optical performance is required. Given the relatively large size of photonic circuits, specialized photonic foundries simplified the stack of standard microelectronic processes, which is no longer necessary, by selecting only a few essential steps to reduce costs while allowing for low-loss optical devices. The electronic functions required to operate the photonic chip are in these cases provided by external electronic circuits connected to the photonic chip. The role of the electronics is to set and control the working points of photonic devices and counteract their drifts in a closed-loop fashion [8], [9], [10], [11] by collecting signals from integrated photodetectors to properly drive on-chip actuators. However, the number of electrical connections between the photonic chip and the electronics constitutes one of the limitations to further extend the optical complexity above a few hundred devices, thus seriously limiting the development of large-scale architectures [12], [13].

We want to overcome this limitation by integrating electronic devices and circuits into standard photonic technologies, enabling the control of a large number of optical devices with few external electrical connections. However, the structure of conventional transistors needs to be greatly modified to tackle the lack of self-aligning gate process and vertical control of diffusions of the standard silicon-on-insulator (SOI) stack of photonic platforms. The design of vertical transistors with good channel modulation and low threshold voltage is also made difficult by the separation (usually 700 nm of oxide) between the metal layers used for electrical routing and the silicon, needed to ensure minimal transmission losses in the WGs. Indeed, the optoelectronic devices implemented in this technology are usually simple resistors or lateral p-n junctions [14], [15], [16], [17].

Despite these limitations, it is still extremely desirable to realize electronic circuits without changing in any way the available fabrication processes of the photonic foundries. This zero-change approach allows to maintain high optical

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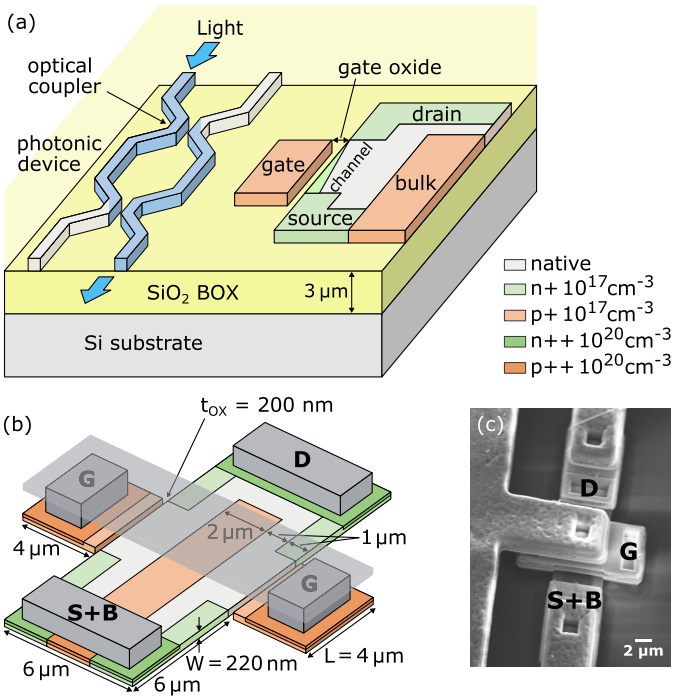

Fig. 1. (a) Schematic view (not to scale) of the typical silicon photonics technological process stack, showing a photonic device on the left and a section of the proposed MOSFET on the right. (b) 3-D quoted view of the nMOS transistor elementary cell and (c) its SEM photograph.

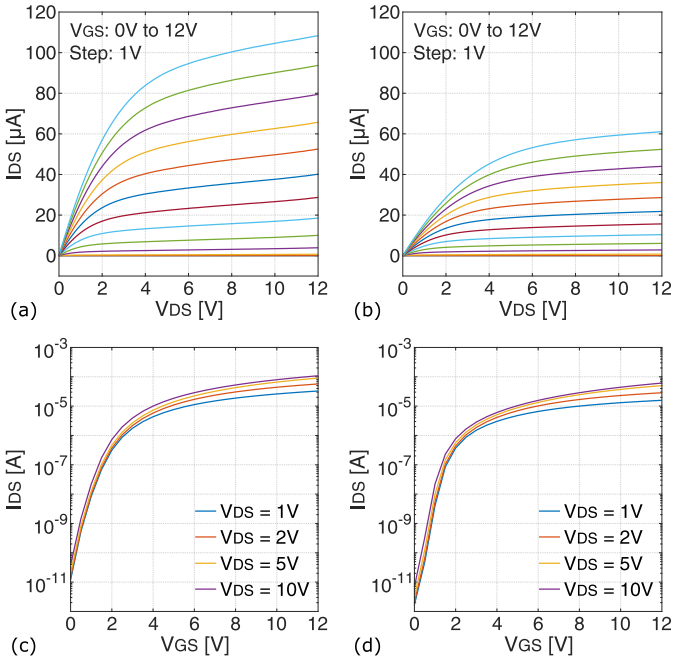

Fig. 2. Experimental characteristic curves of the designed (a) nMOS, (b) pMOS, and (c) and (d) corresponding transcharacteristic curves at different drain-source voltages.

quality, low cost, and complete interoperability among different photonic foundries, even in multiproject wafer runs. Starting from elementary transistors, this article describes the implementation of several electronic circuits of increasing complexity, up to the integration of electronic multiplexers and operational amplifiers, with the future perspective of complete autonomy of the chip from external electronics as the result of a full electronic-photonic co-design.

II. Integrated Transistors

A. CMOS Side-Gate Transistors

We have designed lateral metal-oxide-semiconductor field-effect transistors (MOSFETs) to overcome the technological limits of the photonic fabrication stack. The 3-D device structure implemented in a standard SOI photonic process (Advanced Micro Foundry, Singapore [18]) is shown in Fig. 1(a). The substrate of nMOSFETS is implemented with the 220 nm-thick native silicon layer, lightly p-doped (nominally 10^{15} cm^{-3}). By opening a vertical trench in this region, a lateral gate is then created as close as possible to the substrate (t_{ox} = 200 nm in our case), p-doped (10^{17} cm^{-3}) to improve its conductivity. The 220 nm thickness of the SOI layer thus defines the channel width W. Low substrate doping and proximity of the lateral gate ensure a threshold voltage between 1.5 and 2.5 V. Finally, the transistor body is locally n-doped (10^{17} cm^{-3}) to create the Drain (D) and Source (S) contacts, while a p-type diffusion defines the bulk (B). Numerical simulations have been used to optimize the channel length L of 4 μm and achieve low leakage currents in the OFF state without significantly decreasing the device conductivity. The final MOSFET structure is a symmetric elementary cell obtained by mirroring the described structure along the D–S axis [Fig. 1(b)]: the bulk diffusion is shared between the two halves, the source and drain contacts are combined and the two side gates are connected with a common metal electrode. In order to design devices with the correct aspect ratio, multiple elementary cells can then be connected in series or parallel.

By changing the doping type that constitutes the transistor diffusions, the pMOSFET can be implemented while keeping the same geometry described so far. Since the doping of the native silicon layer cannot be controlled, the device substrate is the only unmodified region. However, the (mostly positive) electronic charges in the SiO_2 cladding and at the Si/SiO_2 interface cause depletion of free carriers in the p-type silicon core, because of its thin structure and high surface-to-volume ratio [19], [20]. This results in a very low conductivity of the native SOI layer that behaves like an almost intrinsic semiconductor and can thus be employed as the substrate for both nMOSFETS and pMOSFETs. Standard electronic fully depleted SOI (FDSOI) technologies indeed exploit the same effect [21]. By providing a bias voltage to the chip substrate, which behaves as a common back-gate, the conductivity of the native silicon can be further controlled. $V_{sub} = -10$ V was selected in our case after preliminary measurements on the technology [20] and numerical simulations to guarantee good performance and low leakage currents to both n- and pMOSFETs. This value is used in the rest of the article.

The manufactured transistors, shown in a scanning electron microscope (SEM) image in Fig. 1(c), have been systematically characterized at room temperature. The measured characteristic and transcharacteristic curves for the nMOS and pMOS devices are shown in Fig. 2(a)–(d), respectively. The measured parameters of the elementary-cell transistors are reported in Table I. As will be seen in the next paragraphs, these values are suitable for realizing fully operational electronic circuits

TABLE I
MEASURED PARAMETERS OF THE ELEMENTARY-CELL MOSFETS

	nMOS	pMOS
Threshold voltage [V]	2.45	1.8
Gain factor ($\mu C_{ox} W/L$) [μA/V^2]	4	2
Early voltage [V]	35	55
Inverse subthreshold slope [mV/dec]	350	250

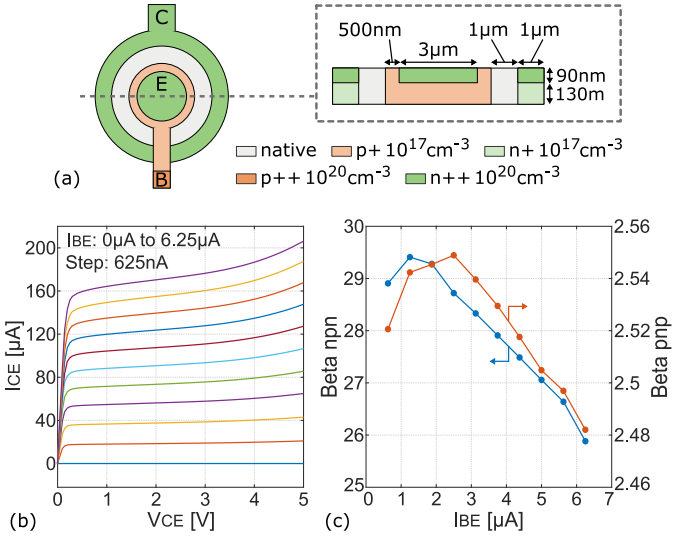

Fig. 3. (a) Schematic view and cross section of the designed npn bipolar transistor, (b) its experimental characteristic curves, and (c) corresponding current gain factor β as a function of the base current. The figure also shows the β of a pnp device.

with the required performance. The proposed approach is technology-transparent, since the transistors are manufactured without altering the fabrication process or the design rules of the photonic stack. The only important parameter that a photonic foundry should guarantee to fabricate the transistors is the minimum distance t_{ox} between source and gate, which we set to 200 nm. This value is slightly larger than the minimum feature size needed to design directional couplers, gratings, and other key optical building blocks, and it is thus guaranteed by most silicon photonics foundries. Technologies allowing for smaller t_{ox} would result in better transistors, with a lower threshold voltage.

B. Bipolar Transistors

The SOI stack, suitable for lateral devices, has also given the possibility of integrating circular bipolar junction transistors (BJTs), shown in Fig. 3(a) in the npn version. The current gain of the transistor has been maximized by setting the doping of the emitter region to 10^{20} cm^{-3}, much higher than the base one of 10^{17} cm^{-3}, and the length of the base region has been set to the minimum allowed by the technology. At the collector side, a 1 μm-wide region of native silicon has been used to increase the Early voltage of the transistor and the breakdown voltage of the base-emitter junction, thus allowing safe operations at high voltages. The pnp device can be obtained simply by inverting the doping species of the diffusion regions while keeping the same geometry.

Fig. 3(b) shows the measured characteristic curves of the npn transistor. From the measurement, an Early voltage of 33 V is derived. Fig. 3(c) reports the current gain β of the

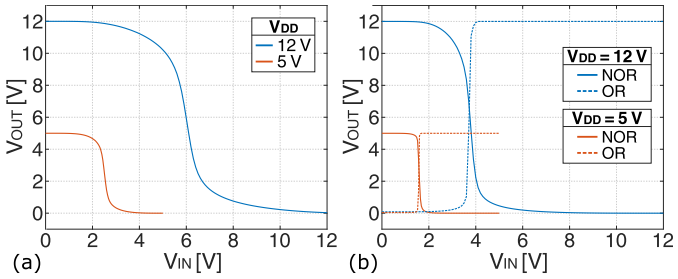

Fig. 4. Experimental input-output characteristic curves of (a) NOT and (b) OR/NOR gates, at both 5 and 12 V power supply. The OR/NOR curves were obtained by driving both inputs with the same signal.

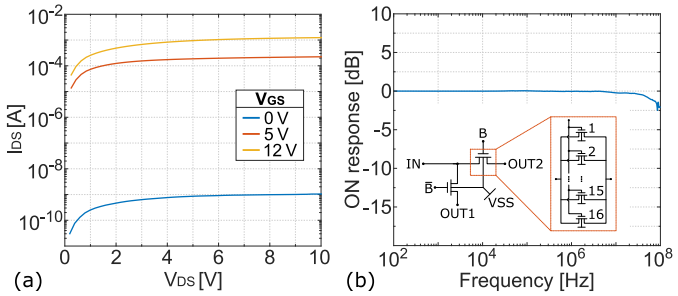

Fig. 5. (a) Measured static on and off currents of the SPDT switch as a function of the drain-source voltage. (b) Signal bandwidth of the device in the on condition. The circuit structure is shown in the inset of the figure.

device as a function of the base current. A β of around 30 is obtained, about one order of magnitude higher than what is reported in [22], with an expected slight degradation at large base currents due to the Kirk effect [23]. As the geometry and doping levels of the pnp and npn transistors are the same, the former shows a β about nine times smaller than the latter due to the lower mobility (about a factor 3) of holes with respect to electrons.

III. CMOS Logic Gates and Analog Switches

Analog and digital building blocks have been created with the designed MOS transistors to support the operation of photonic devices and circuits. CMOS logic, employing both n- and pMOSFETs simultaneously, has been chosen to implement the digital gates and profit from its intrinsic low power consumption. Fig. 4(a) shows the measured input-output characteristic curves of the designed inverter. The circuit works well with a power supply of both 5 and 12 V. Similar to this, Fig. 4(b) reports the characteristic curves of the two-input NOR gate, where both inputs have been driven with the same signal. The NOR and the inverter can also be easily coupled to create the OR gate, providing maximum flexibility in the design of digital circuits. The NOR and OR outputs are compared in Fig. 4(b) to highlight the steeper transition region of the latter. Even in this unusual technology, the digital gates thus maintain their regenerative property and can be cascaded without penalties to implement the desired logic function. The static power dissipation due to leakage currents is 2 nW for the NOT and 10 nW for the OR/NOR gate, with a supply voltage of 12 V.

In view of connecting sensors/actuators of the photonic layer to the readout/driving electronics, analog switches

have also been designed. By combining two pass transistors controlled with complementary gate voltages, a single-pole double-throw (SPDT) analog switch has been implemented. The switch is made only of nMOSFETs, where the bulk has been separated from the source to create a bidirectional device. Sixteen transistors were connected in parallel to lower the ON-resistance of each switch. The device current at $V_{GS} = 0$, 5, and 12 V is shown in Fig. 5(a). The graph demonstrates the good isolation of the switch in the OFF state, with a leakage below 5 nA even for high V_{DS} voltages, and the strong conductivity in the on condition, with a maximum current around 1 mA. The slope of the curves in the figure around $V_{DS} = 0$ V can be used to calculate the ON and OFF resistances of the device, normally operated at low drain-source voltages. With $V_{GS} = 12$ V, an on-resistance of 1.8 kΩ is observed. The conductivity of the switch can be increased by connecting more transistors in parallel, if a lower value is required. Instead, with $V_{GS} = 0$ V, the OFF resistance results to be roughly 2 GΩ, demonstrating that the device correctly connects and disconnects the input to the outputs depending on the digital command. Fig. 5(b) reports the signal bandwidth of the switch, showing a −3 dB cutoff frequency of about 100 MHz. The device is thus capable of carrying signals from/to sensors or actuators on the photonic chip, which typically have frequencies between dc and a few tens of MHz. The circuit diagram is shown in the inset of the figure.

IV. Integrated Multiplexer for Sequential Monitoring of Photonic Devices

To validate the functionality of monolithic electronics in controlling photonic devices, we designed an analog multiplexer (MUX), that allows us to sequentially interrogate an array of integrated photodiodes (PDs). The main benefit of an on-chip MUX is the reduction of the number of electrical input-output (I/O) lines, which represents a limiting factor for scaling up the complexity of photonic circuits. The use of an N-to-1 MUX logarithmically scales the number of required connections from N_{SENS} detectors down to

$$N_{MUX} = \log_2(N_{SENS}) + 4. \quad (1)$$

Since one output port, two power supplies (V_{DD}, V_{SS}), and one reference voltage (GND) are needed in addition to the digital address bits, the MUX is convenient when more than eight detectors are used. The advantage becomes more evident as the number of sensors increases, since doubling the device channels requires only adding a digital bit. On the other hand, by employing a MUX the working point of each optical element cannot be monitored simultaneously, but rather in sequence [24] at a frequency determined by the sampling rate of the system divided by the number of multiplexed channels. As a result, the ratio between the maximum switching frequency of the MUX and the minimum readout rate given by the application sets the maximum number of devices that can be interrogated in series. Temperature drifts are, for instance, characterized by a millisecond timescale. Therefore, a readout rate of few kHz is typically enough to mitigate their effect, allowing us to multiplex many detectors without penalties.

Fig. 6(a) shows the schematic of an integrated 16-to-1 analog MUX for the readout of on-chip PDs. The device is

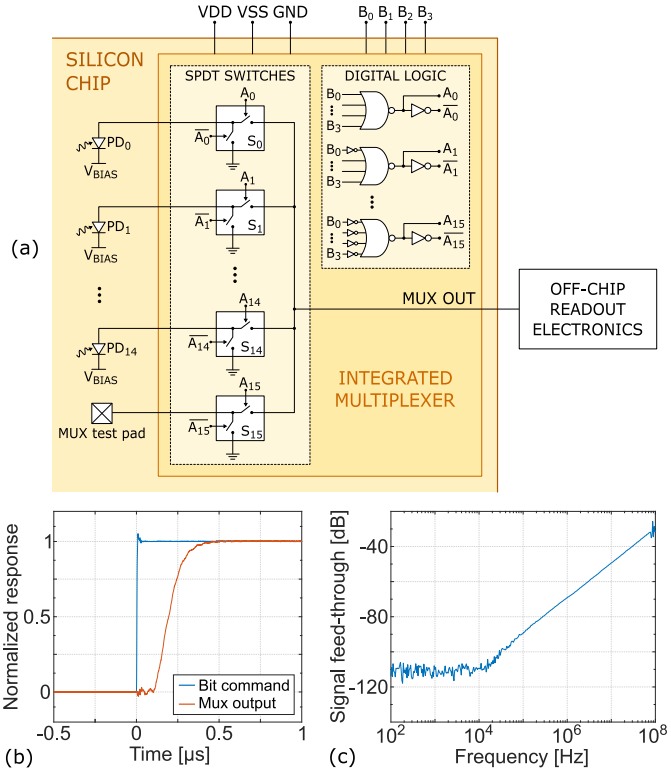

Fig. 6. (a) Schematic view of the 16-to-1 electronic MUX connected to on-chip PDs. (b) Response of the MUX when changing the digital bits, resulting in a maximum switching frequency of 2 MHz. (c) Measured signal feed-through of the MUX, obtained by injecting an electrical signal to the test pad while leaving the corresponding switch open.

connected to a single external transimpedance amplifier (TIA) and it uses the SPDT switches of the previous paragraph to connect one PD to the virtual ground of the TIA and the others to ground. This allows one to keep all the detectors always biased at the same operating voltage, reducing the switching time of the circuit. CMOS digital gates with a NOR-based logic drive the correct switches according to the input digital word. The multiplexer uses 596 nMOSFETs and 84 pMOSFETs, for an overall footprint of 250 × 1200 μm, which corresponds to less than 0.0188 mm^2 per channel. The measured static power consumption of the circuit is around 200 nW with a supply voltage of 12 V. The measurement in Fig. 6(b) shows the settling time of the MUX (around 500 ns, red curve) when the configuration of the digital bits is changed (blue curve), corresponding to a maximum switching frequency of about 2 MHz. Assuming a target readout rate of 10 kHz per PD, the MUX thus allows us to perform sequential readout of up to 200 PDs by using just 12 electrical lines, a dramatic improvement with respect to the case of parallel detection. By using a test pad connected to one of the MUX channels, we also measured the signal feed-through of the circuit. Fig. 6(c) shows the result, obtained by measuring the MUX output when injecting a signal to the test input while leaving the corresponding switch open. The measurement shows negligible spurious coupling of signals up to 10 MHz, demonstrating that no electrical penalty is introduced in the readout of the sensors.

To validate the use of the MUX in an optical experiment, the circuit has been integrated into a large-scale photonic system

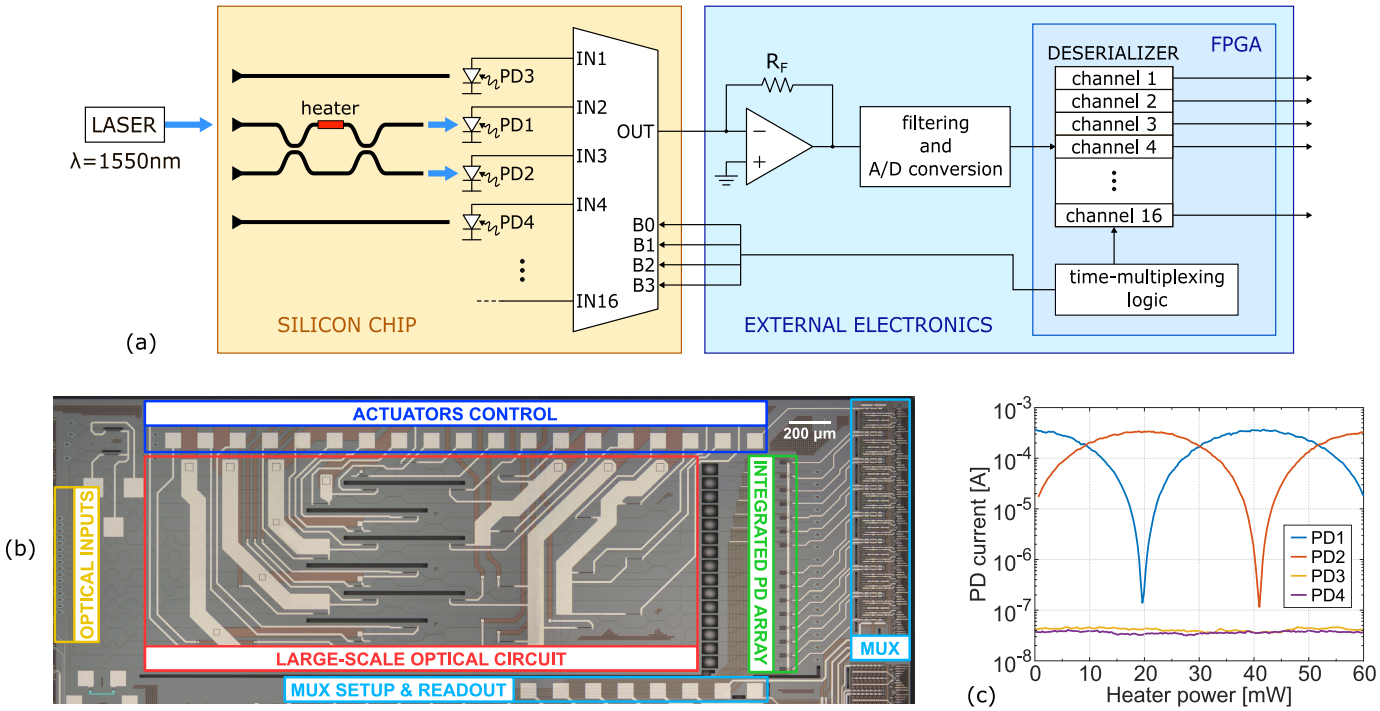

Fig. 7. (a) Schematic view of the complete electro-optical system, including the photonic chip and the readout electronics. (b) Microscope photograph of the fabricated silicon chip. (c) Photocurrents measured when sweeping the heater driving voltage and recording the readout of the on-chip PDs, multiplexed in time by using the designed MUX.

made of 110 building blocks. A subsection of the chip has then been employed to test the MUX, by sequentially interrogating an array of integrated Germanium PDs, available from the foundry process design kit [18]. As reported in Fig. 7(a), four detectors have been used. The first two (PD1 and PD2) have been coupled to the output ports of a balanced Mach–Zehnder interferometer (MZI), that implements a thermally tuneable 2×2 optical switch, while the others (PD3 and PD4) have been coupled to two reference WGs without light. A microscope photograph of the full chip is shown in Fig. 7(b), highlighting the small footprint of the electronics with respect to the photonic part. A custom electronic system has been used to automatically set the MUX digital bits and read, digitize, and deserialize its output to recover the information of the four sensors [25]. To perform the optical experiment, a laser beam at 1550 nm wavelength has been coupled to one of the input ports of the MZI. The PDs have been monitored through the MUX while increasing the electrical power dissipated in the thermal phase shifter (heater) of the MZI. The results in Fig. 7(c) show that, as the relative phase shift between the MZI arms increases (heater voltage swept from 0 V to 5 V, heater power up to 60 mW), the signals detected by PD1 and PD2 provide complementary information about the MZI transfer function and periodically change in agreement with the expected power switch at the MZI output ports. A dynamic range of more than three decades is measured in the PD currents, resulting from the device optical extinction ratio of more than 30 dB (the nominal PD responsivity is 0.9 A/W). In contrast, the current measured by the reference PD3 and PD4, coupled to WGs with no light, remains constant to a value of about 50 nA, which is indeed the nominal value of the sensor's dark current. The local heating power of the actuators does not affect the behavior of the electronic circuits, as the transistors are far from the heaters and thermally insulated by means of oxide trenches. The measurement thus demonstrates that the sequential readout performed by the MUX does not degrade the photodetectors readout and does not produce crosstalk, showing that it can be effectively used to monitor the state of large-scale photonic chips.

V. On-Chip Analog Amplifier

To further extend the opportunity given by the integration of electronic devices and circuits into state-of-the-art photonic platforms, we also designed a full operational transconductance amplifier (OTA), which represents the fundamental building block of many analog electronic circuits. This would allow us to integrate, for example, the TIA for reading the PDs into the photonic chip when a low-impedance voltage signal is preferred with respect to a current in the connection toward the external electronics. An OTA is also a building block of most analog-to-digital converters (ADCs) [26] and it could be used to integrate a simple Sigma–Delta ADC and directly digitize on-chip the readout of integrated detectors.

Fig. 8(a) and (b) show the schematic and microscope photograph of the two-stage OTA: a transdiode current generator (10 μA) biases the input nMOSFETs pair and the active load. A second Miller-compensated stage provides further amplification and the desired single-pole frequency response. The circuit has a supply voltage of 5 V and a power consumption of 400 μW. The measured transfer function of the OTA, shown in Fig. 8(c), demonstrates a gain-bandwidth product of more than 1 MHz and about 40° phase margin, ensuring stability in the applications where on-chip analog processing is required. This is also confirmed by the stable frequency response of the amplifier connected in unity-gain buffer configuration, shown in the same figure. The results

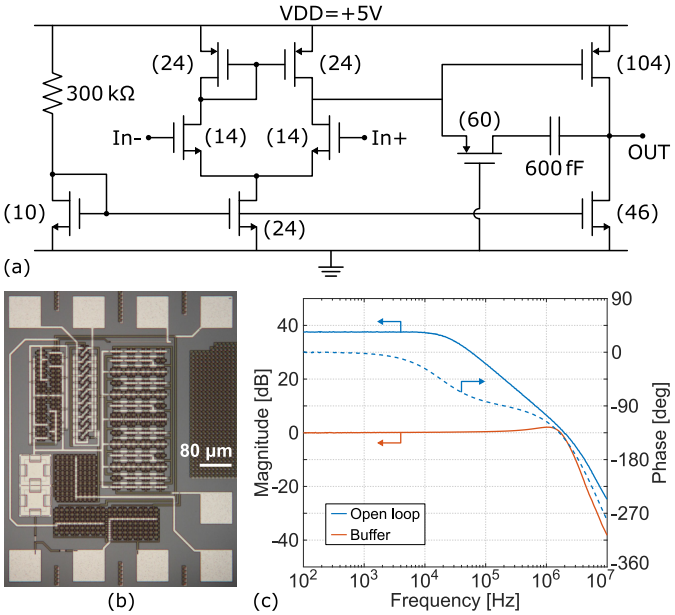

Fig. 8. (a) Schematic of the OTA (reporting the number of MOSFETs in parallel for each transistor), (b) its microscope photograph, and (c) its measured transfer function, in open-loop and buffer configuration.

thus validate the possibility of integrating analog processors directly on the photonic chip.

VI. Conclusion

We demonstrated that transistors and active electronic circuits can be monolithically integrated on an optical chip, without changing the standard fabrication steps used to manufacture state-of-the-art photonic devices. The electronic layer adds no penalty to the optical performance, since it does not affect the fabrication of WGs or photonic devices. The electronics can therefore be directly integrated into optical architectures of any complexity allowed by the technology to create building blocks that support the photonic functionality. As the devices are compliant with the foundry design rules, we have not found any experimental evidence of malfunctioning or substantial misbehavior on roughly 1000 transistors that we operated.

The realization of a monolithic analog amplifier and a multiplexer for sequential readout of sensors are examples of circuits that can complement the optical layer, allowing us to manage future scalable systems integrating thousands of photonic components. Note that the proposed electronics addresses the low-speed devices needed to set and stabilize the photonic functionality, and it does not interfere with high-frequency components, like modulators or receivers, that can still be seamlessly operated by means of external high-speed circuits. This approach thus perfectly adapts also to research and development of innovative silicon photonics platforms, enabling further improvements in the field of solid-state optics.

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