LASER
& PHOTONICS
REVIEWS

Supporting Information

for *Laser Photonics Rev.*, DOI 10.1002/lpor.202300124

Time-Multiplexed Control of Programmable Silicon Photonic Circuits Enabled by Monolithic CMOS Electronics

Francesco Zanetto, Fabio Toso, Vittorio Grimaldi, Matteo Petrini, Andres Martinez, Maziyar Milanizadeh, Alessandro Perino, Francesco Morichetti, Andrea Melloni, Giorgio Ferrari and Marco Sampietro*

Supplementary material
Time-multiplexed control of programmable silicon photonic circuits enabled by monolithic CMOS electronics

Francesco Zanetto Fabio Toso Vittorio Grimaldi Matteo Petrini Andres Martinez Maziyar Milanizadeh Alessandro Perino Francesco Morichetti Andrea Melloni Giorgio Ferrari Marco Sampietro*

F. Zanetto, F. Toso, V. Grimaldi, M. Petrini, A. Martinez, M. Milanizadeh, A. Perino, F. Morichetti, A. Melloni, M. Sampietro
Department of Electronics, Information and Bioengineering, Politecnico di Milano, piazza Leonardo da Vinci 32, Milano 20133, Italy
* E-mail: francesco.zanetto@polimi.it

G. Ferrari
Department of Physics, Politecnico di Milano, piazza Leonardo da Vinci 32, Milano 20133, Italy

1 Supplementary section 1: simulations of the nMOS device

The proposed transistors have been simulated with the technology CAD software Sentaurus (Synopsys Inc., Mountain View, USA) to optimize their geometry. Figure 1a shows the top view of the simulated device, reporting all the dimensions and doping levels. The simulations have been repeated varying the channel length L from 2 µm to 5 µm, to compare the behaviour in both the on and off conditions, while all the other parameters have been kept constant. Figure 1b, 1c, 1d, 1e show the resulting characteristic curves for gate-source voltages from $V_{GS} = 0\,\text{V}$ to $V_{GS} = 10\,\text{V}$. The simulation is in good agreement with the experimental measurements, even though surface effects are not considered. As expected, the conductivity of the transistor reduces for longer channel lengths while the Early voltage increases, demonstrating the correct design of the device.
Figure 1f reports the simulated current in the transistor when $V_{GS} = 0\,\text{V}$ and the drain-source voltage is swept from $V_{DS} = 0\,\text{V}$ to $V_{DS} = 10\,\text{V}$. The simulation allows to optimize the transistor channel length to obtain a negligible current in the off condition, a relevant aspect to be considered in particular when designing analog switches. The figure highlights that the shortest L that ensures low leakage currents for all the possible drain-source voltages is $L = 4\,\mu\text{m}$. Longer channel lengths do not show a relevant improvement in the transistor off behaviour and reflect in lower device conductivity in the on condition, therefore $L = 4\,\mu\text{m}$ has been selected and used for the fabricated transistors.

2 Supplementary section 2: electrical characterization of the integrated multiplexer

The electrical characterization of the integrated multiplexer has been performed by wirebonding the photonic chip to a custom interface PCB, in order to easily provide and read all the necessary signals. A test multiplexer, identical to the one employed in the optical measurements but not connected to integrated photodiodes, has been used for the electrical characterization.
The on and off currents of the device have been obtained with a quasi-static measurement performed with a Keithley 4200-SCS semiconductor parameter analyzer equipped with high-resolution monitor units (Figure 2a). To measure the on current, the digital bits of the MUX have been configured to select channel 16. The input voltage of the MUX has been swept from 0 V to 12 V and the current at the output, kept at a constant voltage of 0 V, has been measured with the parameter analyzer. The same operation has been repeated to measure the off current, but in this case the digital bits where configured to select channel 1 of the device, connected to ground. From the two curves, shown in Fig. 2c in the main manuscript (reported here again in Figure 3 for convenience), the on and off resistances of the device

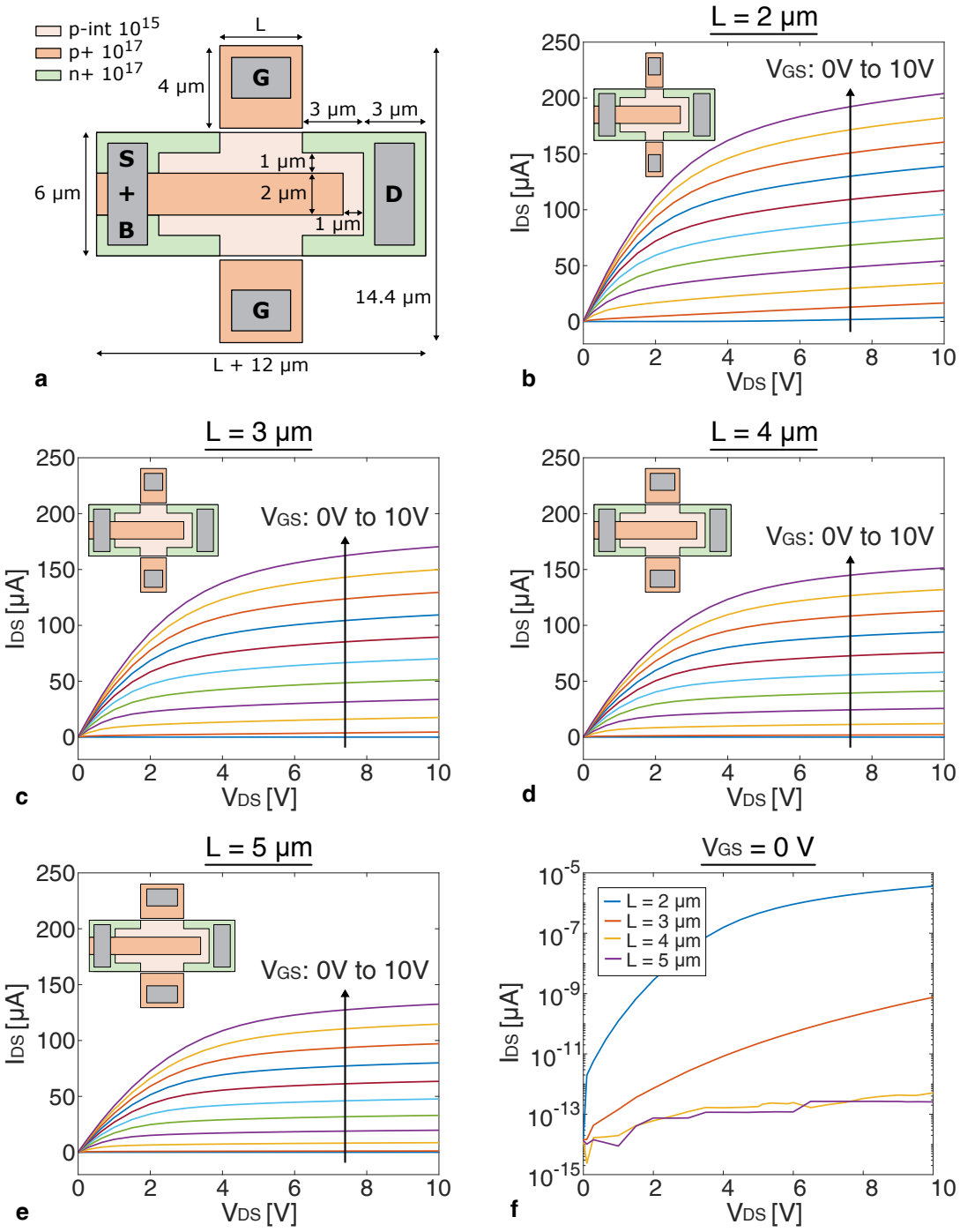

Figure 1: a) Schematic view of the simulated nMOS transistor, reporting dimensions and doping levels of all the regions. b), c), d), e) Simulated characteristic curves of the nMOS transistor as a function of the channel length L, varying from 2 µm to 5 µm. f) Simulated current in the transistor at $V_{GS} = 0$ V for different channel lengths, highlighting that for L larger than 4 µm the leakage current in the off condition becomes negligible.

can be obtained. Since in normal operations the multiplexer is placed between a photodiode, providing a maximum current in the tens of µA range, and the virtual ground of the readout transimpedance amplifier, kept at 0 V, the voltage across the device is always limited to few hundreds of mV. The on and off resistances can be thus computed as the slope of the two curves of Figure 3 for small drain-source voltages, revealing values of 1.8 kΩ and 2 GΩ respectively.

The frequency response measurements have been instead performed with an Agilent E5061B network analyzer. The bandwidth of the MUX has been obtained by injecting a stimulation voltage with a frequency between 100 Hz and 100 MHz to channel 16 and by reading the corresponding signal at the output of the device (Figure 2b). Impedance matching between the instrument input/output ports, the con-

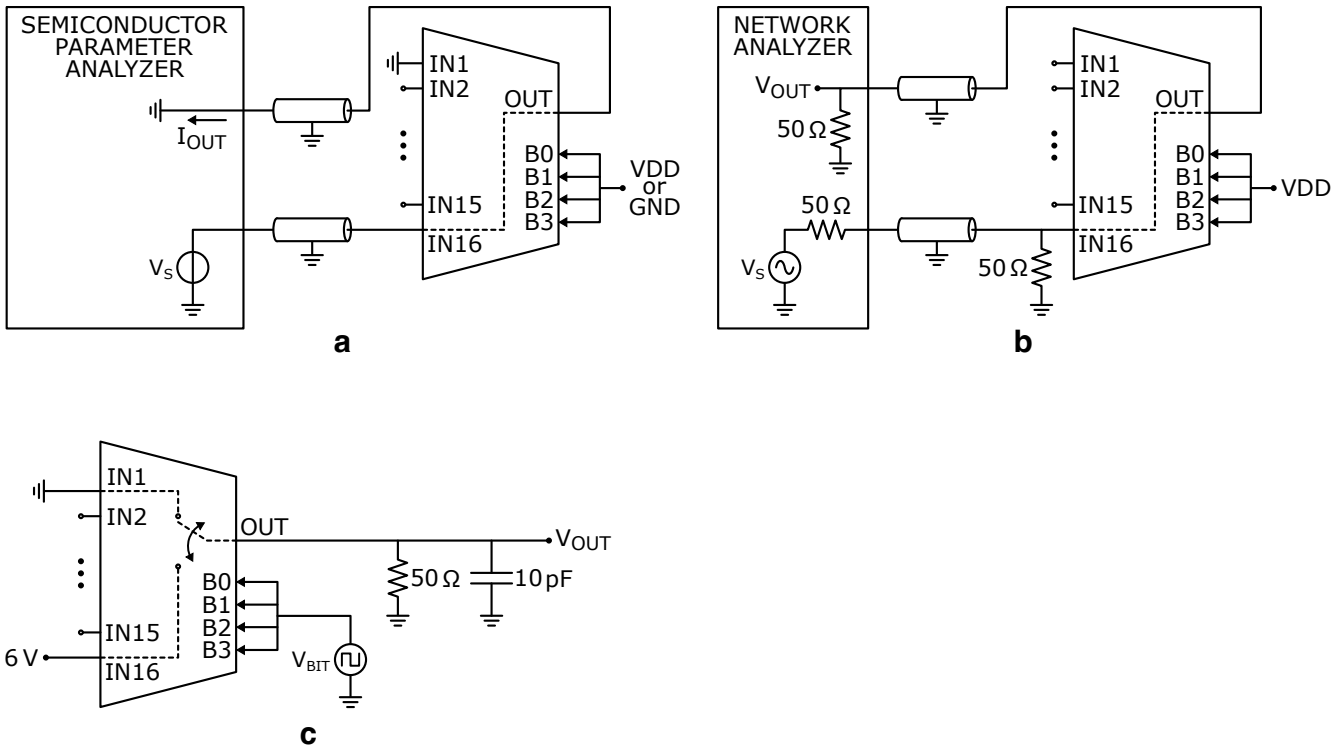

Figure 2: a) Characterization of the static on-off response of the MUX. b) Experimental setup to characterize the device signal bandwidth. c) Characterization of the device switching time.

necting cables and the device-under-test have been ensured with proper terminations. The measured signal bandwidth of the circuit is around 100 MHz, therefore the mux is able to route the signals from the photodetectors or to the actuators on the photonic chip, that are usually characterized by a frequency in the range between DC and few tens of MHz.

Finally, Figure 2c shows the measurement setup used to test the switching speed of the device. Input 1 and 16 of the MUX have been connected to 0 V and 6 V, respectively, and a square wave signal between VDD and GND has then been used to drive the configuration bits, alternatively selecting the two inputs. Changing all the bits at the same time causes a commutation of the longest chain of digital gates in the MUX, therefore the worst case switching time is measured in this way. The output of the MUX has been terminated with a 50 Ω load and acquired with an oscilloscope (Agilent DS09254A), having a 10 pF input capacitance probe. The readout bandwidth of the system is thus set to 300 MHz, much larger than the switching bandwidth of the MUX, and it does not limit the measurement.

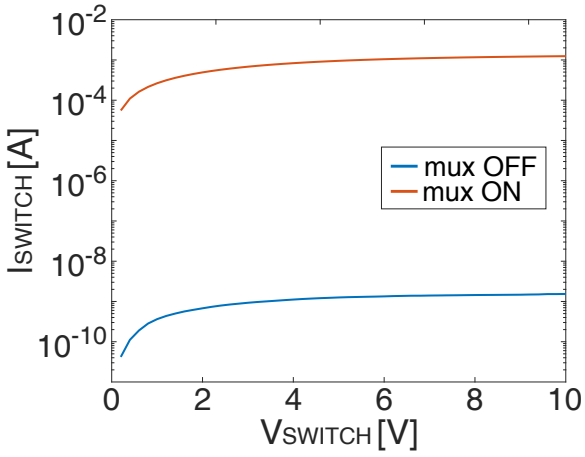

Figure 3: Measured on/off response of the MUX, from which a 1.8 kΩ on resistance and a 2 GΩ off resistance can be computed.

3 Supplementary section 3: digital architecture for time-multiplexed control of photonic circuits

Figure 4 shows the digital architecture implemented in the FPGA to automatically configure and stabilize the functionality of the optical router with a time-multiplexed logic. This mode of operation requires to continuously update the MUX configuration bits to cyclically read the 4 photodiodes along the selected input-output light path. Each time the configuration bits are changed, the anti-aliasing filter on the readout PCB needs to settle in order not to have errors in the readout. Being the bandwidth of the 4th order filter 400 kHz, we set the MUX switching frequency to a safe value of 80 kHz. Therefore, the 4 selected photodiodes are interrogated at an equivalent rate of 20 kSps.
The ADC bit-stream, updated at 960 kSps, contains 12 samples per each photodiode in a single MUX switching period. Consequently, a decimator of a factor 12 is first used to discard the samples taken during the settling of the anti-aliasing filter. The signals of the 4 photodiodes then need to be separated to be processed independently. This is done with a demultiplexer (DEMUX) that sends the data to the correct digital chains depending on the router configuration. The DEMUX is operated at the same 80 kHz rate as the MUX. The demultiplexed data are finally processed in parallel with 15 identical digital chains. Only 4 of them are active at the same time, since only 4 heaters need to be controlled to route light from one input of the MZI mesh to the output. The same control logic that sets the MUX configuration bits also activates the correct processing chains and drives the DEMUX operations.
The average light power measured by each photodiode is obtained by simply low-pass filtering the readout after the DEMUX. Instead, to tune the MZIs and keep them locked in the correct working point, the dithering technique is used. The technique requires to add a small sinusoidal oscillation to the heater DC voltage. This causes the MZI transfer function to vibrate around its bias point, modulating the amplitude of the light at the output. If the oscillation is small enough, the light modulation amplitude is proportional to the first derivative of the MZI transfer function. This information can be effectively used to control each optical switch, since driving the dithering signal to zero by properly setting the heater voltage translates into tuning the MZI in the maximum or minimum of its transfer function. We implemented the control logic as shown in Figure 4.

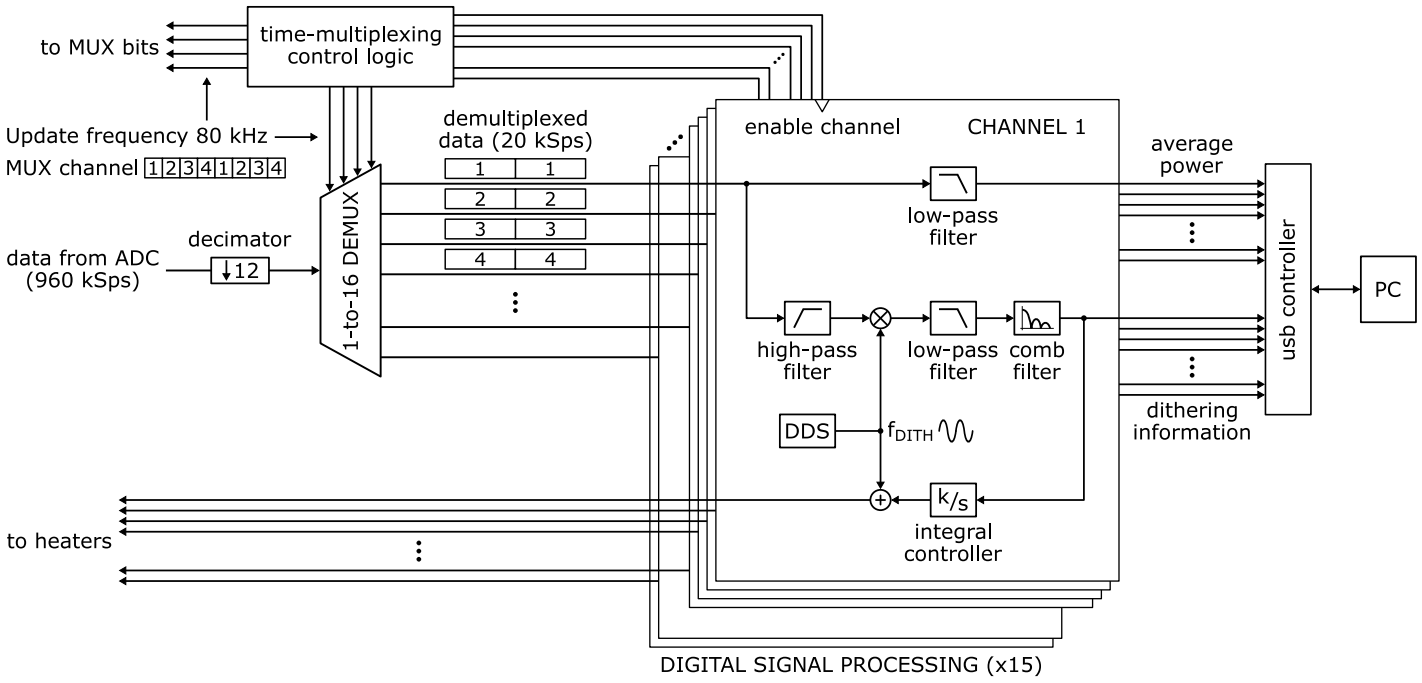

Figure 4: Schematic view of the digital architecture implemented in the FPGA to control the 16-to-1 optical router. The circuit exploits the dithering and the lock-in techniques in combination with integral controllers to stabilize each MZI in the maximum transmission point.

The dithering information is extracted with a digital lock-in architecture. The frequency f_{dith} has been set to 2 kHz, in order not to have aliasing phenomena with the 20 kSps equivalent sampling frequency of the system. To extract the information, a high-pass filter first removes the DC value of the photodiode readout, then a mixer downconverts the dithering signal from f_{DITH} to DC. A low-pass filter, in combination with a comb filter, finally removes the harmonics resulting from the demodulation. The obtained signal is then integrated by an integral controller to automatically drive each heater. In this way, a zero steady-state dithering amplitude is ensured, effectively locking the MZI. By changing the sign of the controller gain, both minimum and maximum transmission points of the MZIs can be targeted. In our case, we set all the controllers to minimize the light reaching each photodiode.

4 Supplementary section 4: optical setup and measurements

The detailed optical setup employed in the measurements on the transmission quality is shown in Figure 5.
The wavelength of a tunable laser source (Ando AQ4321D) has been set to 1550 nm, where the input and output grating couplers on the photonic chip have the peak of their transmission. The power at the laser output has been set to 5 dBm. The light signal has then been intensity-modulated with a $(2^{31}-1)$-long pseudo-random bit sequence (PRBS-31) thanks to a commercial $LiNbO_3$ Mach-Zehnder modulator. An on-off keying (OOK) modulation scheme at 10 Gbit/s has been chosen due to limitations in the high-speed equipment. Before entering the photonic chip, the light signal has been amplified with an erbium-doped fiber amplifier (IPG photonics EAD-1K-C) to compensate the insertion losses of the modulator and of the following optical switch, around 10 dB in total. The optical switch after the amplifier has been used to easily couple the input light signal to the desired photonic chip port. The light power at the input of the chip can be estimated around 0 dBm, taking into account the grating coupler loss of around 4 dB. Polarization controllers have been used between the instruments and the chip to ensure operations at the optimal polarization.
The signal at the output of the chip has been monitored with both a low-frequency high-accuracy power monitor and with high-speed receivers, thanks to a 90-10 light splitter. The power monitor (HP 81533B) has been used in the control experiment to assess the average light power at the chip output while the high-speed receivers were employed to measure the transmission quality through the router. In particular, an optical oscilloscope (Tektronix CSA8200) has been used to acquire the eye diagrams, while a BER tester (Texas Instruments TLK10034) was employed to acquire the BER measurements. The measurements have been successfully repeated for several input-output configurations of the router, as shown

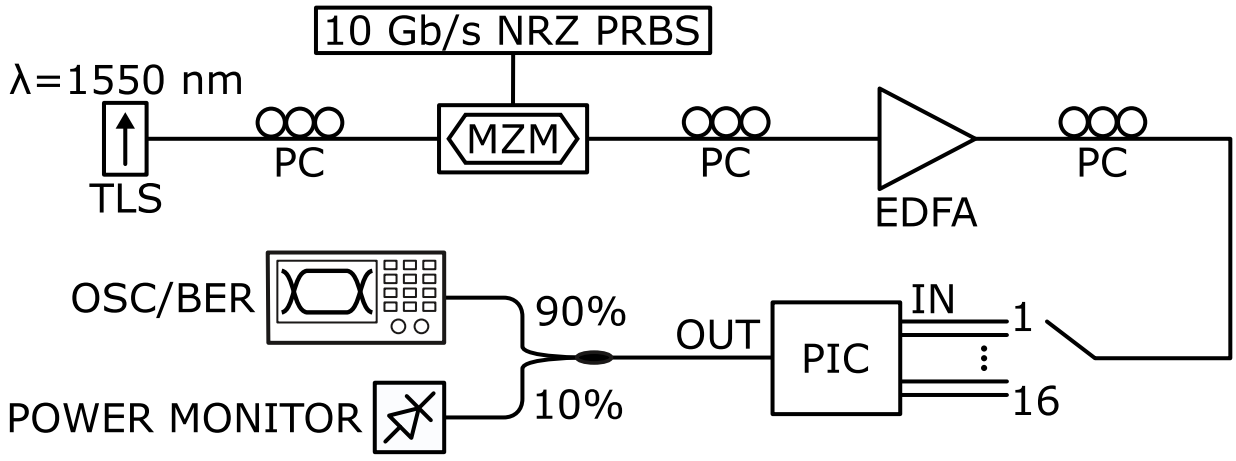

Figure 5: Schematic view of the optical setup, showing the external laser source at 1550 nm, the 10 Gbit/s modulator, the erbium-doped fiber amplifier, the photonic chip and the receiving equipment. In particular, a power monitor was used to measure the average optical power at the output and an optical oscilloscope or a BER tester allowed to assess the transmission quality.

in Figure 5d and 5e in the main article body, demonstrating the correct operation of the circuit controlled with the integrated multiplexer.
The BER measurements have been performed on a time window of few minutes, as described in the following. The employed BER tester stores the number of transmission errors in a register that can host up to 10^8 samples. The number of errors N_e accumulated within a certain time window T_w is used to evaluate the $BER = N_e/N_b$, where N_b is the number of transmitted bits during T_w. In order to avoid register overflow at high error rates (e.g. 10^{-4}), we set $T_w = 1\,\mathrm{s}$ in our measurements, resulting in $N_b = 10^{10}$ when transmitting at 10 Gbit/s. This means that on average we measured $N_e = 10^6$ at $BER = 10^{-4}$ and $N_e = 10^2$ at $BER = 10^{-8}$. Each data point shown in Figure 5d of the main manuscript (reported again here in Figure 6 for convenience) is finally obtained by averaging the BER measurements over 240 time windows, that means for about 4 minutes. BER data processing has been performed by an external computer connected to the BER-tester, providing both the average and the standard deviation of the measurement. For a received optical power of $-5\,\mathrm{dBm}$, the $\pm 3\sigma$ deviation was $\pm 2 \cdot 10^{-8}$ for all the considered IN-OUT configurations.

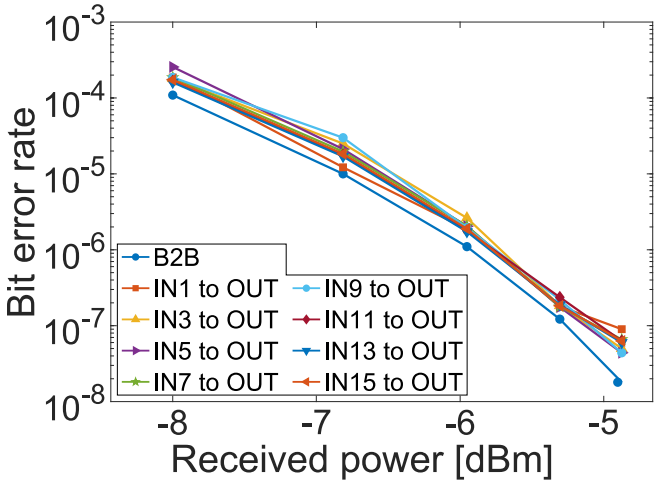

Figure 6: BER measurements for the back-to-back (B2B) case and for 8 different I/O configurations of the 16-to-1 optical router, requiring to read all the photodiodes in the photonic chip. The curves were obtained when routing a 10 Gbit/s modulated signal through the chip.