# Zynq Architecture and Vivado IPI

SDx 2018.2

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# Objectives

- **After completing this module, you will be able to:**
  - Identify the basic building blocks of the Zynq architecture processing system (PS)
  - List the available PS to the programmable logic (PL) connections through the AXI ports
  - Identify clocking sources for the PL peripherals
  - List the various AXI-based system architectural models
  - Describe what is Vivado IPI and how it can be used to view the SDSoC generated hardware

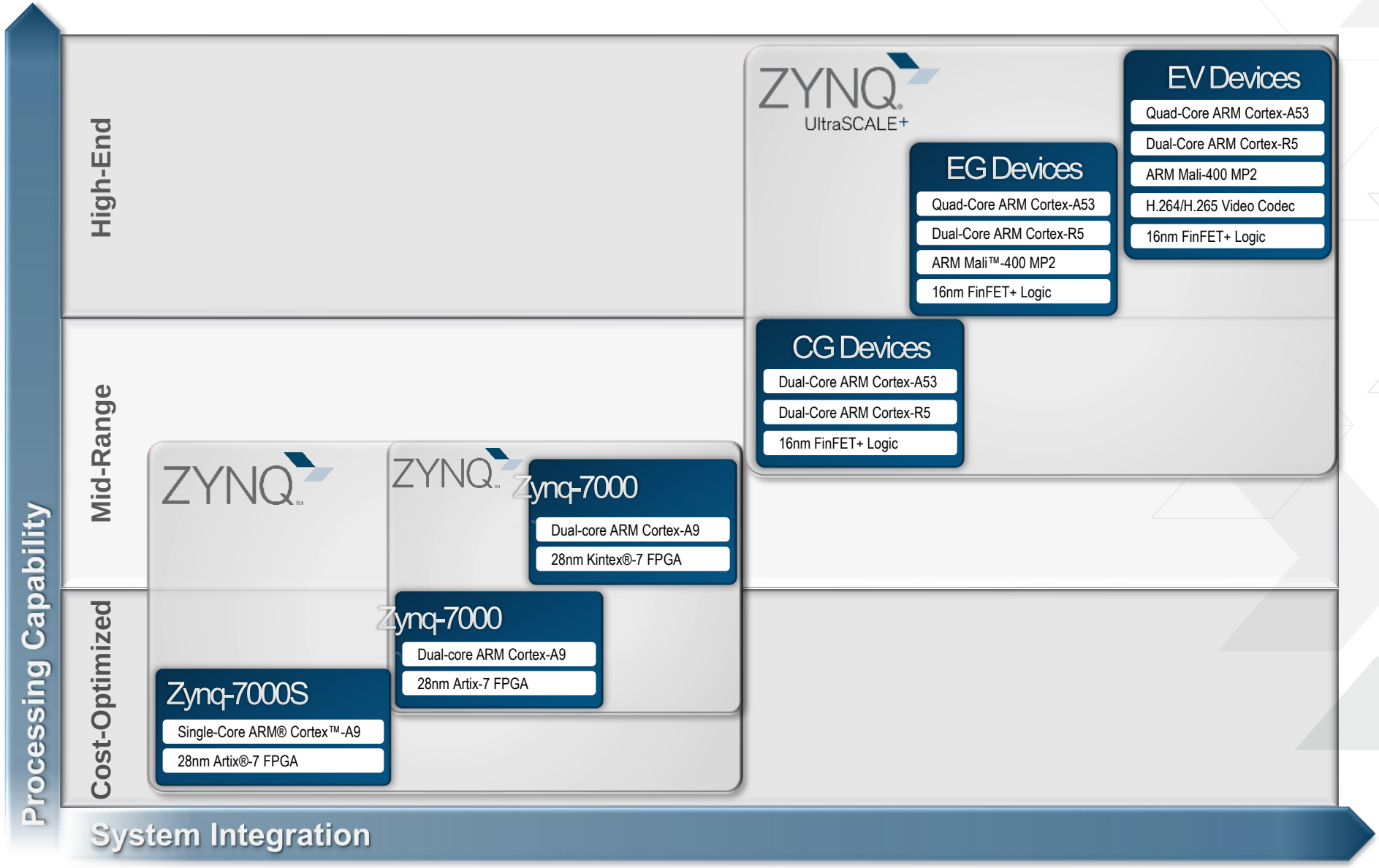
# Outline

- Zynq SoC
- Processor Peripherals and Interfaces
- Clocks and Resets
- AXI Interfaces
- Vivado IPI
- Summary

# The PS and the PL

- **The Zynq-7000 AP SoC architecture consists of two major sections**
  - PS: Processing system
    - Dual ARM Cortex-A9 processor based (Single core versions available)
    - Multiple peripherals
    - Hard silicon core
  - PL: Programmable logic
    - Shares the same 7 series programmable logic as
      - Artix™-based devices: Z-7010, Z-7015, and Z-7020 (high-range I/O banks only)
      - Single core versions: Z-7007S, Z-7012S, and Z-7014S
      - Kintex™-based devices: Z-7030, Z-7035, Z-7045, and Z-7100 (mix of high-range and high-performance I/O banks)

# Extending Scalability Across the Zynq Portfolio





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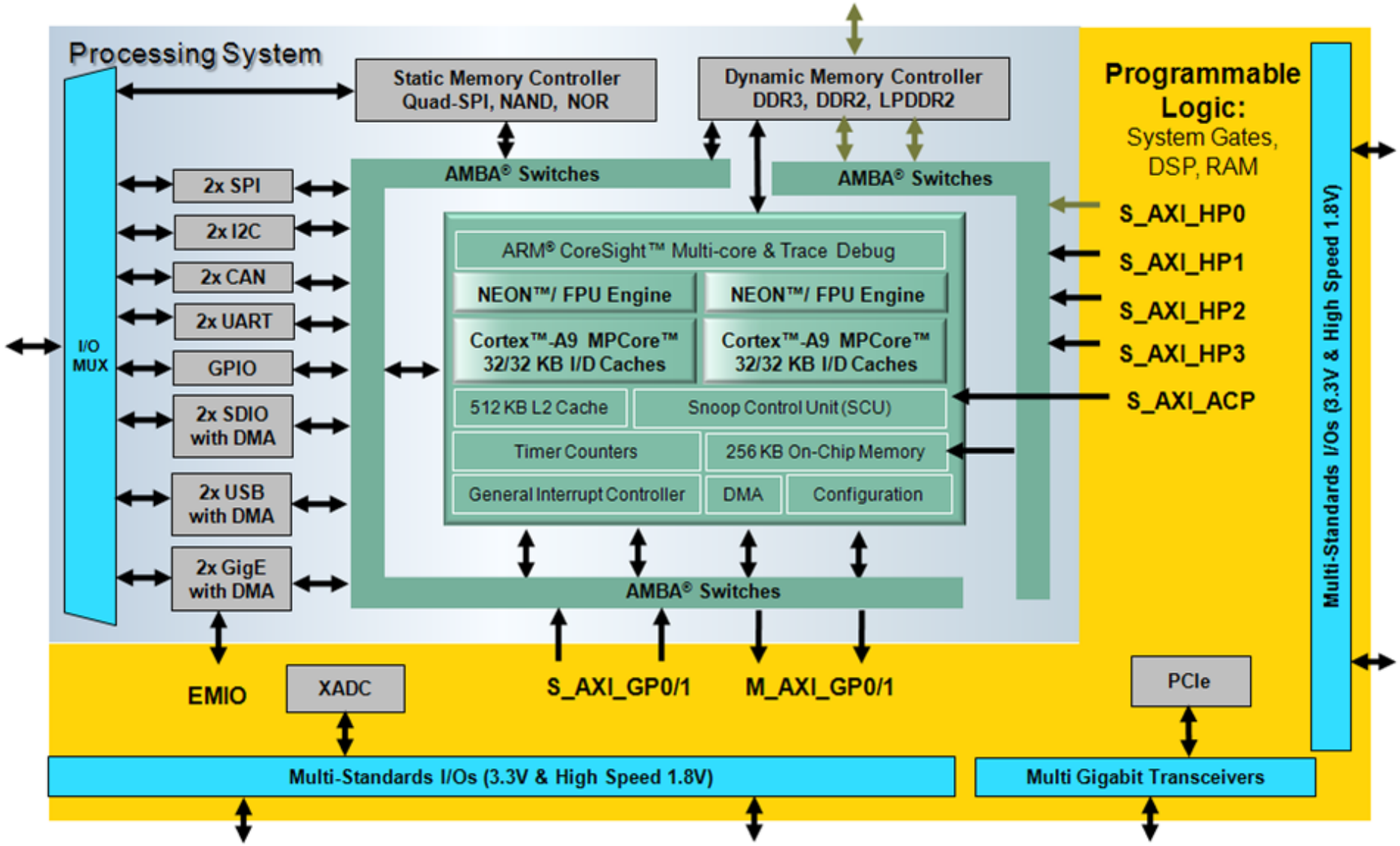
# Zynq-7000 AP SoC Block Diagram





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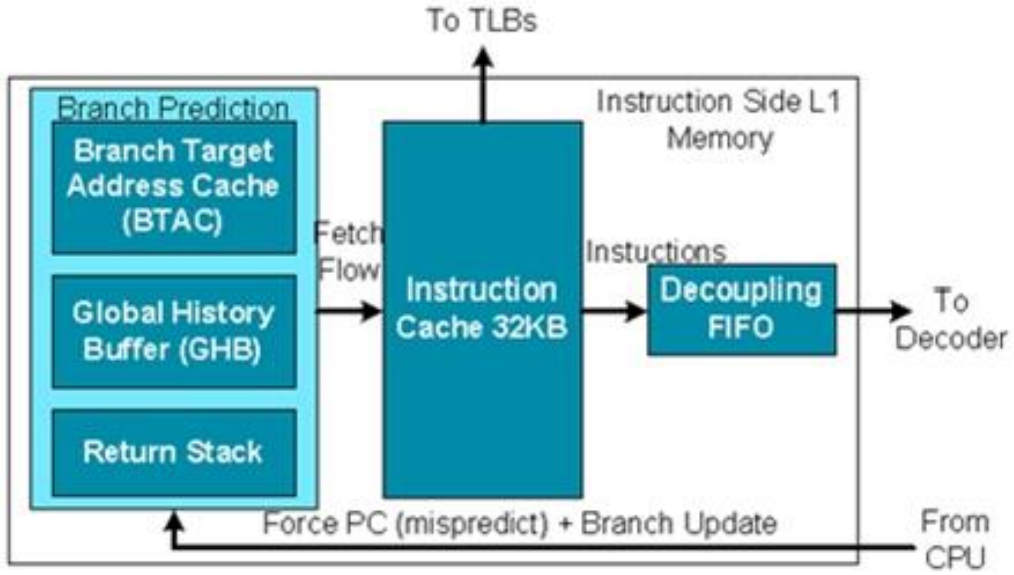
# PS Components

- **Application processing unit (APU)**
- **I/O peripherals (IOP)**
  - Multiplexed I/O (MIO), extended multiplexed I/O (EMIO)
- **Memory interfaces**
- **PS interconnect**
- **DMA**
- **Timers**
  - Public and private
- **General interrupt controller (GIC)**
- **On-chip memory (OCM): RAM**
- **Debug controller: CoreSight**

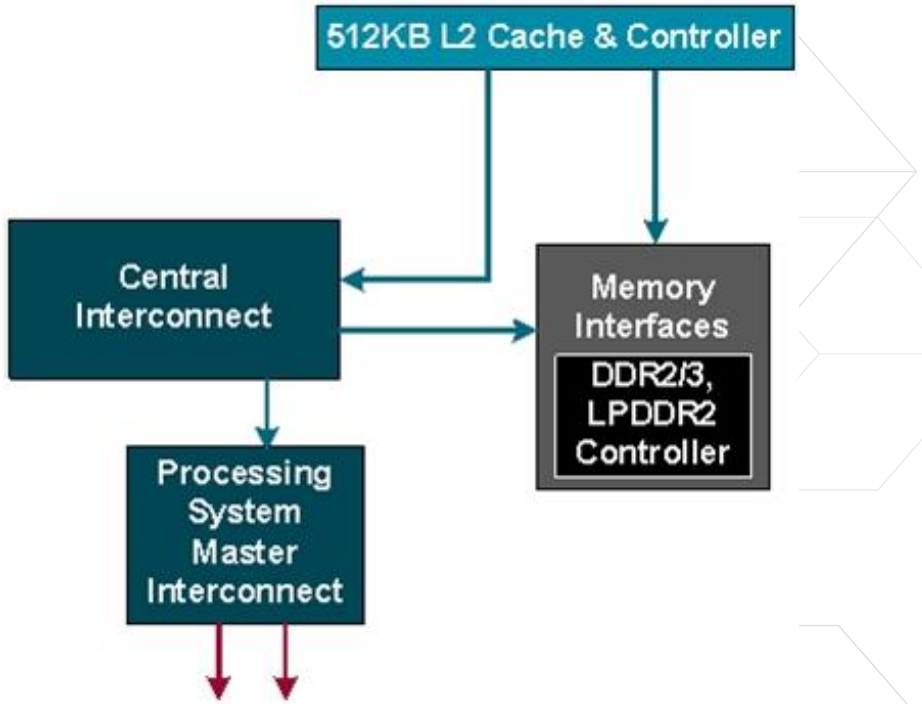
# L1 Cache Features

- Separate instruction and data caches for each processor
- Caches are four-way, set associative and are write-back
- Non-lockable
- Eight words cache length
- On a cache miss, critical word first filling of the cache is performed followed by the next word in sequence



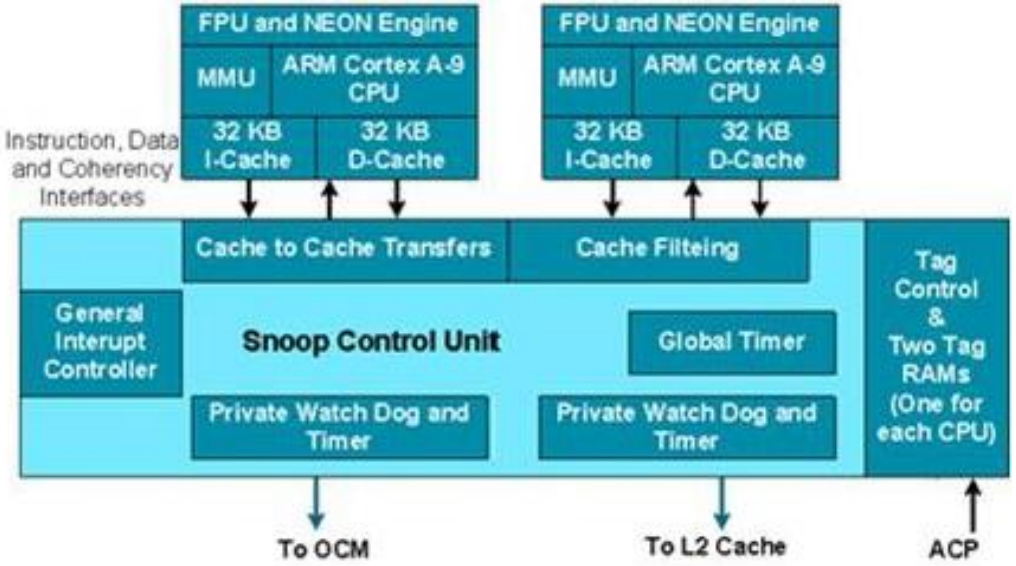
# L2 Cache Features

- **512K bytes of RAM built into the SCU**
  - Latency of 25 CPU cycles
  - Unified instruction and data cache
- **Fixed, 256-bit (32 words) cache line size**
- **Support for per-master way lockdown between multiple CPUs**
- **Eight-way, set associative**
- **Two AXI interfaces**
  - One to DDR controller
  - One to programmable logic master (to peripherals)



# Snoop Control Unit (SCU)

- **Shares and arbitrates functions between the two processor cores**
  - Data cache coherency between the processors
  - Initiates L2 AXI memory access
  - Arbitrates between the processors requesting L2 accesses
  - Manages ACP accesses
  - A second master port with programmable address filtering between OCM and L2 memory support





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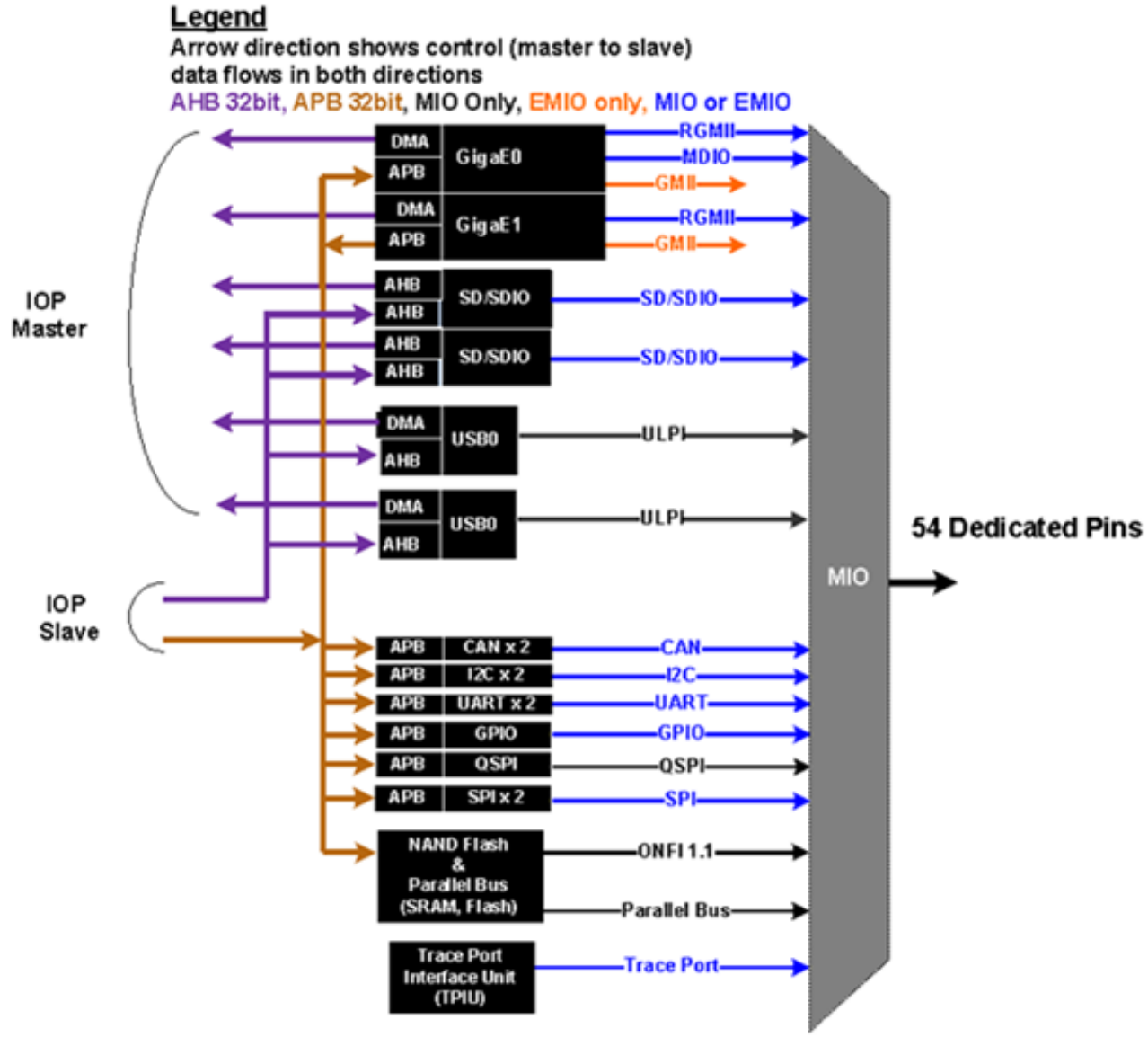
# Processor Peripherals and Interfaces

# Input/Output Peripherals

- Two GigE
- Two USB
- Two SPI
- Two SD/SDIO
- Two CAN
- Two I2C
- Two UART
- Four 32-bit GPIOs
- Static memories
  - NAND, NOR/SRAM, Quad SPI
- Trace ports





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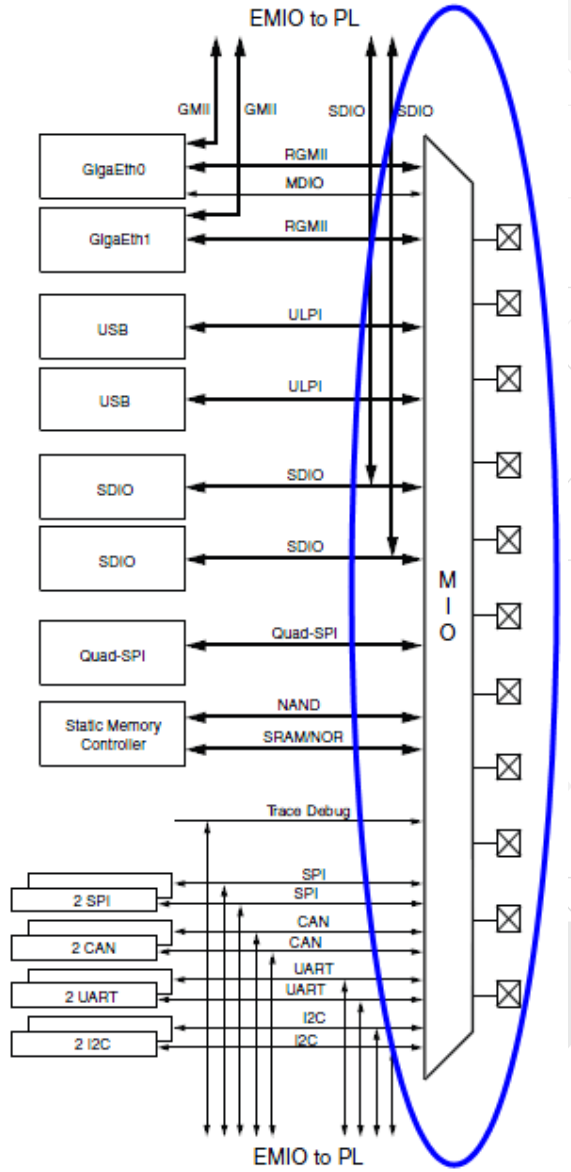
# Multiplexed I/O (MIO)

- **External interface to PS I/O peripheral ports**
  - 54 dedicated package pins available
  - Software configurable
    - Automatically added to bootloader by tools
  - Not available for all peripheral ports
    - Some ports can only use EMIO





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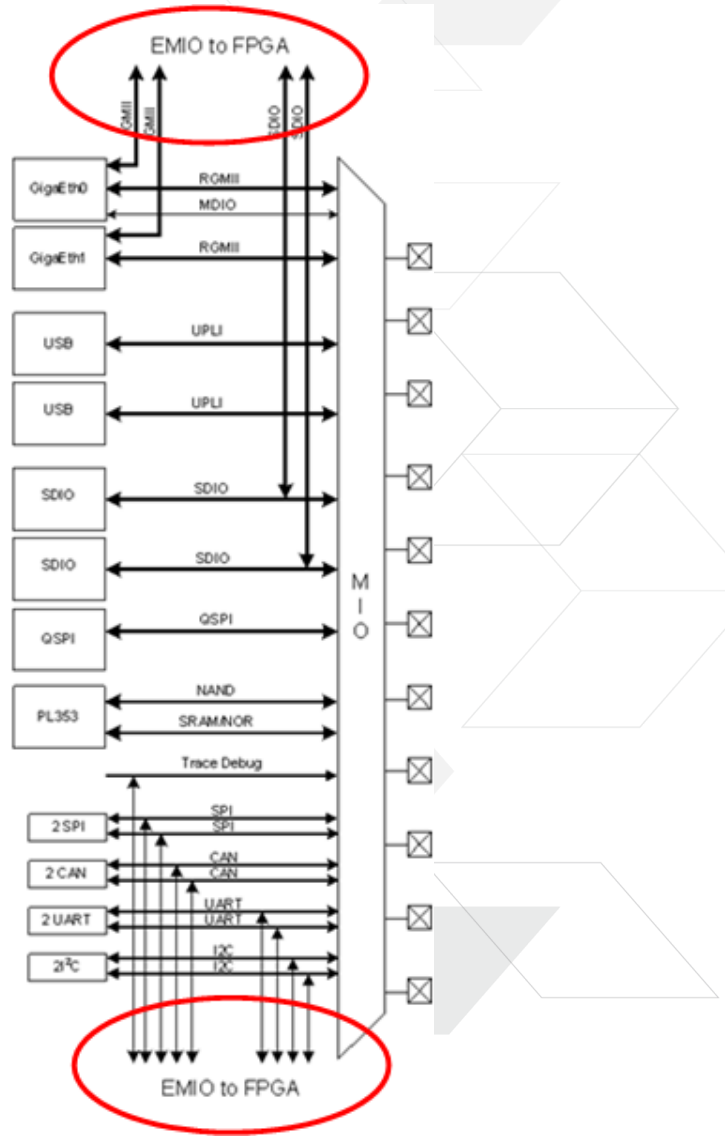
# Extended Multiplexed I/O (EMIO)

- **Extended interface to PS I/O peripheral ports**
  - EMIO: Peripheral port to programmable logic
  - Alternative to using MIO
  - Mandatory for some peripheral ports
  - Facilitates
    - Connection to peripheral in programmable logic
    - Use of general I/O pins to supplement MIO pin usage
    - Alleviates competition for MIO pin usage





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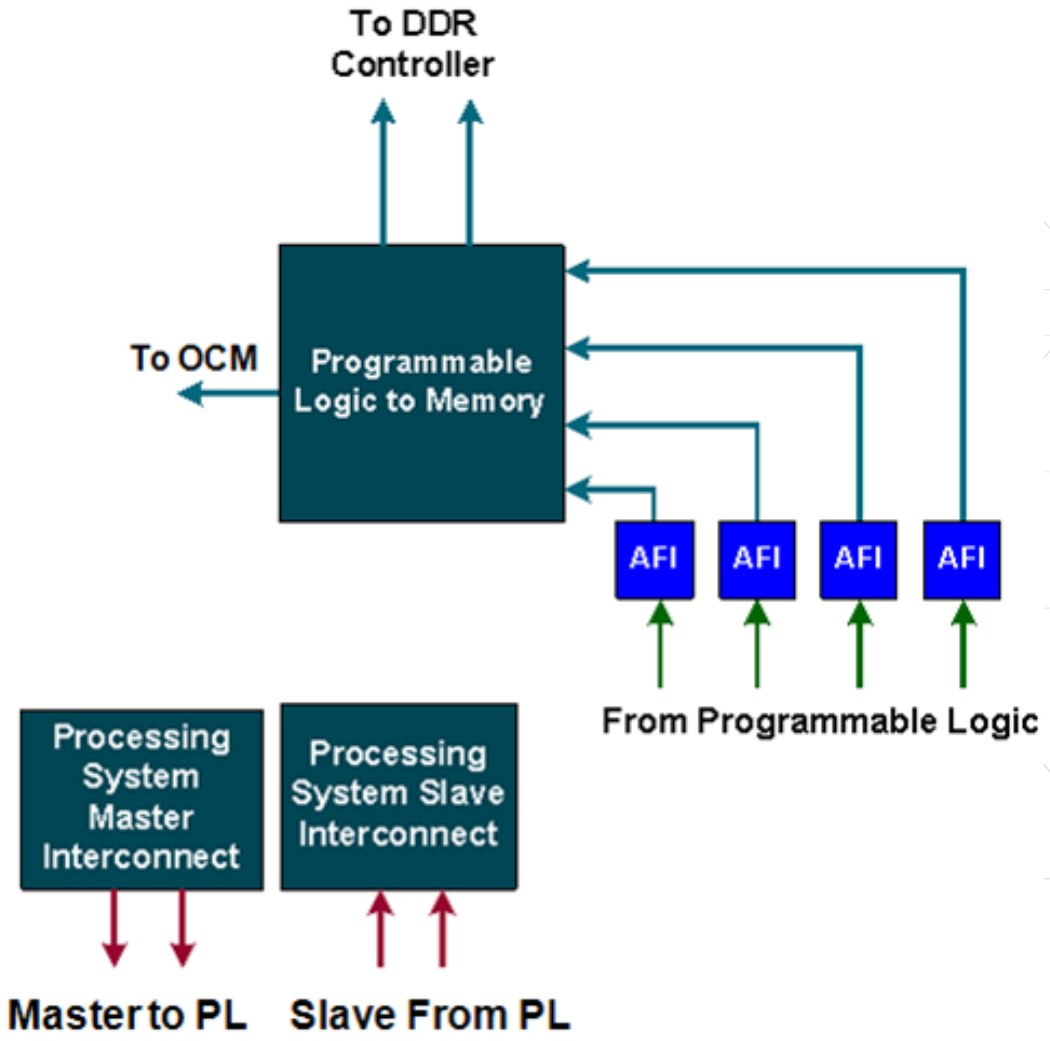
# PS-PL Interfaces

- **AXI high-performance slave ports (HP0-HP3)**
  - Configurable 32-bit or 64-bit data width
  - Access to OCM and DDR only
  - Conversion to processing system clock domain
  - AXI FIFO Interface (AFI) are FIFOs (1KB) to smoo large data transfers
- **AXI general-purpose ports (GP0-GP1)**
  - Two masters from PS to PL
  - Two slaves from PL to PS
  - 32-bit data width
  - Conversation and sync to processing system clock domain





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# PS-PL Interfaces

- **One 64-bit accelerator coherence port (ACP) AXI slave interface to CPU memory**
- **DMA, interrupts, events signals**
  - Processor event bus for signaling event information to the CPU
  - PL peripheral IP interrupts to the PS general interrupt controller (GIC)
  - Four DMA channel RDY/ACK signals
- **Extended multiplexed I/O (EMIO) allows PS peripheral ports access to PL logic and device I/O pins**
- **Clock and resets**
  - Four PS clock outputs to the PL with enable control
  - Four PS reset outputs to the PL
- **Configuration and miscellaneous**

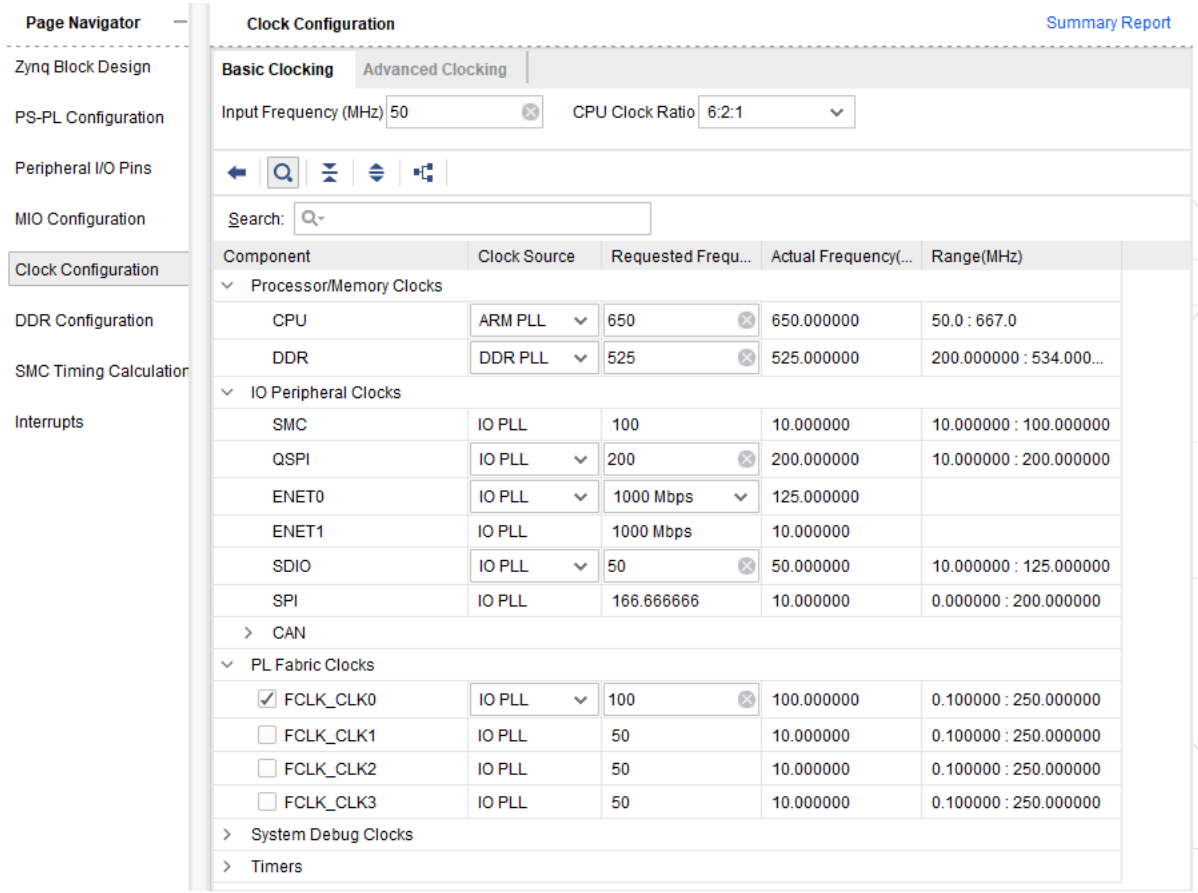
# Clocks and Resets

# PL Clocking Sources

- **PS clocks**
  - PS clock source from external package pin
  - PS has three PLLs for clock generation
  - PS has four clock ports to PL
- **The PL has 7 series clocking resources**
  - PL has a different clock source domain compared to the PS
  - The clock to PL can be sourced from external clock capable pins
  - Can use one of the four PS clocks as source
- **Synchronizing the clock between PL and PS is taken care by the architecture of the PS**
- **PL cannot supply clock source to PS**

# Clock Generation (Using Zynq Tab)

- **Clock Configuration**
  - Input frequency can be set
    - Processor, DDR
  - All IOP clock frequencies can be set
  - PL fabric clocks can be enabled and configured
  - Set Timers





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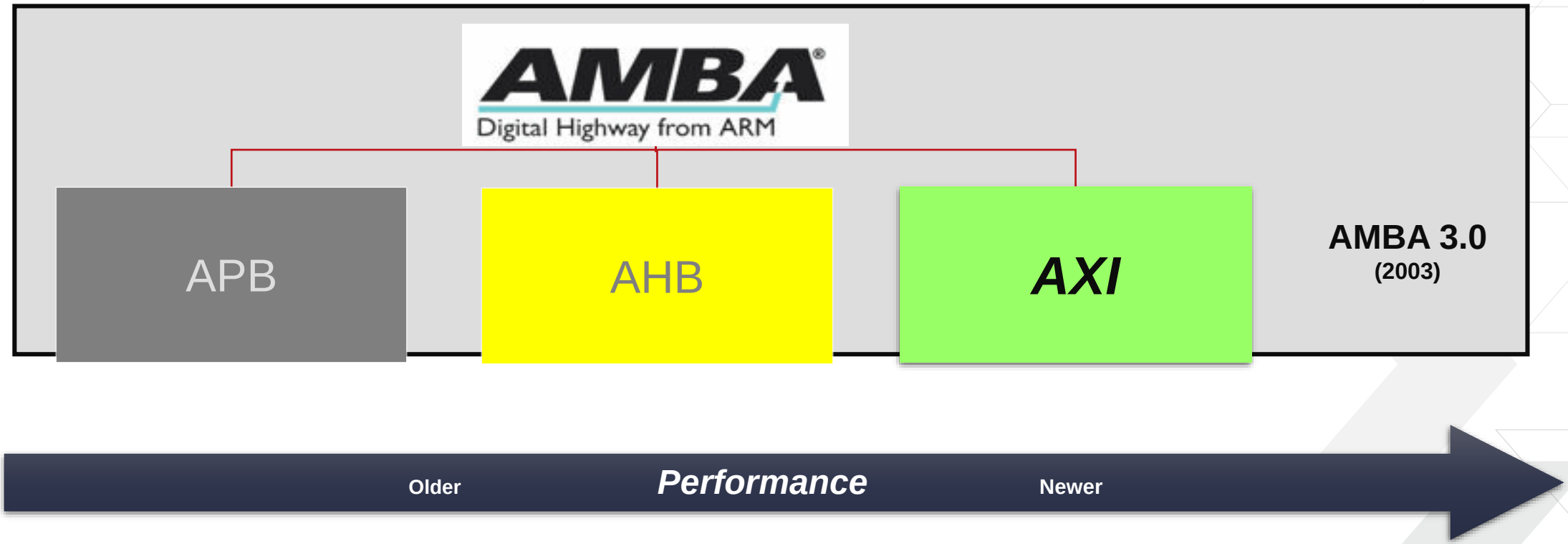
# Zynq Resets

- **Internal resets**
  - Power-on reset (POR)
  - Watchdog resets from the three watchdog timers
  - Secure violation reset
- **PS resets**
  - External reset: PS_SRST_B
  - Warm reset: SRSTB
- **PL resets**
  - Four reset outputs from PS to PL
  - FCLK_RESET[3:0]

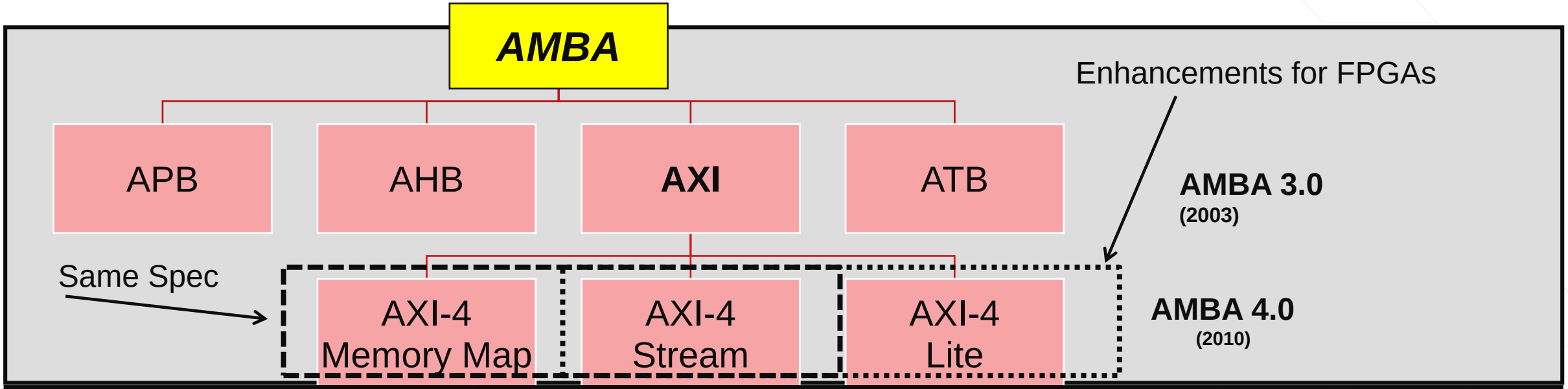
# AXI Interfaces

# AXI is Part of ARM's AMBA




**AMBA: Advanced Microcontroller Bus Architecture**
**AXI: Advanced Extensible Interface**

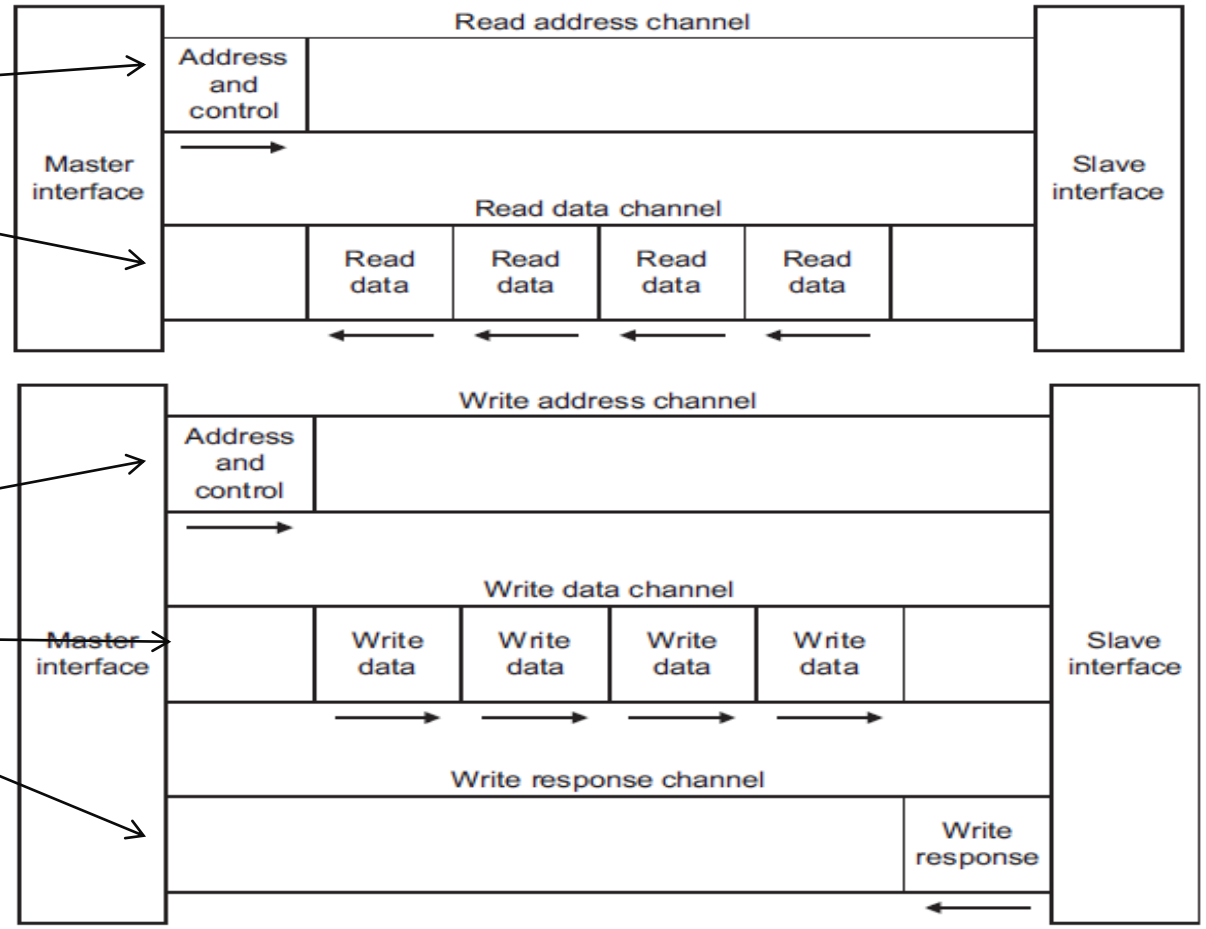
# AXI is Part of AMBA




| Interface | Features |
|---|---|
| **Memory Map / Full (AXI4)** | **Traditional Address/Data Burst (single address, multiple data)** |
| **Streaming (AXI4-Stream)** | **Data-Only, Burst** |
| **Lite (AXI4-Lite)** | **Traditional Address/Data—No Burst (single address, single data)** |

# Basic AXI Signaling – 5 Channels

1. Read Address Channel
2. Read Data Channel
3. Write Address Channel
4. Write Data Channel
5. Write Response Channel





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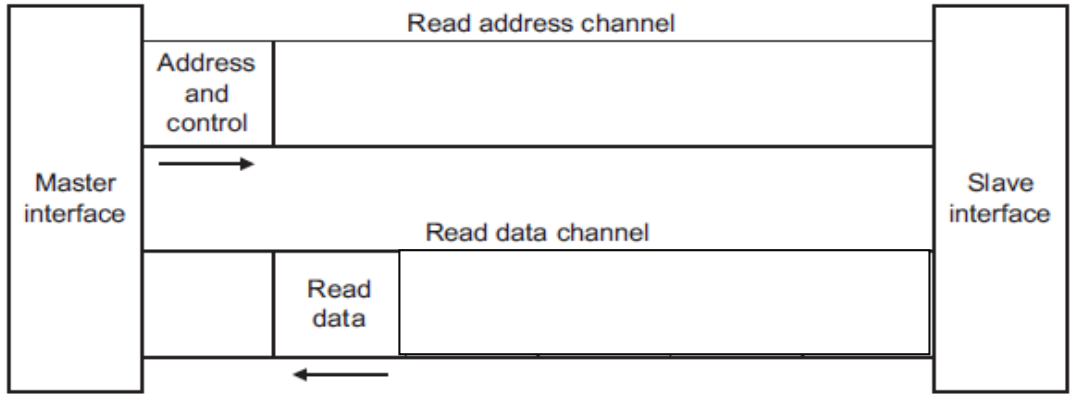
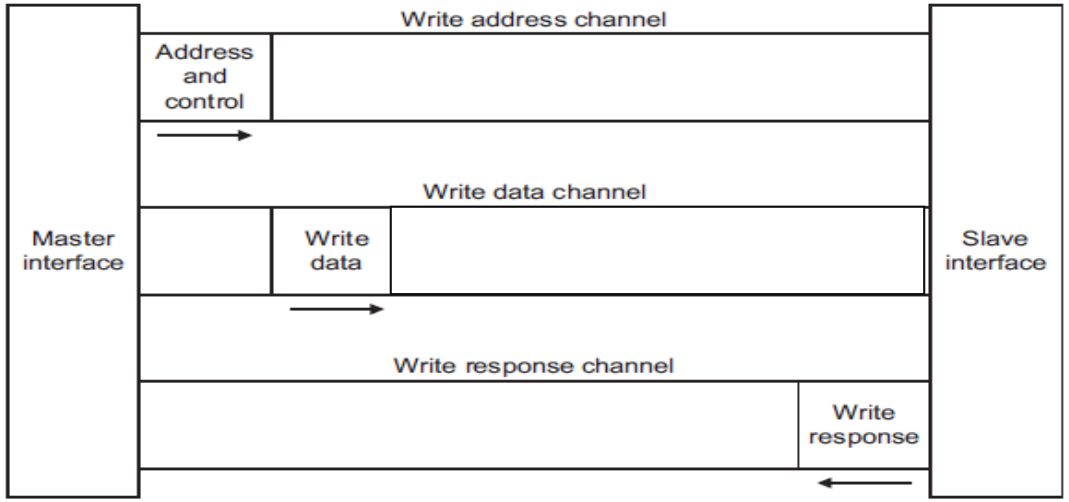
# The AXI Interface—AXI4-Lite

- **No burst**
- **Data width 32 or 64 only**
  - Xilinx IP only supports 32-bits
- **Very small footprint**
- **Bridging to AXI4 handled automatically by AXI_Interconnect (if needed)**




AXI4-Lite Read




AXI4-Lite Write





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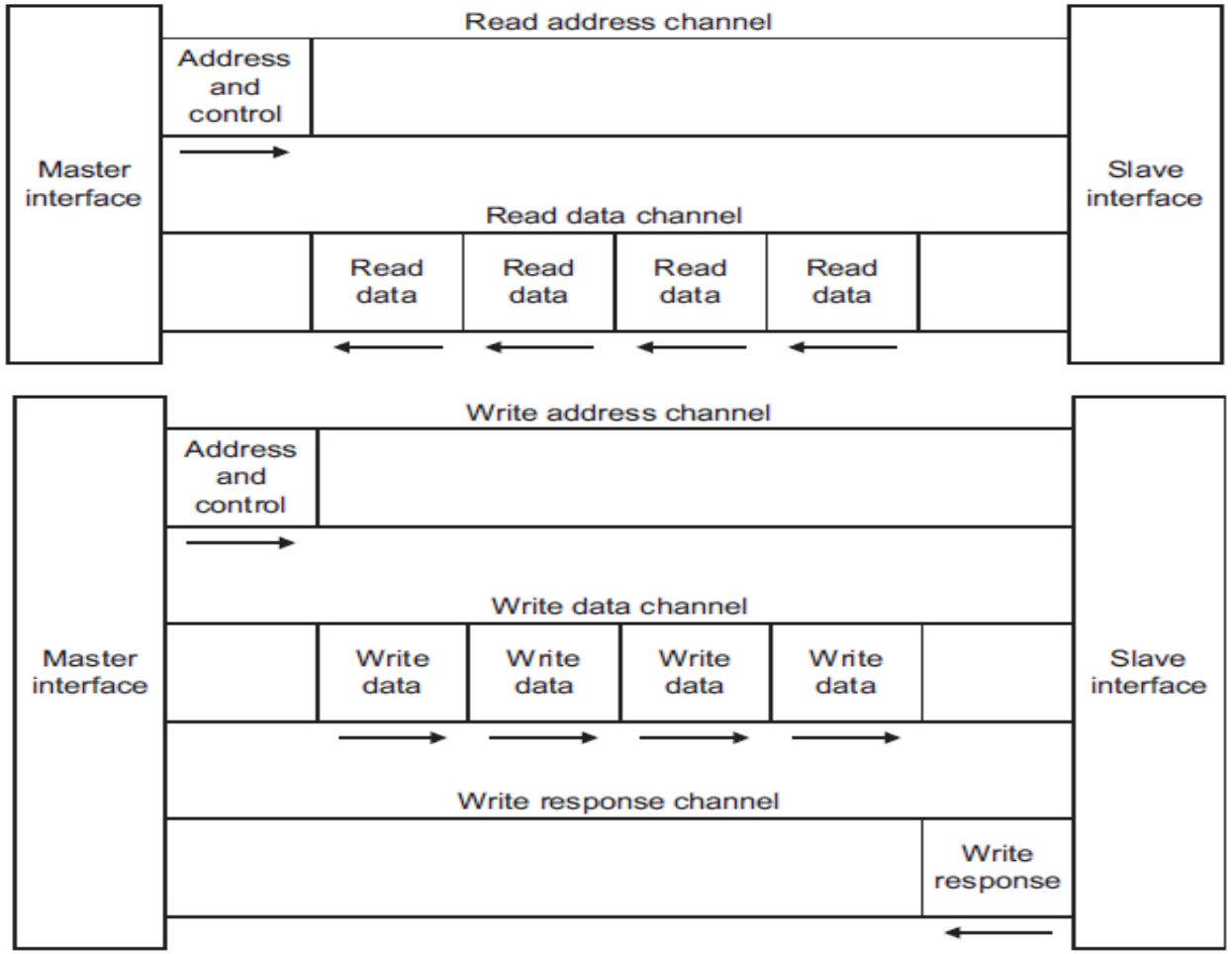
# The AXI Interface—AXI4

- **Sometimes called “Full AXI” or “AXI Memory Mapped”**
  - Not ARM-sanctioned names
- **Single address multiple data**
  - Burst up to 256 data beats
- **Data Width parameterizable**
  - 1024 bits





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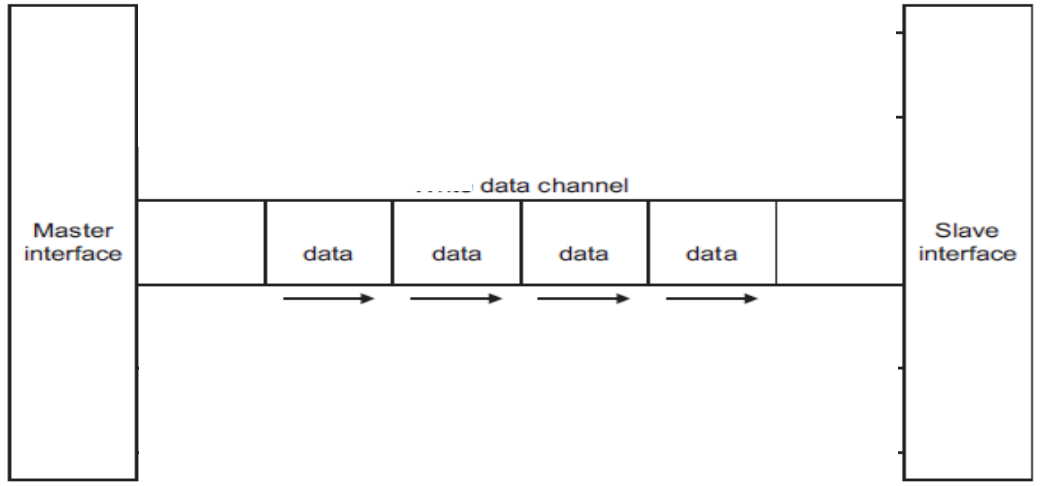
# The AXI Interface—AXI4-Stream

- **No address channel, no read and write, always just master to slave**
  - Effectively an AXI4 “write data” channel
- **Unlimited burst length**
  - AXI4 max 256
  - AXI4-Lite does not burst
- **Virtually same signaling as AXI Data Channels**
  - Protocol allows merging, packing, width conversion
  - Supports sparse, continuous, aligned, unaligned streams

AXI4-Stream Transfer





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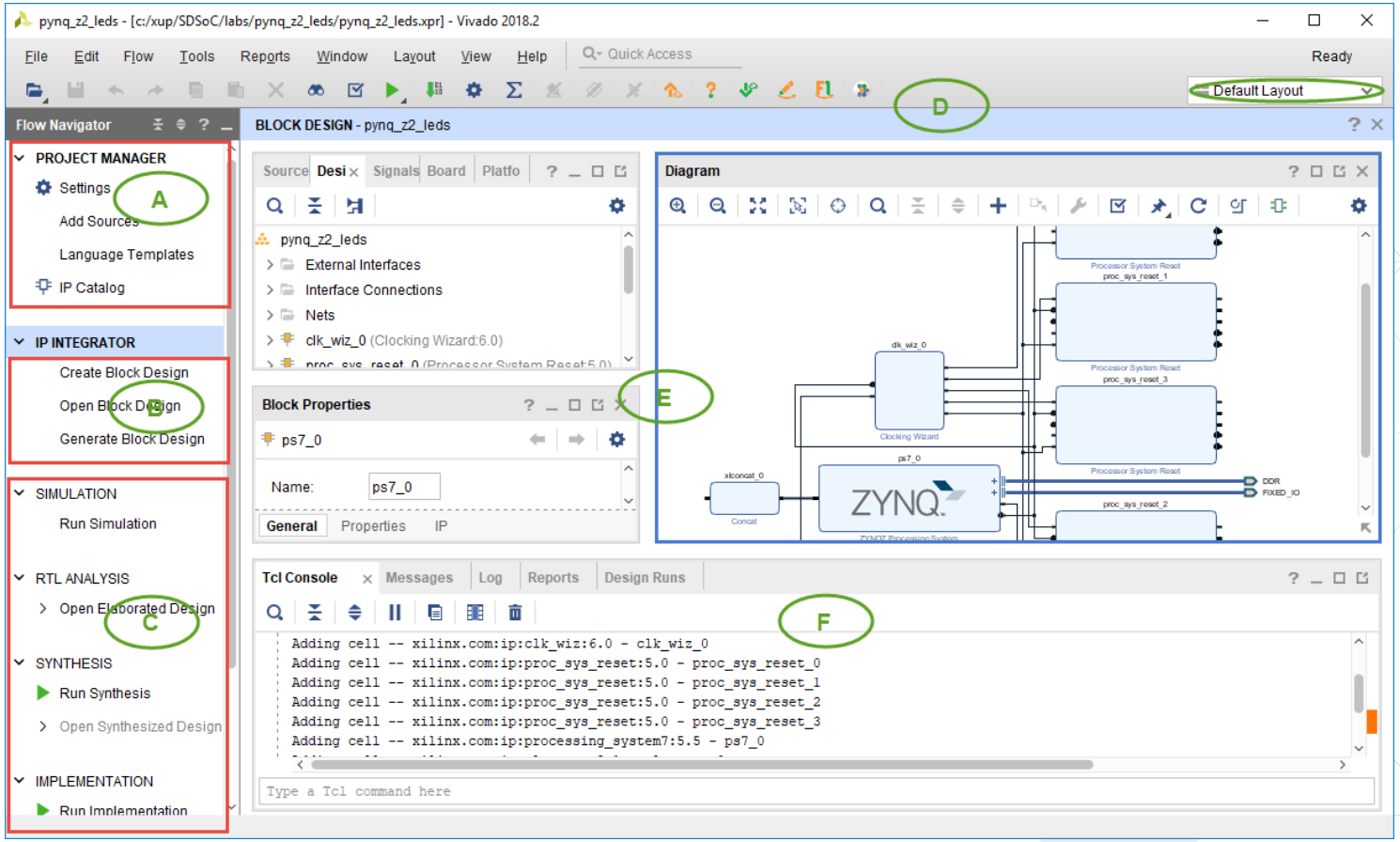
# Vivado IPI

# Vivado View

- **Customizable panels**
  - A: Project Management
  - B: IP Integrator
  - C: FPGA Flow
  - D: Layout Selection
  - E: Project view/Preview Panel
  - F: Console, Messages, Logs





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# Summary

# Summary

- **The Zynq-7000 processing platform is a system on a chip (SoC) processor with embedded programmable logic**
- **The processing system (PS) is the hard silicon dual core consisting of**
  - APU and components
    - Two Cortex-A9 processors
    - NEON co-processor
    - General interrupt controller (GIC)
    - General and watchdog timers
  - I/O peripherals
  - External memory interfaces
- **The PS provides clocking resources to the PL**
- **Vivado IPI can be used to see the generated hardware**

# Summary (2)

- **The programmable logic (PL) consists of 7 series devices**
- **Communication between the PS and the peripherals in PL may occur using**
  - Four HP slave ports
  - Two GP master ports
  - Two GP slave ports
  - An ACP slave port
- **AXI is an interface providing high performance point-to-point connection**
- **AXI has separate, independent read and write interfaces implemented with channels**
- **The AXI4 interface offers improvements over AXI3 and defines**
  - Full AXI memory mapped
  - AXI Lite
  - AXI Stream

# Adaptable.
# Intelligent.

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