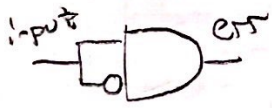
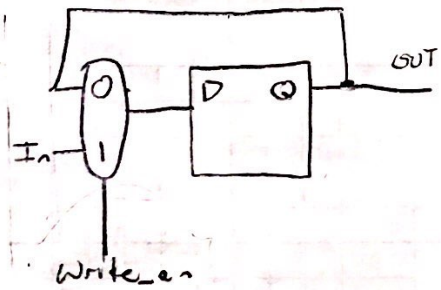
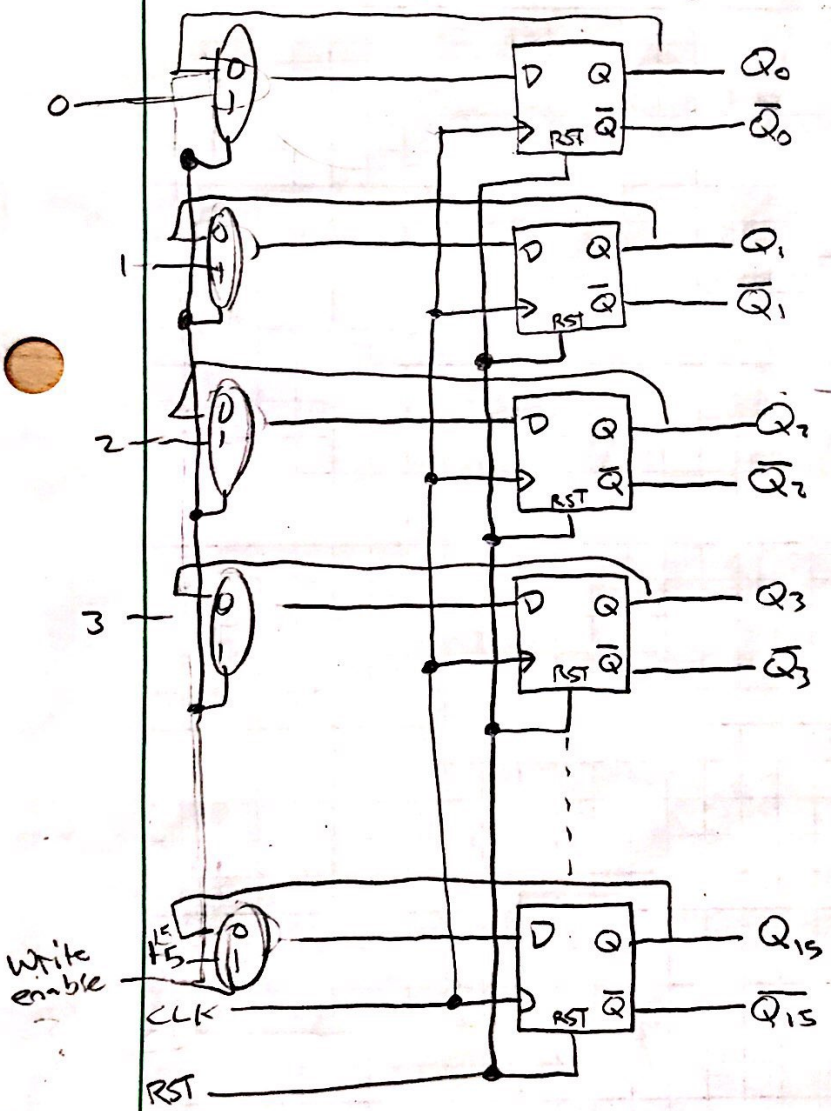
8x16 Register File (8 registers, 16 bits each)

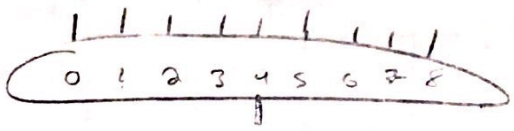
1 write port
2 read ports
3 register select inputs (2 for read, 1 for write) (each are 3 bits)
1 write enable
1 reset (active high)
1 clock (rising edge)
1 error output
Use D-Flip-Flops
Read ports are combinational logic.
No TRI-STATE LOGIC ALLOWED



Step 1) Design a 16-bit register



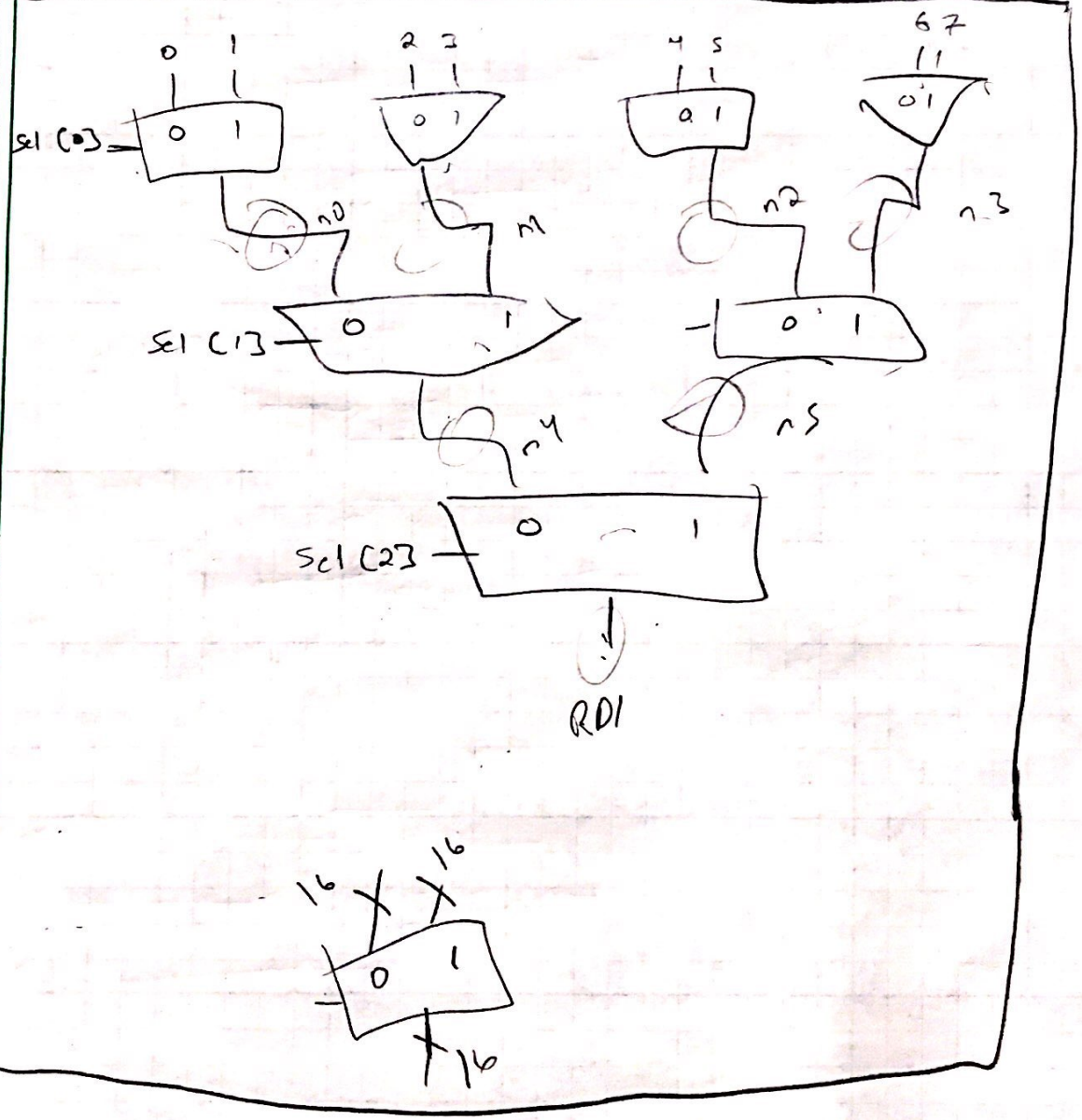




0	000
1	001
2	010
3	011
4	100
5	101
6	110
7	111

000
writtl = unknown

Read Reg Select



Full system For HW5_1