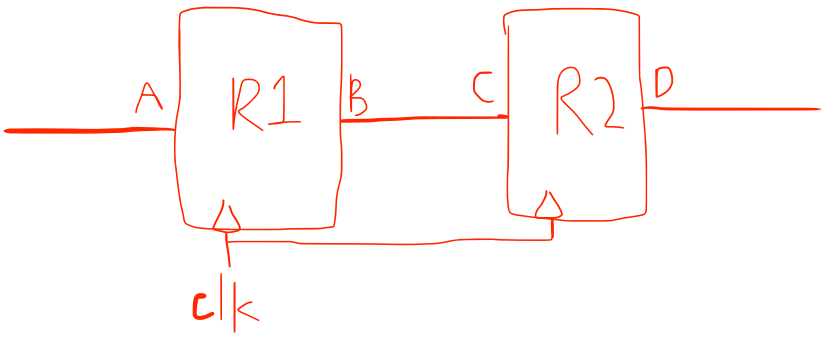
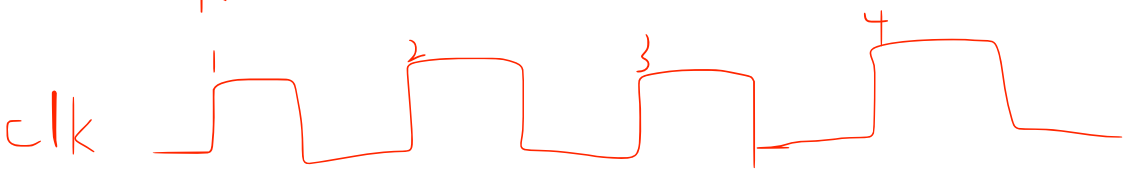


The example becomes clearer when we look at only the wires in the diagram. Call them:

A = input of register 1
B = output of register 1
C = input of register 2
D = output of register 2

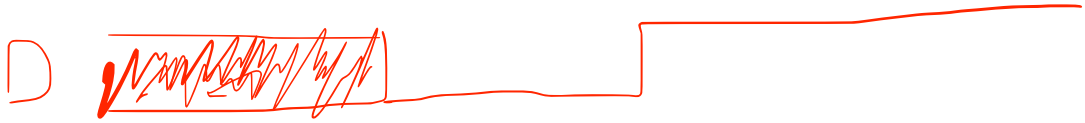


Let's say A is some arbitrary input signal.

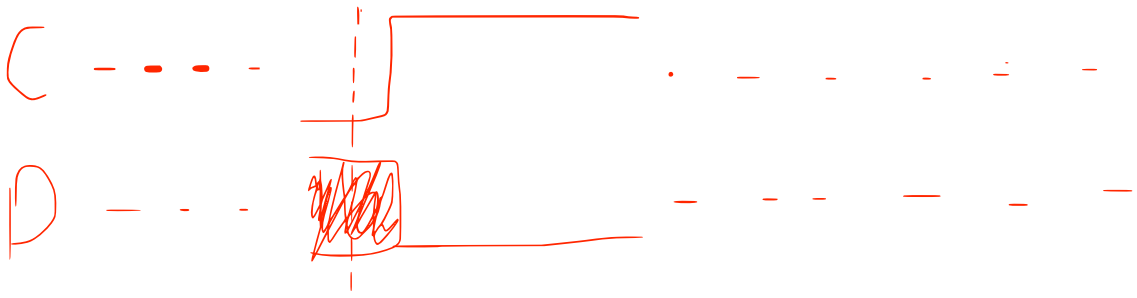
Register 1 propagates the value of A to B at each rising edge.

C has the same value as B since it's part of the same wire.

Register 2 propagates the value of C to D at each rising edge.



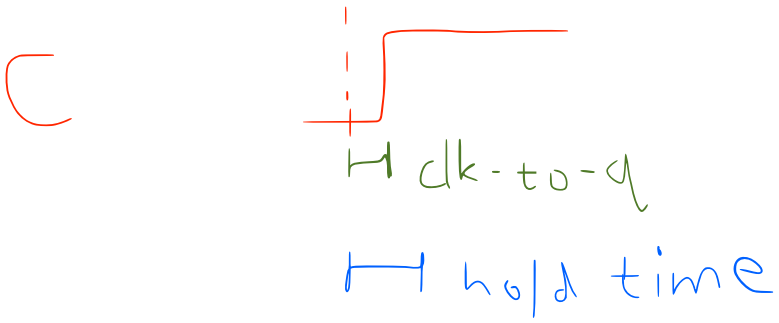
Let's take a closer look at what happens when Register 2 propagates the value of C at rising edge 2.



Note that Register 2 reads the value of C at the rising edge, which is still 0. Shortly after the rising edge (after clk-to-q time), the value of C updates to the value Register 1 will hold for the next clock cycle, 1.

Remember that due to hold time constraints, C needs to be held constant for a certain amount of time after the rising edge in order for Register 2 to properly read its value. However, as we can see in the waveform, C changes shortly after the rising edge. Does this mean that we are violating the hold time constraint of Register 2?

It depends. If the clk-to-q time of Register 1 is shorter than the hold time of Register 2:



Then C has changed to soon after the rising edge, meaning there is a hold time violation in this circuit. The value of D is now unknown, rather than 0.

On the other hand, if the clk-to-q time of Register 1 is longer than the hold time of Register 2, there will be no hold time violation, since C will change after the needed period of stability after the rising edge. However, clk-to-q time is often shorter than hold time.

So, how do fix this violation while keeping the functionality of this circuit the same? One way to fix it (as discussed in class) is to add an even number of inverters (NOT gates) between the registers, in order to introduce combinational delay. In this case, C will be updated slightly later than B, meaning with enough registers, we'll be able to "hold" C's value constantly sufficiently long after the rising edge of the clock. For example: