		IW in	put b	its							Cont	trol output	bits																	
	INAME		26		5 2	4	23	22	21	2	0 RFV			Extop0	ALUsrcB	ALU	p2 ALUop	1 ALUo	0 PCse	I1 PCse	IO RI	R0sel1	RR0sel0	RR1sel	WRsel	WDsel	MR	MW	input bits	output bits
add(r)	ADDR	0				0	1	0			0	1	. 0						0	0	0	0	0	0	0				о оьоооо1ооо	
add(i)	ADDI	0	0)	1	0	1	0	0		0	1	0	0	1		0	0	0	0	0	0	0	0	0	0	C		0 0Ь00101000	
mov(r)	MOVR	0			0	1	1	0	1		0	1	0						1	0	0	0	0	0	0				о 0600011010	
mov(i)	MOVI	0				1	1	0	1		0	1	0					1	1	0	0	0	0	0	0				0 0Ь00111010	
ldr(i)(up)	LDRI	0	1		0	1	1	0	0		1	1	0	1	1		0	0	0	0	0	0	0	0	0	0	1		0 0b01011001	0b10110000000000010
str(i)(up)		0	1		0	1	1	0	0		0	0	0	1	1				0	0	0	0	0	1	0	0	C		1 0b01011000	
b	В	1	0)	1	0	Х	Х	Х		x	0	1	0	1		0	0	0	0	1	0	1	0	0	0	C		0 0b1010XXXX	0b0101000010100000
bl	BL	1	0)	1	1	Х	Х	Х		x	1	1	0	1		0	0	0	0	1	0	1	0	1	1	C	1	0 0b1011XXXX	0b1101000010101100
bx	BX	(a)										0	0						0	1	0	0	0	0	0	0			0 Øb(a)	0b000000100000000
nop	NOP_	(b)										0	0	0	0		0	0	0	0	0	0	0	0	0	0	C		0 Øb(b)	060000000000000000000000000000000000000
none	NONE	(c)										0	0	0	0		0	0	0	0	0	0	0	0	0	0	C		0 Øb(c)	
	(a) Chec	k for B	хсо	DE 0	x12F	FF1																								
	(b) Chec	ck for 0	xE1A	0000	0																									
	(c) Chec	k for 0	x0000	0000	0																									
											1																			
											-																			
											-																			
											-																			
											_																			
											_																			
											1																			
											-																			
											-																			
											\perp																			
											-																			
											-																			
											+																			
											-																			
											+																			

	IIW in	put bir	ts						Control	output bits															1	
NAME	27	26	25	24	23	2	2 2	1 20	RFW	EXTop1	Extop0	ALUsrcB	ALUop2	ALUop1	ALUop0	PCsel1	PCsel0	RR0sel*	RR0sel0	RR1sel	WRsel	WDsel	MR	MW	input bits	output bits
											· ·				· ·											
									1																	
									1																	
									1																	
									1																	
									1																	
									1																	
									1																	
									1																	
									1																	
									1																	
									1																	
									1																	
									1																	
									1																1	

	IW in	put bit	S						Control	output bits																
NAME	27	26	25	24	23	2	2 2	1 20	RFW	extrop1	Extop0	ALUsrcB	ALUop2	ALUop1	ALUop0	PCsel1	PCsel0	RR0sel1	RR0sel0	RR1sel	WRsel	WDsel	MR	MW	input bits	output bits
									-																	
									1																	
									1																	
									1												-				-	
									1																	
									1																	
									1																	
									1																	
									1																	
									1																	
									1																	
									1												-					
									1																	
									1								1				I				I	

	IIW in	put bit	S						Contro	l output bits															1	
NAME	27	26	25	24	23	2	2 2	1 2	0 RFW	EXTop1	Extop0	ALUsrcB	ALUop2	ALUop1	ALUop0	PCsel1	PCsel0	RR0sel1	RR0sel0	RR1sel	WRsel	WDsel	MR	MW	input bits	output bits
											· ·				· ·											
									_																	
									-																	
									_																	
									1																	
									-																	
									1																	
									_																	
									1																	
									1																	
									-																	
									_																	
									1																	
									-																	
																					-				1	
									-																	
									1								1				ı					

	IIW in	put bir	ts						Control	output bits															1	
NAME	27	26	25	24	23	2	2 2	1 20	RFW	EXTop1	Extop0	ALUsrcB	ALUop2	ALUop1	ALUop0	PCsel1	PCsel0	RR0sel*	RR0sel0	RR1sel	WRsel	WDsel	MR	MW	input bits	output bits
											· ·				· ·											
									1																	
									1																	
									1																	
									1																	
									1																	
									1																	
									1																	
									1																	
									1																	
									1																	
									1																	
									1																	
									1																	
									1																1	

	I IVV Ir	put bi	ts						Control of	output bits																
NAME	27	26	25	24	23	2	2 2	1 20	RFW	EXTop1	Extop0	ALUsrcB	ALUop2	ALUop1	ALUop0	PCsel1	PCsel0	RR0sel1	RR0sel0	RR1sel	WRsel	WDsel	MR	MW	input bits	output bits
									1																	
									1																	
																	-									
																	1				1					

	IW in	put bit	s						Control of	output bits																
NAME	27	26	25	24	23	22	2 2	1 20	RFW	EXTop1	Extop0	ALUsrcB	ALUop2	ALUop1	ALUop0	PCsel1	PCsel0	RR0sel1	RR0sel0	RR1sel	WRsel	WDsel	MR	MW	input bits	output bits
									-												-					
																					-					
									-												-					
									l																	
									1												1				I	

	I IVV Ir	put bi	ts						Control of	output bits																
NAME	27	26	25	24	23	2	2 2	1 20	RFW	EXTop1	Extop0	ALUsrcB	ALUop2	ALUop1	ALUop0	PCsel1	PCsel0	RR0sel1	RR0sel0	RR1sel	WRsel	WDsel	MR	MW	input bits	output bits
									1																	
									1																	
																	-									
																	1				1					

	IIW in	put bit	s						Control	output bits																
NAME	27	26	25	24	23	2	2 2	1 20	RFW	EXTop1	Extop0	ALUsrcB	ALUop2	ALUop1	ALUop0	PCsel1	PCsel0	RR0sel1	RR0sel0	RR1sel	WRsel	WDsel	MR	MW	input bits	output bits
									1																	
									-																	
									1																	
									1																	
									1																	
									1												-					
									1																	
									1																	
									1																	
									1												-				1	
									-																	
									1								1				I				1	

	IIW in	put bi	ts						Control o	output bits																
NAME	27	26	25	24	23	2	2 2	1 20	RFW	EXTop1	Extop0	ALUsrcB	ALUop2	ALUop1	ALUop0	PCsel1	PCsel0	RR0sel1	RR0sel0	RR1sel	WRsel	WDsel	MR	MW	input bits	output bits
									1																	
									1																	
																									1	
																	1				1					

	I IVV III	put bi	is						Control	output bits																
NAME	27	26	25	24	23	2	2 2	1 2	RFW	EXTop1	Extop0	ALUsrcB	ALUop2	ALUop1	ALUop0	PCsel1	PCsel0	RR0sel1	RR0sel0	RR1sel	WRsel	WDsel	MR	MW	input bits	output bits
									1																	
									_																	
									_																	
									1																	
									1																1	
									1																	
									1																	
									1																	
									_																	
									1																	
									_																	
									1																	
									1																	
									1								-				-					
									1																	
									1																	
									1																	
									1																	
																	1				1					

	IW in	put bi	ts						Control	output bits																
NAME	27	26	25	24	23	2	2 2	1 20	RFW	extrop1	Extop0	ALUsrcB	ALUopa	ALUop1	ALUop0	PCsel1	PCsel0	RR0sel1	RR0sel0	RR1sel	WRsel	WDsel	MR	MW	input bits	output bits
									1																	
									1																	
									-																	
									1																	
									1																	
									1																	
									-																	
									1																	
									1																	
									1																1	
									1												-					
									-																	
									1																	
									1																	
									1																	
									1																	
									1																	
									1																1	

	I IVV in	put bi	ts						Control o	output bits																
NAME	27	26	25	24	23	2	2 2	1 20	RFW	EXTop1	Extop0	ALUsrcB	ALUop2	ALUop1	ALUop0	PCsel1	PCsel0	RR0sel1	RR0sel0	RR1sel	WRsel	WDsel	MR	MW	input bits	output bits
									1																	
									1																	
																	1				1					

	IW in	put bit	ts						Control	output bits																
NAME	27	26	25	24	23	2	2 2	1 2	0 RFW	output bits EXTop1	Extop0	ALUsrcB	ALUop2	ALUop1	ALUop0	PCsel1	PCsel0	RR0sel1	RR0sel0	RR1sel	WRsel	WDsel	MR	MW	input bits	output bits
									1																	
									_																	
									-																	
									_																	
									1																	
									1																	
									-																	
									1																	
									1																	
									-																	
									1								-				-					
									1																	
									1																	
									1																	
									-																	
									1																	
									1																	
									1								-				-				1	
									-																	
																	I				ı				1	

	I IVV Ir	put bi	ts						Control o	output bits																
NAME	27	26	25	24	23	2	2 2	1 20	RFW	EXTop1	Extop0	ALUsrcB	ALUop2	ALUop1	ALUop0	PCsel1	PCsel0	RR0sel1	RR0sel0	RR1sel	WRsel	WDsel	MR	MW	input bits	output bits
									1																	
									1																	
																	1				1					

	IW ir	put bi	ts						Control	output bits																
NAME	27	26	25	24	23	3 2	2 2	1 2	0 RFW	EXTop1	Extop0	ALUsrcB	ALUop2	ALUop1	ALUop0	PCsel1	PCsel0	RR0sel1	RR0sel0	RR1sel	WRsel	WDsel	MR	MW	input bits	output bits
									1																	
									1																	
									1																	
									1																	
									1																	
									1												-				1	
									1																	
									1																	
									1																	
									-																-	
									1																	
									1																	
									1																	
									1																	
									1																	

	IW in	put bi	ts						Control o	utput bits																
NAME	27	26	25	24	23	22	2 21	20	RFW	EXTop1	Extop0	ALUsrcB	ALUop	2 ALUop1	ALUop0	PCsel1	PCsel0	RR0sel1	RR0sel0	RR1sel	WRsel	WDsel	MR	MW	input bits	output bits
																	-								ļ	
									l																	
									-																	
									l																	
									-																	
									l																1	
									l																	
																									1	
									I								1				1				I	

	IIW in	put bit	S						Control	output bits															1	
NAME	27	26	25	24	23	22	2 2	1 20	RFW	EXTop1	Extop0	ALUsrcB	ALUop2	ALUop1	ALUop0	PCsel1	PCsel0	RR0sel1	RR0sel0	RR1sel	WRsel	WDsel	MR	MW	input bits	output bits
									1																	
									-												-					
																					-					
									-												-					
									l																	
									1												1				I	

	IW in	put bit	:S						Control	output bits																
NAME	27	26	25	24	23	2	2 2	1 2	0 RFW	output bits EXTop1	Extop0	ALUsrcB	ALUop2	ALUop1	ALUop0	PCsel1	PCsel0	RR0sel1	RR0sel0	RR1sel	WRsel	WDsel	MR	MW	input bits	output bits
									1																	
									_																	
									-																	
									_																	
									1																	
									1																	
									-																	
									1																	
									1																	
									-																	
									-																	
									1																	
									1																	
									-																	
									1																	
									1																	
									1																	
									1												-					
									-																	
																	1				I				1	

	IW inp										out bits																
INAME	27	26	25	24	23	2	2 :	21	20 RFW	' E	EXTop1	Extop0	ALUsrcB	ALUop2	ALUop1	ALUop0	PCsel1	PCsel0	RR0sel1	RR0sel0	RR1sel	WRsel	WDsel	MR	MW	input bits	output bits