CS3281 / CS5281

I/O Devices

CS3281 / CS5281

Spring 2025

**Some lecture slides borrowed and adapted from Andrea Arpaci-Dusseau*

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Motivation

What good is a computer without any I/O devices?

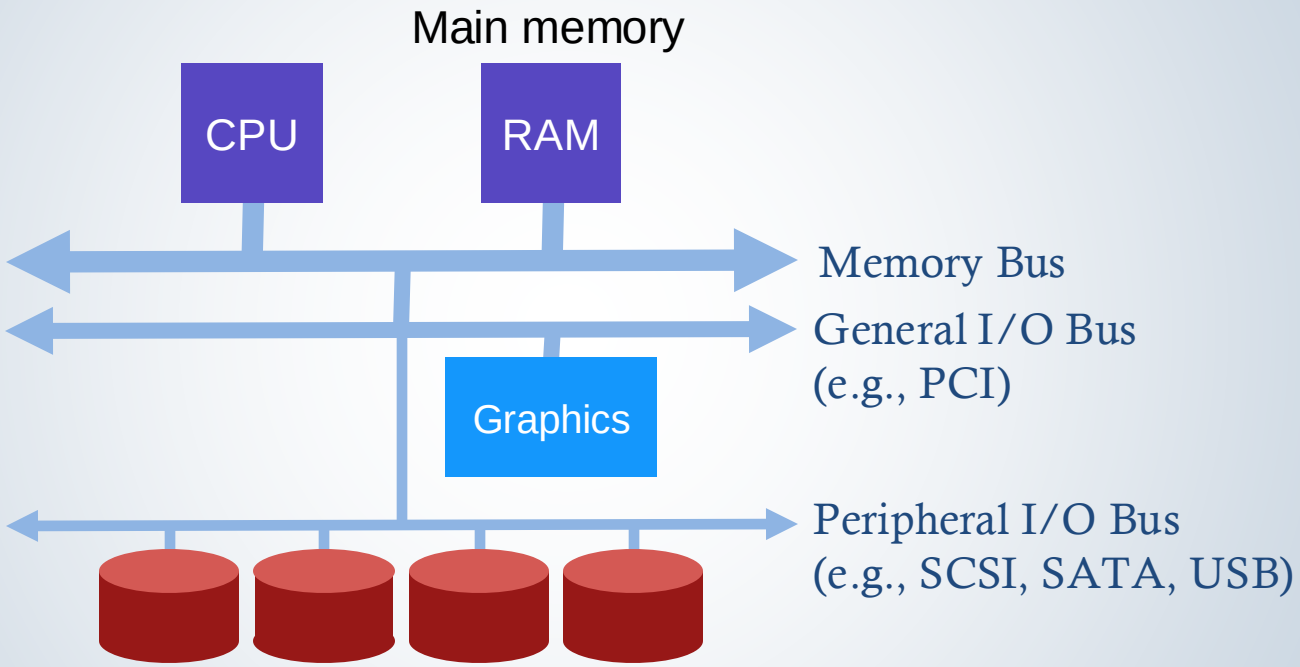
- e.g., keyboard, display, disks

We want:

- **H/W** that will let us plug in different devices
- **OS** that can interact with different combinations

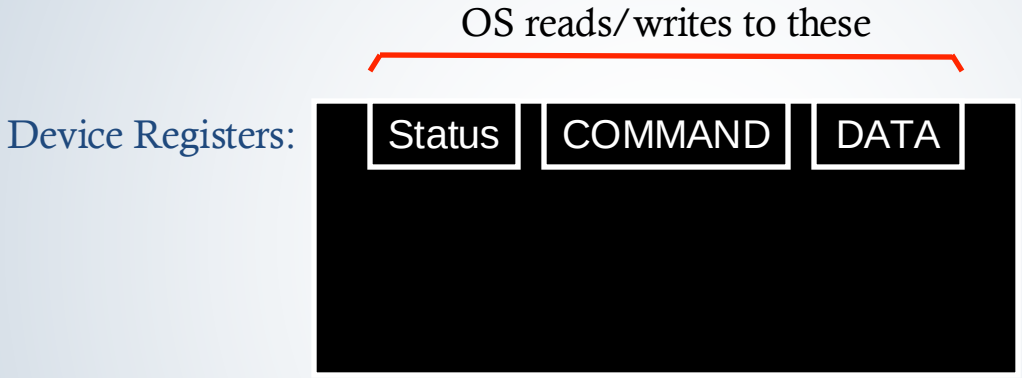
- I/O also allows for *persistence*
  - RAM is *volatile*, i.e., contents are lost when the machine restarts

Hardware support for I/O

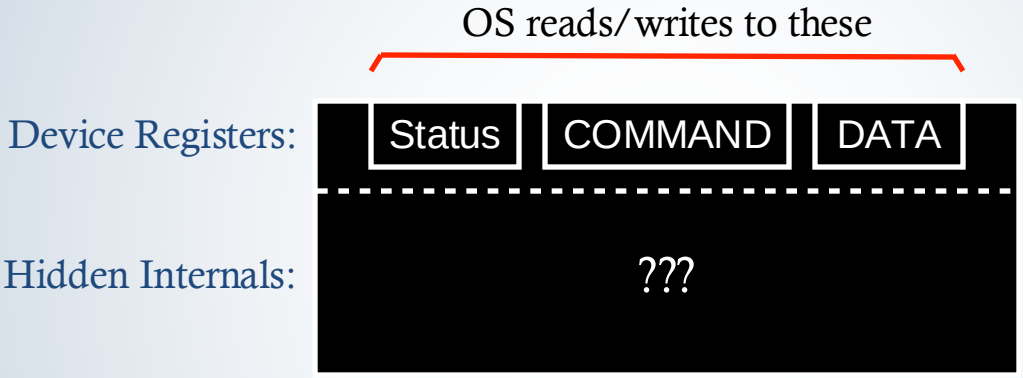


Why use hierarchical buses?

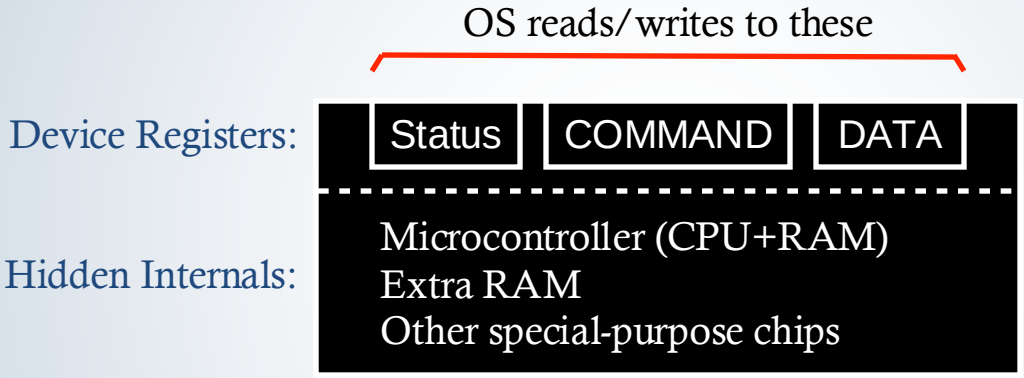
Canonical Device



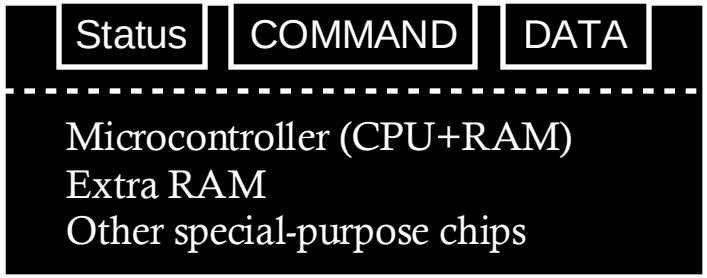
Canonical Device



Canonical Device



Example Write Protocol




```
while (STATUS == BUSY)
    ; // spin
Write data to DATA register
Write command to COMMAND register
while (STATUS == BUSY)
    ; // spin
```

This is called polling when the processor "asks" what the hardware is doing, often continuously

CPU:

Disk:

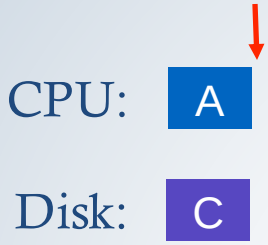
```
while (STATUS == BUSY)            // 1
    ;
Write data to DATA register       // 2
Write command to COMMAND register  // 3
while (STATUS == BUSY)            // 4
    ;
```

CPU: A

Disk: C

```
while (STATUS == BUSY)          // 1
    ;
Write data to DATA register      // 2
Write command to COMMAND register  // 3
while (STATUS == BUSY)          // 4
    ;
```

A wants to do I/O

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    ;
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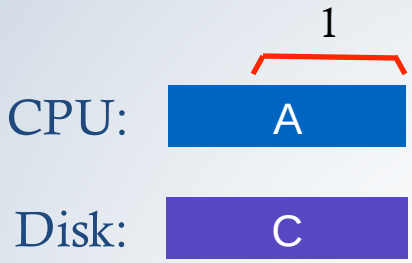


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Write data to DATA register      // 2
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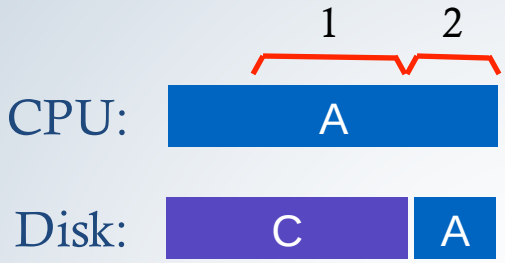
while (STATUS == BUSY)          // 4
    ;
```

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while (STATUS == BUSY)          // 1
    ;
Write data to DATA register      // 2
Write command to COMMAND register  // 3
while (STATUS == BUSY)          // 4
    ;
```

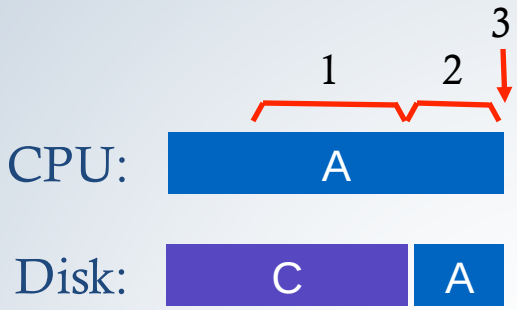


```
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Write data to DATA register      // 2
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while (STATUS == BUSY)          // 4
    ;
```
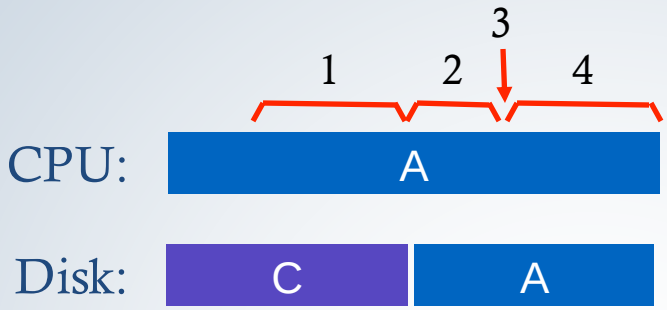
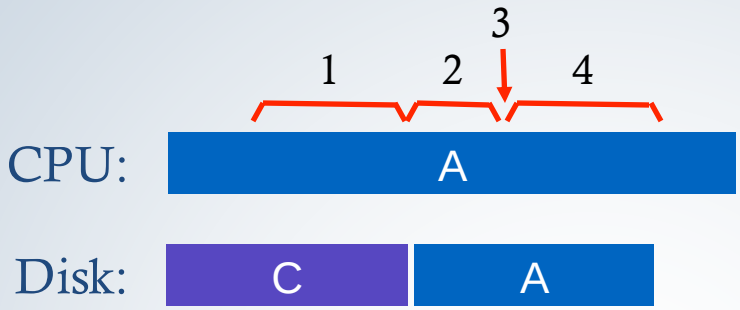
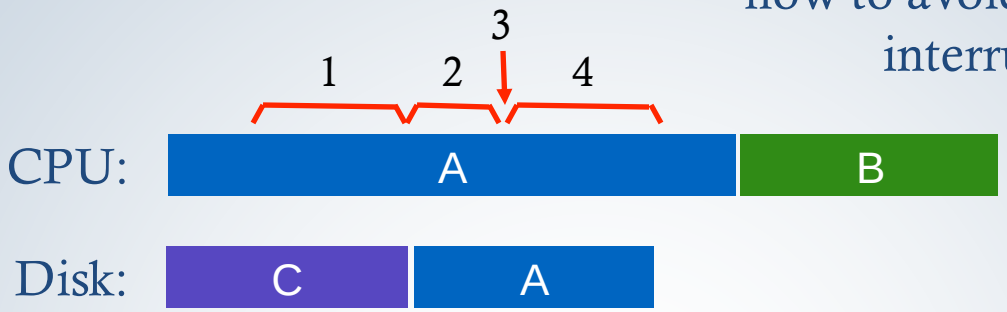




```
while (STATUS == BUSY)          // 1
    ;
Write data to DATA register      // 2
Write command to COMMAND register  // 3
while (STATUS == BUSY)          // 4
    ;
```



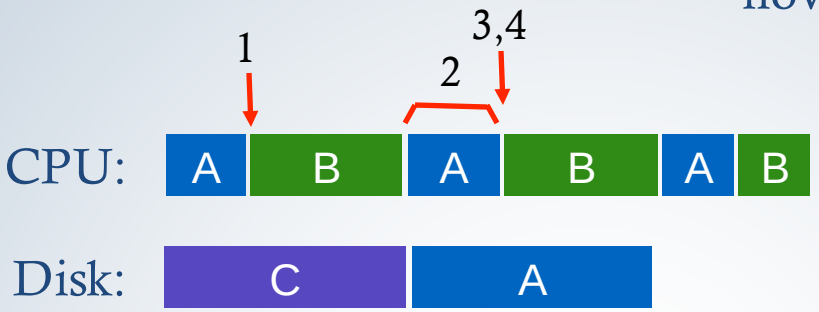

```
while (STATUS == BUSY)          // 1
    ;
Write data to DATA register      // 2
Write command to COMMAND register  // 3
while (STATUS == BUSY)          // 4
    ;
```

how to avoid spinning?
interrupts!




```
while (STATUS == BUSY)          // 1
        wait for interrupt;
Write data to DATA register      // 2
Write command to COMMAND register  // 3
while (STATUS == BUSY)          // 4
        wait for interrupt;
```

how to avoid spinning?
interrupts!




```
while (STATUS == BUSY)          // 1
    Passively wait for interrupt;
Write data to DATA register      // 2
Write command to COMMAND register  // 3
while (STATUS == BUSY)          // 4
    Passively wait for interrupt;
```

Interrupts vs. Polling

Are interrupts ever worse than polling?

Fast device: Better to spin than take interrupt and context-switching overhead

- Device time unknown? Hybrid approach (spin then use interrupts)

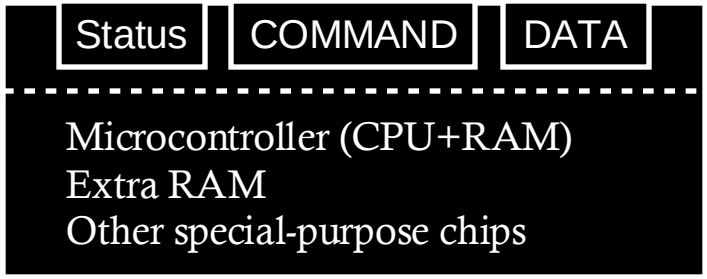
Flood of interrupts arrive

- Can lead to livelock (always handling interrupts)
- Better to ignore interrupts while making some progress handling them

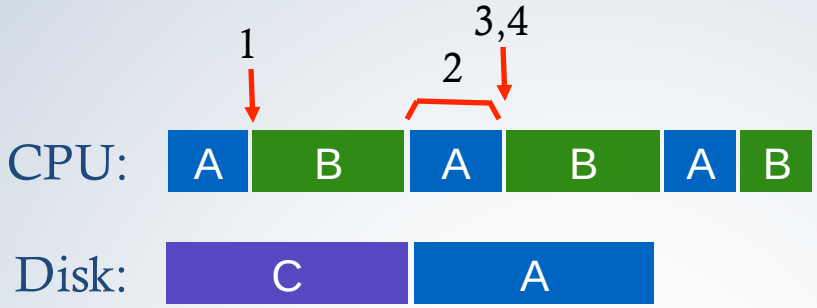
Other improvement

- Interrupt coalescing (hardware batches together several interrupts)

Protocol Variants



- **Status checks**: polling *vs.* interrupts
- **Data**: programmed I/O (PIO) *vs.* direct memory access (DMA)
- **Control**: special instructions *vs.* memory-mapped I/O




```
while (STATUS == BUSY)          // 1
        wait for interrupt;
Write data to DATA register      // 2
Write command to COMMAND register  // 3
while (STATUS == BUSY)          // 4
        wait for interrupt;
```

what else can we optimize?

data transfer!

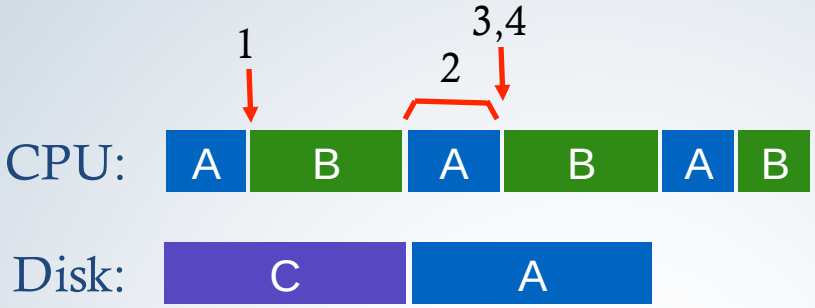
Programmed I/O vs. Direct Memory Access

PIO (Programmed I/O):

- CPU directly tells device what the data is
- Efficient for a few bytes/words, but *scales terribly*

DMA (Direct Memory Access):

- CPU leaves data in memory
- Device reads/writes data directly from/to memory
- Efficient for large data transfers




```
while (STATUS == BUSY)          // 1
        wait for interrupt;
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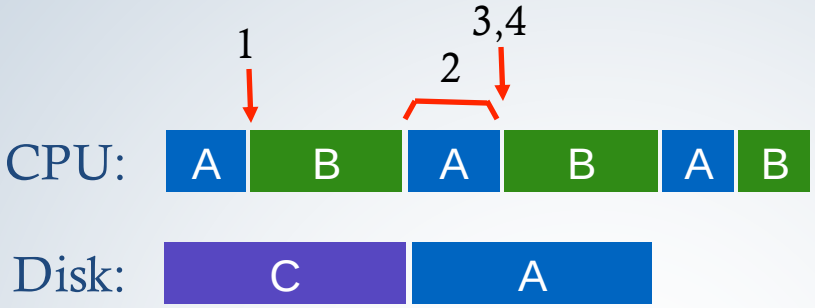


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while (STATUS == BUSY)          // 1
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        wait for interrupt;
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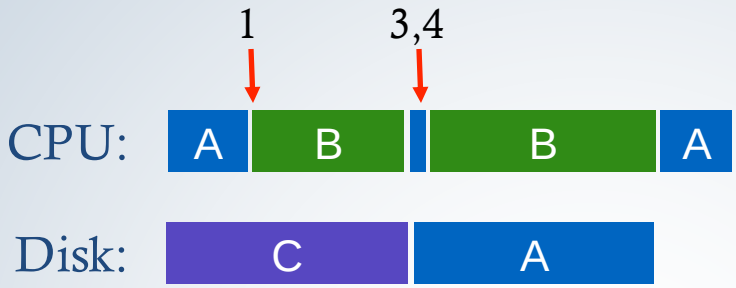
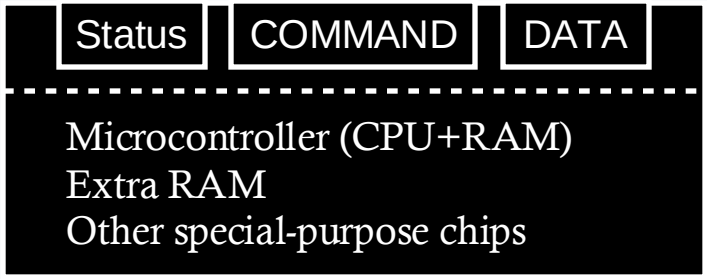



```
while (STATUS == BUSY)          // 1
        wait for interrupt;
~~Write data to DATA register      // 2~~
Write command to COMMAND register  // 3
while (STATUS == BUSY)          // 4
        wait for interrupt;
```

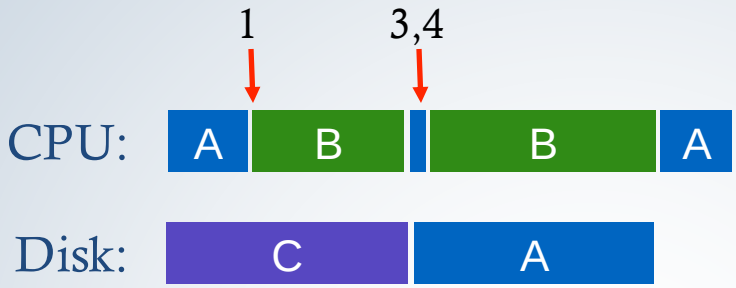
Protocol Variants



Status checks: polling *vs.* interrupts

Data: PIO *vs.* DMA

Control: special instructions *vs.* memory-mapped I/O

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while (STATUS == BUSY)          // 1
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```
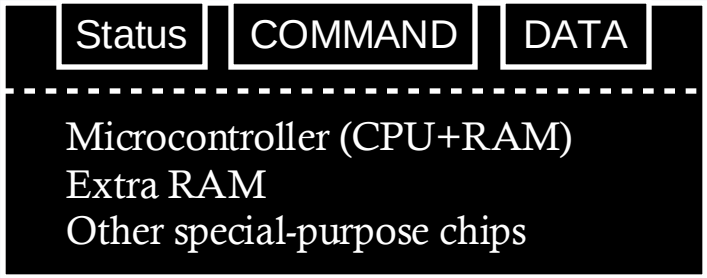

how does OS read and write registers?

Protocol Variants



Status checks: polling *vs.* interrupts

Data: PIO *vs.* DMA

Control: special instructions *vs.* memory-mapped I/O

Special Instructions vs. Memory-Mapped I/O

Special instructions

- each device has a port
- in/out instructions (x86) communicate with device

Memory-Mapped I/O

- H/W maps registers into the virtual address space
- loads/stores sent to device

Doesn't matter much (both are used)