CS 4110

Programming Languages & Logics

Lecture 32
Shared-Memory Parallelism

IMP with Parallel Composition

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$$
\begin{array}{rcl}
a & ::= & x \mid n \mid a_1 + a_2 \\
b & ::= & \textbf{true} \mid \textbf{false} \mid a_1 < a_2 \\
c & ::= & \textbf{skip} \mid x := a \mid c_1; c_2 \mid \textbf{if } b \textbf{ then } c_1 \textbf{ else } c_2 \mid \textbf{while } b \textbf{ do } c \\
 & & \mid \; c_1 \mid\mid c_2
\end{array}
$$

Operational Semantics

And add small-step operational semantics rules for $c_1 \mid\mid c_2$ that interleave the execution of c_1 and c_2:

$$\frac{\langle \sigma, c_1 \rangle \rightarrow \langle \sigma', c_1' \rangle}{\langle \sigma, c_1 \mid\mid c_2 \rangle \rightarrow \langle \sigma', c_1' \mid\mid c_2 \rangle}$$

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$$\langle \sigma, \textbf{skip} \mid\mid \textbf{skip} \rangle \to \langle \sigma, \textbf{skip} \rangle$$

The rules allow either sub-command to take a step; two sub-commands can interleave read and write operations involving the same store.

Parallel Bank Account

What happens if we deposit into a bank account twice under parallel composition?

$$\begin{array}{l}\mathsf{bal} := 0; \\ (\mathsf{bal} := \mathsf{bal} + 21.0 \quad || \;\; \mathsf{bal} := \mathsf{bal} + 21.0)\end{array}$$

Synchronization

Languages have synchronization constructs that control the interactions between threads.

Many languages have mutual exclusion, a.k.a. *locking:*

```
**lock** $l$;
bal $:=$ bal $+ 21.0$;
**unlock** $l$
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```

A well-behaved alternative is transactional memory:

```
transaction $\{$
    bal $:=$ bal $+ 21.0$
$\}$
```

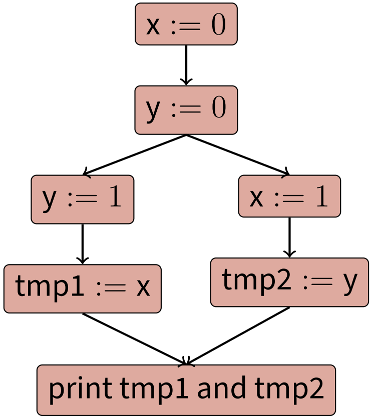
Reasoning About Shared Memory

This program reads and writes two shared variables from two different “threads”:

$$\begin{array}{l} \mathsf{x} := 0; \mathsf{y} := 0; \\ (\mathsf{y} := 1; \mathsf{tmp1} := \mathsf{x}) \quad || \\ (\mathsf{x} := 1; \mathsf{tmp2} := \mathsf{y}) \end{array}$$

What can tmp1 and tmp2 be afterward?

Ordering Operations



Happens Before

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See also Lamport, 1978: “Time, Clocks and the Ordering of Events in a Distributed System.”

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Operation a happens before b, written $a \to b$, iff:

- a and b belong to the same thread and a comes before b in a single-threaded execution, or
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(Also add transitivity: if $a \rightarrow b$ and $b \rightarrow c$, then $a \rightarrow c$.)

See also Lamport, 1978: “Time, Clocks and the Ordering of Events in a Distributed System.”

Happens Before

In modern multithreaded programming, messages are sent and received at *synchronization* events:

- unlock $l \rightarrow$ lock l
- fork $t \rightarrow$ first operation in thread t
- last operation in thread $t \rightarrow$ join t

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Model an execution as a total order $a \rightarrow_e b$ on the same set of events. For example:

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\boxed{\mathsf{y} := 1} \arrow[r] & \boxed{\mathsf{tmp1} := \mathsf{x}} \arrow[r] & \boxed{\mathsf{x} := 1} \arrow[r] & \boxed{\mathsf{tmp2} := \mathsf{y}}
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Intuitively, $\rightarrow_e$ is an *interleaving* that obeys $\rightarrow$.

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To see what a parallel program can do, we can enumerate all the SC executions and “run” them:

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  $\Longrightarrow \mathsf{tmp1} \mapsto 1, \mathsf{tmp2} \mapsto 0$

Legal Executions

Enumerating SC executions gets old fast, but lets us produce the set of possible final stores, σ:

$\{\text{tmp1} \mapsto 0, \text{tmp2} \mapsto 1\}$
$\{\text{tmp1} \mapsto 1, \text{tmp2} \mapsto 1\}$
$\{\text{tmp1} \mapsto 1, \text{tmp2} \mapsto 0\}$

So no sequentially consitent execution makes both tmp1 and tmp2 equal to zero.

That Same Program, in C

```c
volatile int x, y, tmp1, tmp2;

// Thread 0: write x and read y.
void *t0(void *arg) {
  x = 1;
  tmp1 = y;
  return 0;
}

// Thread 1, the opposite: write y and read x.
void *t1(void *arg) {
  y = 1;
  tmp2 = x;
  return 0;
}
```

That Same Program, in C

```
void main() {
  x = y = tmp1 = tmp2 = 0;

  // Launch both threads.
  pthread_t thread0, thread1;
  pthread_create(&thread0, NULL, t0, NULL);
  pthread_create(&thread1, NULL, t1, NULL);

  // Wait for both threads to finish.
  pthread_join(thread0, NULL);
  pthread_join(thread1, NULL);

  printf("%d %d\n", tmp1, tmp2);
}
```

Weak Memory Models

No real parallel machine enforces sequential consistency!

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There are many reasons and/or excuses:

- Per-processor caching lets each CPU read values that other processors can’t see yet.
- Private write buffers are critical for good performance with coherent caches.
- Lots of “obvious” compiler optimizations violate sequential consistency.

See also Boehm, 2005: “Threads cannot be implemented as a library.”

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Every machine (and every programming language) as a memory model. Memory models describe the set of legal executions.

Sequential consistency is the *strongest* memory model out there: it allows the fewest different executions.

Real machines and languages have *weaker* memory models:

$$\text{SC} \geq \text{x86} \geq \text{ARM} \geq \text{C/C++} \geq \text{DRF0}$$

Data Races

A data race occurs when:

- There are two events a and b that are unordered in the happens-before relation ($a \nrightarrow b$ and $b \nrightarrow a$),
- both events access the same shared variable, and
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Our little example has *two* data races: one on x and one on y.

Data Races & Memory Models

Languages have recently agreed on one critical property:

$$\text{data race free} \Rightarrow \text{sequentially consistent}$$

As long as you avoid data races, you get sequential consistency on *any* machine in Java, C, and C++.

(In jargon: the *DRF implies SC* theorem.)

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(In jargon: the *DRF implies SC* theorem.)

Languages still disagree about what happens when you *do* have a race. In C and C++, races allow undefined behavior.

Race-Free Programming

Data race detection is an active field of research.

One called ThreadSanitizer is included with recent Clang and GCC compilers:

```
$ cc -g -fsanitize=thread simple_race.c
$ ./a.out
WARNING: ThreadSanitizer: data race (pid=26327)
  Write of size 4 at 0x7f89554701d0 by thread T1:
    #0 Thread1(void*) simple_race.cc:8

  Previous write of size 4 at 0x7f89554701d0 by thread 
    #0 Thread2(void*) simple_race.cc:13
```