EECS 3216 LAB-2
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LAB NUMBER:02

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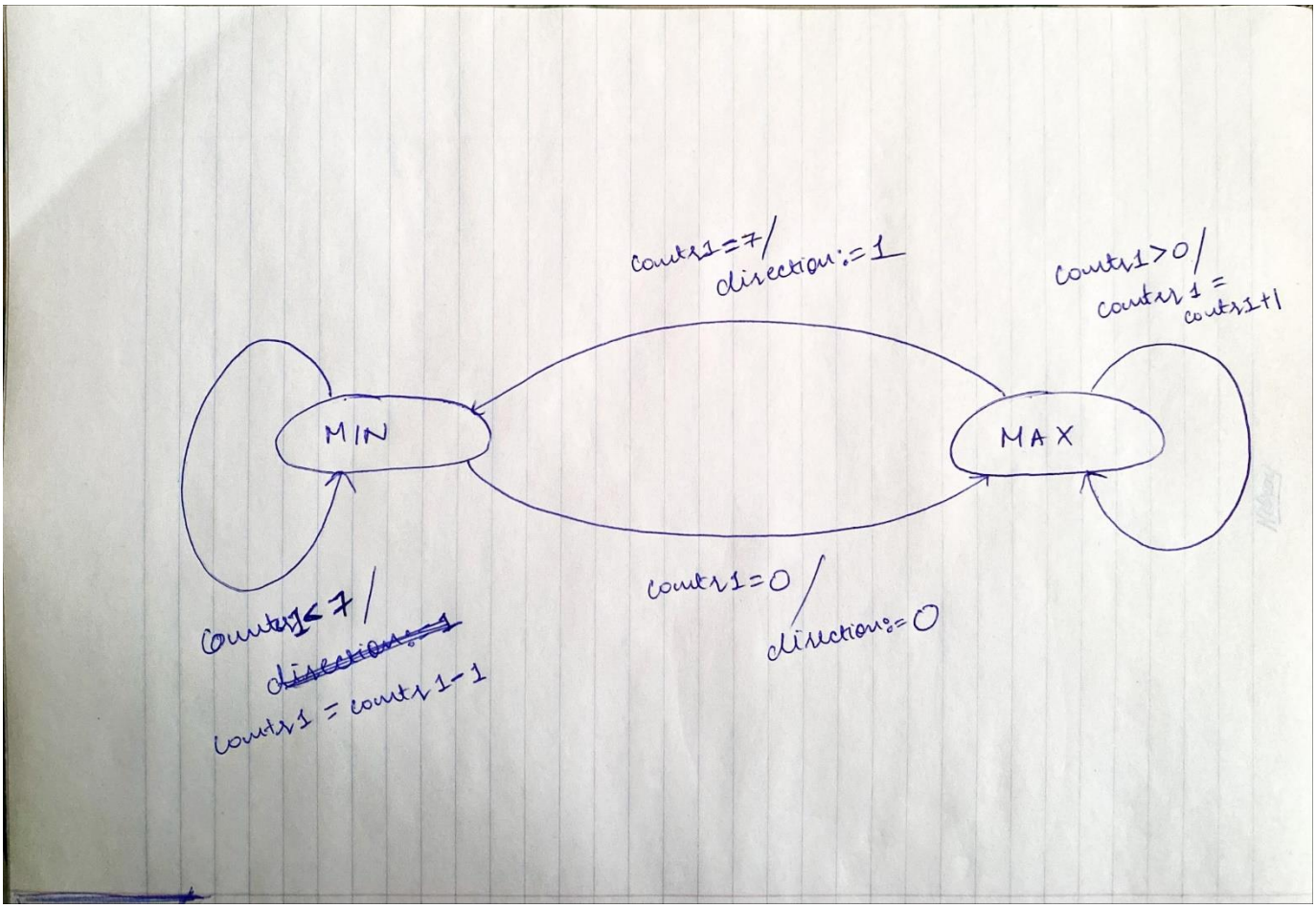
Design

B)

As a clock divider slows down the clock, I used that for slowing down the cycles of original clock 50MHz to 1Hz. Then I used a counter that goes from 0 to 25000 to divide 50,000,000 into 1 cycles. When the counter reaches 0 , I increment or decrement another counter (Counter 1) based on the direction variable . On every posedge of the clock cycle I check if the counter 1 is 7 or 0 and change direction variable according to that.

FSM



Verilog Code

C)

```
module Lab1(clk,ledo);
input clk;
reg clkout;
output [3:0] ledo;


reg[31:0] counter = 32'd0 ;
parameter frequency = 32'd50000000 ;
reg[3:0] counter1 = 4'd0 ;
reg value = 1'd0 ;
reg direction = 1'd0 ;

always @(posedge clk)
begin
        counter <= counter + 32'd1;
        if (counter >= frequency - 1)
        begin
                counter <= 32'd0;
        end
        if (counter == 25000000)
        begin
                if (direction == 0)
                begin
                        counter1 <= counter1 + 4'd1;
                end
                if (direction == 1)
                begin
                        counter1 <= counter1 - 4'd1;
                end
        end
        if (counter1 >= 4'd7)
        begin
                direction <= 1'b1;
        end
        if (counter1 <= 4'd0)
        begin
                direction <= 1'b0;
        end
end



assign ledo = counter1;

endmodule
```

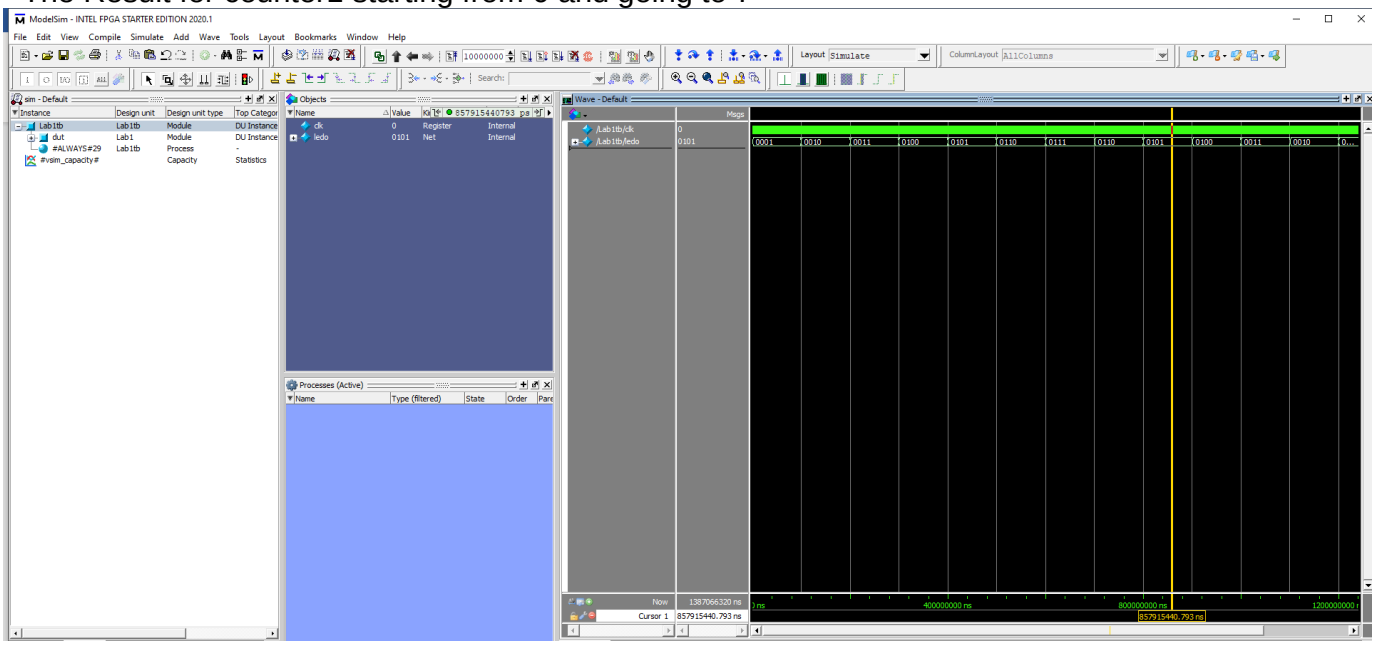
Test Bench Verilog Code

C)

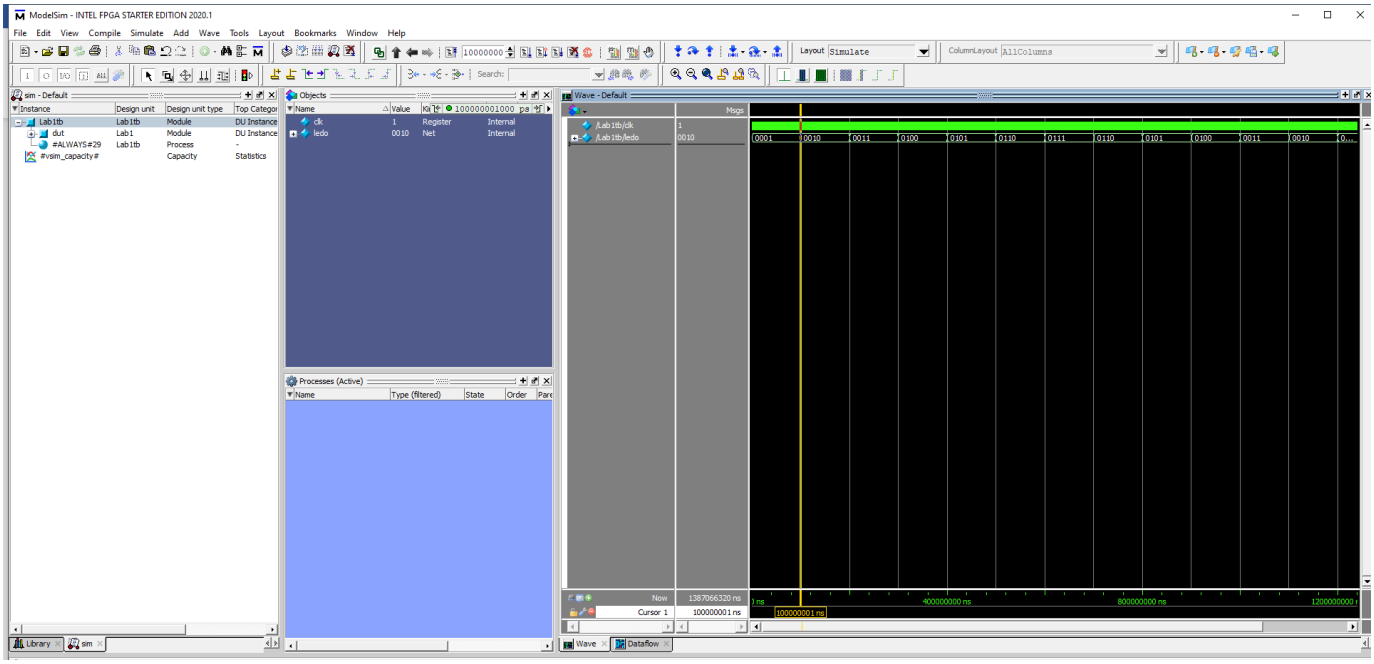
```
`timescale 1 ns/1 ps

module Lab1tb();

reg clk;
wire [3:0] ledo;



Lab1 dut(.clk(clk),.ledo(ledo));

always
begin
clk = 1'b1;
#10;
clk = 1'b0;
#10;
end
endmodule
```

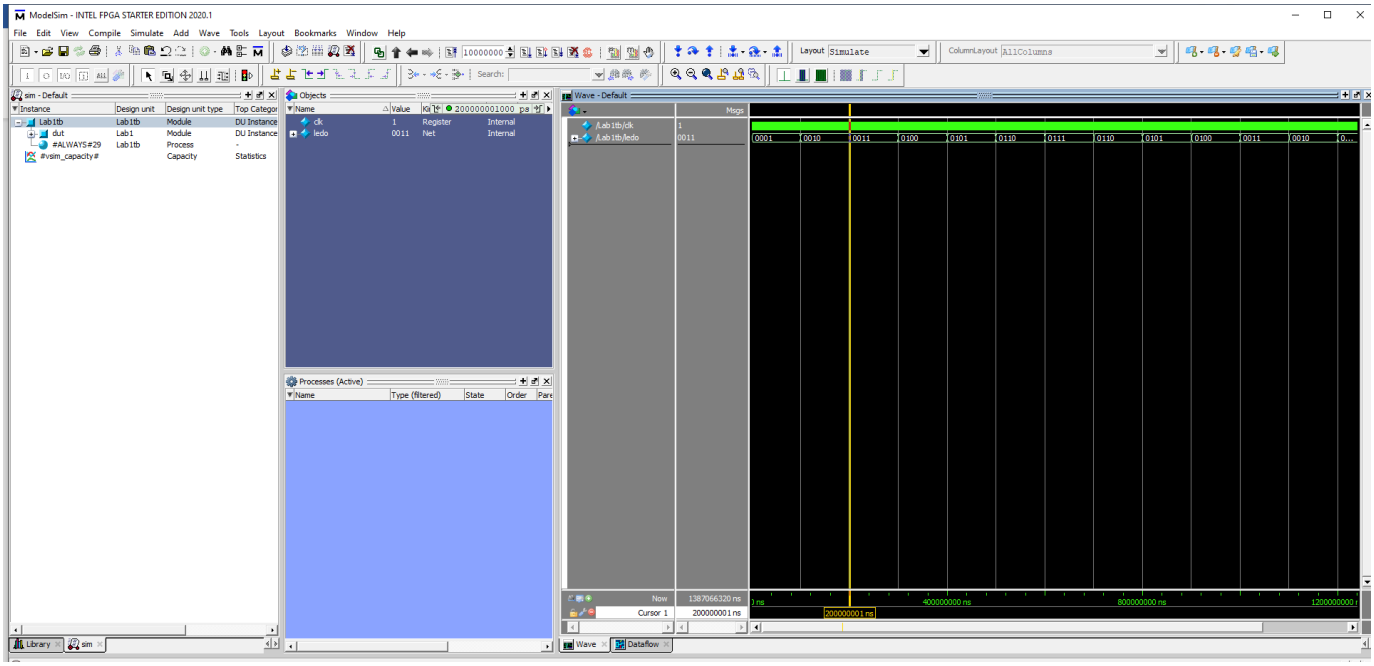
Model-Sim Results

The Result for counter1 starting from 0 and going to 7

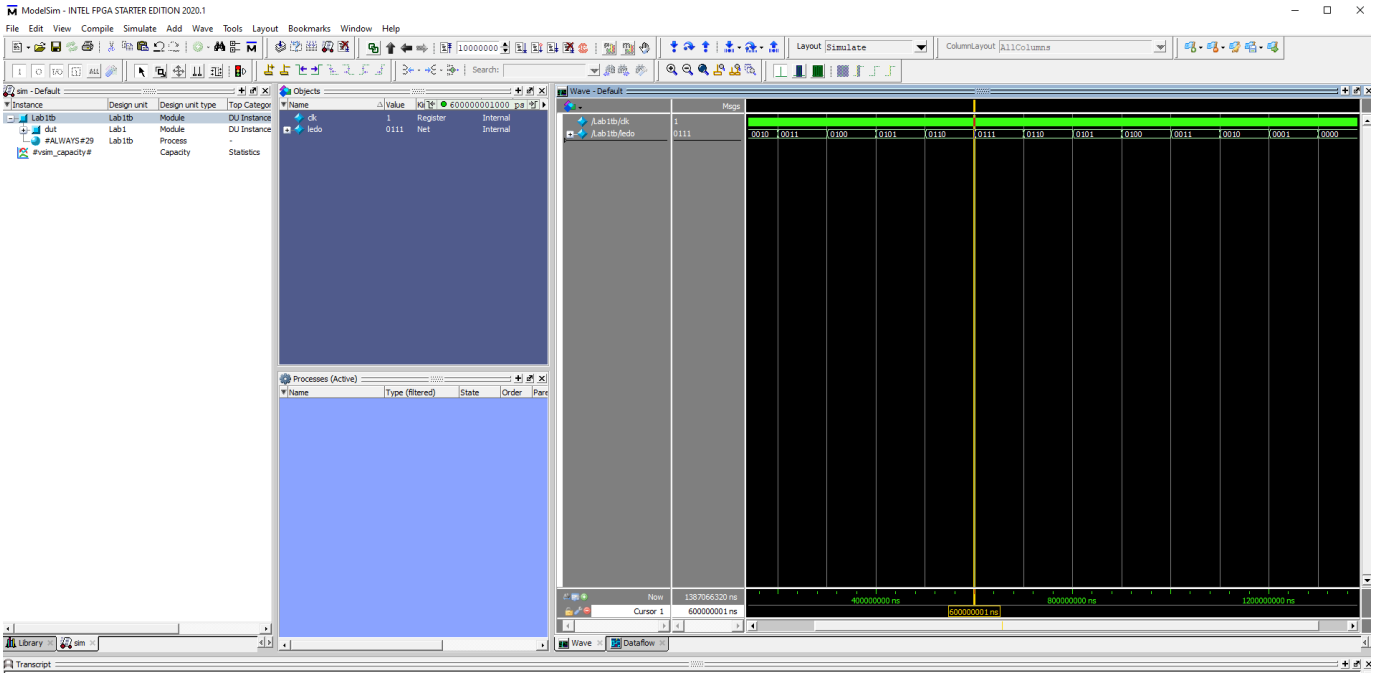


Counter changes every 1 second





Led count goes from 7 to 0 again


ModelSim - INTEL FPGA STARTER EDITION 2020.1
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
sim - Default
Instance
Design unit
Design unit type
Top Categor
Lab1tb
Lab1tb
Module
DU Instance
dut
Lab1
Module
DU Instance
#ALWAYS#29
Lab1tb
Process
#vsim_capacity#
Capacity
Statistics
Objects
Name
Value
Register
Internal
clk
1
Net
Internal
ledo
0111
Processes (Active)
Type (filtered)
State
Order
Wave - Default
/Lab1tb/clk
/Lab1tb/ledo
0010
0011
0100
0101
0110
0111
0110
0101
0100
0011
0010
0001
0000
Now
1387066320 ns
Cursor 1
600000001 ns
400000000 ns
800000000 ns
1200000000 ns
Library
sim
Wave
Dataflow
Transcript