STATE MACHINE name clock reset_signal reset_state default_state_is_x INPUTS CLK RST WCNT[2:0] EVNCNT[3:0] ODDCNT[3:0]	DSR_align CLK RST Start 1	posedge posedge
OUTPUTS		
ALIGNED	0	comb
WRST	0	comb
WINC	0	comb
BIT_SLIP_EVN	0	comb
BIT_SLIP_ODD	0	comb
STATES		
ALIGNED	0	output
WRST	0	output
WINC	0	output
BIT_SLIP_EVN	0	output
BIT_SLIP_ODD	0	output
TRANSITIONS		
equation	1	def_type
priority	1000	

