STATE MACHINE
  name   DAQ_Rate_Sel_FSM
  clock   CLK   posedge
  reset_signal   RST   posedge
  reset_state   ST_3_2_GBPS
  default_state_is_x   1
  stateout   DQRT_STATE
INPUTS
  CLK
  RST
  DAQ_RATE
  TXRATEDONE
  CNT[3:0]
  CDV_DONE
OUTPUTS
  CLR_CNT   0   regdp
  INC_CNT   0   regdp
  CLK_SEL[2:0]   3'b001   regdp
  RATE_SEL[1:0]   2'b11   regdp
  WRDCLKSEL   1   regdp
  CDV_INIT   0   regdp
  PCSRST   0   regdp
  RATE_3_2   0   regdp
  RATE_1_25   0   regdp
STATES
  CLR_CNT   0   output
  INC_CNT   0   output
  CLK_SEL[2:0]   3'b001   output
  RATE_SEL[1:0]   2'b11   output
  WRDCLKSEL   1   output
  CDV_INIT   0   output
  PCSRST   0   output
  RATE_3_2   0   output
  RATE_1_25   0   output
TRANSITIONS
  equation   1   def_type
  priority   1000