STATE MACHINE

name	Frame_Proc_FSM	
clock	CLK	posedge
reset_signal	RST	posedge
reset_state	Idle	
default_state_is_x	1	
stateout	FRM_STATE	

INPUTS

- CLK
- RST
- VALID
- ROM_ADDR[2:0]

OUTPUTS

INC_ROM	0	comb
RST_ROM	0	regdp
CRC_CALC	0	comb
CRC_VLD	0	comb
CLR_CRC	0	regdp
TX_ACK	0	regdp

STATES

INC_ROM	0	output
RST_ROM	0	output
CRC_CALC	0	output
CRC_VLD	0	output
CLR_CRC	0	output
TX_ACK	0	output

TRANSITIONS

equation	1	def_type
priority	1000	
CRC_VLD		output
INC_ROM		output