name	Pipe_Start_FSM	
clock	CLK	posedge
reset_signal	RST	posedge
reset_state	Idle	
default_state_is_x	1	
INPUTS		
CLK		
RST		
WCNT[8:0]		
HOLD[1:0]		
PDEPTH[8:0]		
RESTART		
OUTPUTS		
PIP_RST	0	comb
WE	0	comb
RE	0	comb
INC_H	0	comb
STATES		
PIP_RST	0	output
WE	0	output
RE	0	output
INC_H	0	output
TRANSITIONS		
equation	1	def_type
priority	1000	

STATE MACHINE

