STATE MACHINE

name	dyn_phase_shift_FSM	
clock	CLK	posedge
reset_signal	RST	posedge
reset_state	Idle	anyvalue
default_state_is_x	1	
stateout	DYN_PHS_STATE	

INPUTS

- CLK
- RST
- LOCKED
- PH_CHANGE
- PS_DONE

OUTPUTS

PSEN	0	regdp
BUSY	0	regdp

STATES

PSEN	0	output
BUSY	0	output

TRANSITIONS

equation	1	def_type
priority	1000