STATE MACHINE		
name	tx_sync_FSM	
clock	CLK	posedge
reset_signal	RST	posedge
reset_state	Idle	
default_state_is_x	1	
SYNC_CNT	8192	parameter
INPUTS		
CLK		
RST		
OUTPUTS		
TXDLYALIGNRESET	0	regdp
TXENPMAPHASEALIGN	0	regdp
TXPMASETPHASE	0	regdp
SYNC_DONE	0	regdp
acnt[4:0]	5'h00	regdp
wcnt[5:0]	6'h00	regdp
scnt[15:0]	16'h0000	regdp
STATES		
TXDLYALIGNRESET	0	output
TXENPMAPHASEALIGN	0	output
TXPMASETPHASE	0	output
SYNC_DONE	0	output
acnt[4:0]	5'h00	output
wcnt[5:0]	6'h00	output
scnt[15:0]	16'h0000	output
TRANSITIONS		
equation	1	def_type
priority	1000