STATE MACHINE name clock reset_signal reset_state default_state_is_x INPUTS CLK RST READY MT	GBT_FIFO_readout_FSM CLK RST Idle 1	posedge posedge
OUTPUTS RD EN	0	regdp
hold[3:0]	4'h0	regdp
STATES		
RD_EN	0	output
hold[3:0]	4'h0	output
TRANSITIONS equation	1	def type
priority	1000	uei_type
priority	1000	

