STATE MACHINE
    name   Pow_on_Rst_FSM
    clock   CLK   posedge
    reset_signal   EOS   negedge
    reset_state   Idle   anyvalue
    default_state_is_x 1
    POR_tmo   120   parameter
    Strt_dly   20'h7FFFF   parameter
INPUTS
    QPLL_LOCK
    MMCM_LOCK
    EOS
    CLK
OUTPUTS
    POR   0   regdp
    MMCM_RST   0   regdp
    RUN   0   regdp
    por_cnt[6:0]   7'h00   regdp
    strtup_cnt[19:0]   20'h00000   regdp
STATES
    POR   0   output
    MMCM_RST   0   output
    RUN   0   output
    por_cnt[6:0]   7'h00   output
    strtup_cnt[19:0]   20'h00000   output
TRANSITIONS
    equation   1   def_type
    priority   1000

Idle
POR <= 1
MMCM_RST <= 1
strtup_cnt[19:0] <= strtup_cnt + 1

strtup_cnt == Strt_dly

W4SysClk
POR <= 1

MMCM_LOCK

Pow_on_Rst
POR <= 1
por_cnt[6:0] <= por_cnt + 1

!MMCM_LOCK

por_cnt == POR_tmo

Run_State
RUN <= 1