DDU5CTRL (file 0dductrl)

6-19-2009_14:34

CF048A01 Version 48

CMS CSC DDU5, Central Control FPGA

v40: DMB & Trig.CRCs use MUX to load Zeroes (not Tbufs), change DDUfb reset
-r2: add time constraint to DDUFB reg to eliminate DDUCRC logic lag. r3: tune BuffOvfl & EthLim logic
v41: SCA_Ovfl separated from DMB_Err & SomethingBad. r2: tune KillFiber glitch
v42: change to proposed format for ALCT; r2: FOV=6, on TFsig kill ALCT/TMBerr, correct SBXN for 3564-4096 difference in BX<40 case (from CloseL1A logic) r3: change to new ALCT/TMB data format; r4: fix TRG bugs in stage2 r5: reduce RST logic delays, may have caused TrgTrail detect problems
added bit usage notes in FIFOCTRL, 27nov2007 v43: tune CMD Strobe timing; r2, adjust TMB/ALCT Fful bits r3: fixed bug in TrgL1err reporting. v44: change TF-DDU definition (0xc0 in Flash-Page7)
v45: tune TrigTrailProb, CfebCntErr logic, add CSC RepeatErr logic to LsumErr reg & take it to JTAG F35
r2: remove DMBwarn from FMMwarn logic. r3: add vote3 for DDUCRC r4: remove CRC voting, delay S-Link clock by 3.2ns
v46: tests ck156, SLink clk from DCM --> SLink. r2: shift OWCLK by +3.2ns
v47: move ROD pipe reg. into stage2 before DDUCRC
v48: GbE skips Empty Events for Global runs

Set All I/O to 3.3V

PART=XC2VP7-6-FF672

PROM=2*XC18V04-VQ44 (PARALLEL)

DDU5ctrl\DDU5ctrl\ddu5ctrl
C045DD99
C145DD99

DDUCNTRL

PromID: 05026093h
FPGAid: 2124A093h

PROGRAM takes < 55 ms (31ms this FPGA)

1: Mode Bit 0 LED0 on top, pins on away-side from LEDs
2: Mode Bit 1 RST_1=Asynchronus Reset for FPGA1 and ALL FP
3: Mode Bit 2
4: Mode Bit 3
5: Mode Bit 4; High for GBE debug, Low otherwise
6: GbE test, send counter on GBE link
7: Set L1A Fake mode, Kill TTC L1A/BXR/ECR if SW8 is off
8: FPGA version on LEDs

ELECTRONICS LAB
PHYSICS DEPARTMENT
THE OHIO STATE UNIVERSITY
174 WEST 18TH AVE
COLUMBUS OHIO 43210

DDU Format Since DDUctrl v15:

BOE1 type L1A Number BXN ID FOV K-Status
H1: 0x/5T/NN.NNNN/XXX/I.II/VK
49-bit ~unique constant DMBfull(15)
H2: 0x/8000/0001/8000/HHHH
LiveDMB(15) Ostat DMB-DAV(15) BOEstat DMBcnt
H3: 0x/LLLL/0000/ZZZZ/GGMY

64-bit unique constant
T-2: 0x/8000/FFFF/8000/8000
DDU EOE Status DMBerr DMBwarn(15)
T-1: 0x/SSSS.SSSS/QQQQ/PPPP
EOE WordCount CRCword EOEstat K-Status
TR: 0x/A/?/WW.WWWW/RRRR/UUMK

DDU WordCount (64-bit words) for "No Data" event: 0x006.
DDU WordCount for one DMB (only one CFEB): 0D2h = 210 dec, 1680 Bytes
DDU WC, 1 DMB with 2 CFEB (8 samples each): 19Ah = 410 dec, 3280 Bytes
DDU WC, 2 DMB with 1 CFEB (nCFEB=2): 19Eh = 414 dec, 3312 Bytes
DDU WC, 2 DMB with 2 CFEB (nCFEB=4): 32Eh = 814 dec, 6512 Bytes
DDU_WordCount = (6 + 25*Nts*nCFEB + 4*nDMB) < 30070; 240560 Bytes
^^Ignores TMB Data^^ GBE_ByteCount = 8*DDU_WordCount 8 TS assumed

mojo

DDU5CTRL -- Project History

v1-2: from ddu4ctrl_v28, FIFO Full JTAG Reg is 16-bits
Last w/DDU_FOV=4 --->> v10-12: Add RCLK1, Tune OutUnit GT resets, tune DCC_WAIT modes & add Klll option
v13-14: Fix LVT/LVA, kill DMB-CFEB-Sync, bring DMB Results to CRCerr; tune DMB checks, GbE Prescale & SLinkWtEn from VMEctrl
v15-16: fix DMBwarn, add VME_FakeL1enable; put DMBLIVE[14:0] in HDR3; put DMBwarn/err in TR-1, Tune TRG_Trail_Err resets, FOV=5
v17-18: tune DMB_Full, RST_InStat, EndTimeRST, PRST, add InRD-C-Code JTAG path (F20), GbE Packets now 7952 bytes
v19: Require SLinkWaitEn for CFEB_L1err check; v20: set RCLK0 to FAST24, CkFB to SLOW6--->rev2: SLOW8
v21: add C-code-err Begin/End to JTAG F20, set CLK40-0 to FAST16, DMBliveErr & In_Time_Out go to BOE_Stat
v22: add DMBLIVE reg's on F25/26, CLK40-1 is FAST16, L1A uses OFD_1; rev2: CLK40's use F16-OFDDR
Good! rev3: tune PDMBLIVE_EN & RST_STRT logic v23: add KillCFEBchecks & require FKILL15 to EnableCheckDisable,
Good! v24: tune DMBlive timing (yellow FMM), bring signals to LEDm10/LA0/1
v25: tune L1err & InFerr "DMBliveOK", fix TTMB_Err, tune RstBOE, check CFEB L1A only on 1st sample (not critical)
v26: BXorbit=3563 now, add IDMB_FULL flag on ERB. v27: tune CFEB_L1er, 8/16 sample flag, WarnMon & BX offset
v28: add Big debug reg. on F21, Timeout reg. on F28 use LnextFIFO, replace LLLREN w/LFOE for TimeoutReg,
make ERA-St/End-TO perm. . v29: fix Mult.L1Err logic, add InSingWarn/InML1Err, tune DDUsyncErr, L1A-fake kills TTC-L1A
v30: tune Critical Error, InRdWarn, SpyOvfl & LextStop logic
v31: tune CFEB-DAV check (OR DAVs from DMB Hdr1 & Hdr2), add SP/TF compatibility & diagnostic logic
v32: change CfebCalDisable default to True, remove DDU_DLL_Err from FMMerr (InRdErr4), modified ERB13 for perm DDU_DLL_err,
add DDU CSC-Board occupancy monitor-F34? r2: add zeroing logic at RST for Occ.Mon. -r3: fix LRST logic
v33: change SourceID=760=2F8h for TF-DDU v34: Inverted CCB_CMD bus & L1A **for TF-DDU ONLY!**
v35: Autodetects TF-DDU, now compatible w/wo TF; add SyncHold & CloseL1A logic; r2, removed redundant
RdyIn2 requirement for SEN bits. r3-4, OSyncRst on ~Clk40, tune OFIFO Mon, req. VMEctrv17+ & InCtrlv22r3+
v36: non-TF DDUs have SrcID==BrdID, NoLiveFibers now readout on L1A. r2: change TF_SIG to FDRE, Reset CheckCRC with NewTFDMB
v37: diagnostic changes....Tune DMBL1err(notALCTerr), BadCtrl(notMissTrg), LIE(addMissTrg),
DMB/TMB/ALCTerr account for MissTrgTrail, DMB-to on Era15, XtraTrgTrails on Erc5+13,DDUfmm 3-bits held Reset until SystemRdy
v37r2-3: tune CfebL1aErr/SyncErr &DMBcritErr logic, MultL1err logic, InSingWarn=Era10,ValidDMBfull=Erb0,DMBtimeout=Era15
v38: DMBcritErr=Erc7, improve Htmb/alct timing,C-codeErr goes to InMxmitReg, InTimeout goes to EndTimeBusyReg
r2: make DAQovfl for FF case only, include C-CodeErr w/MultXmitErr, CFEBcrc flags Reset on BOE, C-code-L1er=FIFOb15,
LDMB_CRCok held at least 4 cycles
r3: add DMB-TO/FIFOfull to TMB/ALCTerr Regs, adjust their time to L2DMBrd; TrgWC only Comp 8 bits, A-T-Switch Req. NoSpwdErr
r4: fix LWCb8 Reset logic for long ALCT case (still not inc. in WC check though)
v39: 64bit_err reset on BOE, TrgWC now uses all 9 bits, CloseL1A range now 1usec, BIG L1Afifo w/better Warn/Busy Logic
r2: add hysteresis for L1A_AF/Busy state, tune DAQovfl logic, tune SysRdy/BUSY logic. r3: tune L1pipe/StuckData logic
-r4: tune CRC_Cnt_Err monitor logic; r5: tune SCAovfl Reset & CountSample timing

To Do:

- COMPARE BXN (DMB/TMB too)
- Watch for TRG buff overflows
- Determine correct values to store in Flash Mem
  ---> BX offset, KillCh's, FIFO thresh, Board ID
- Test DCC/SlinkWait feedback function & thresh's
  ---> Make DMB stop too
- Verify that CFEB-CRC is fixed for B-code case
- No logic for BUS1, DCC SBDATA & TDxxx, 4 LSF, 4 LRL
- Make Verilog module to get Fiber/DMB_RD in one CLK?
- Multiple TRG_L1err ought to request a Sync Reset?
  * Same for consecutive events with a TRG_L1err?

Check Phase of CMD to CLK40
  * pg. 2G & 3I
- CFEB-DMB sync check pg. 12C
- CFEB-L1A check disabled, pg. 12D: not! Found a fix.
- options for Monitoring on pg. 3H, 12E?
- Does CFEB-Check-Disable cause TF/SP mimic?

TST	Clock	BUFGMUX		
0P	drck1	5P	*4P	-TR
2P	2clk	5S	*1S	
3S	clk	7S	*7S	
0S	clk625	2S-	*2S	
7P	ck125	1P	*0S	-BL
5P	clk40	0S	*3P	
4S-	clk156	4S-	*4S	
1S	drck2	3P	*5S	
6S-	sclk	6S-	*6S	

* denotes LOCed position

New Ideas: Store & check DMB source ID's from each fiber?
Feed SLINK status into FMM logic (for UF).
Set DMB CRC OK flag for DDU Empty Events? no...
In case of StuckData send PRST? How to distinguish SEU? Later event still gets LostHdr
or Timeout, could self-correct. Add "PRSTed" VME register to track occurrence.
In case of L1Amismatch, let it run and see if it is better a few~10 evts later. Possible to
self-correct as above...? Can only work if DMB really lost event data.

CSC_L1Err <--Bring to VME-JTAG Reg?

Default Startup Order:

Release DLL (no wait)
4) DONE
5) En. Outputs
6) Release WE

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H3: 0x/LLLL/oooo/ZZZZ/GGMY (LiveDMB(15) Ostat DMB-DAV(15) BOEstat DMBcnt)

T-2: 0x/8000/FFFF/8000/8000 (64-bit unique constant)
T-1: 0x/SSSS.SSSS/QQQQ/PPPP (DDU EOE Status DMBerr DMBwarn(15))
TR: 0x/A/?/WW.WWWW/RRRR/UUMK (EOE WordCount CRCword EOEstat K-Status)

DDU WC, 3 DMB with 1 CFEB (nCFEB=3): 26Ah = 618 dec, 4944 Bytes
DDU WC, 4 DMB with 1 CFEB (nCFEB=4): 336h = 822 dec, 6576 Bytes
DDU WC, 7 DMB with 1 CFEB (nCFEB=7): 59Ah = 1434 dec, 11472 Bytes
DDU WC, 8 DMB with 1 CFEB (nCFEB=8): 666h = 1638 dec, 13104 Bytes
DDU WC, 11 DMB with 1 CFEB (nCFEB=11): 8CAh = 2250 dec, 18000 Bytes
DDU WC, 12 DMB with 1 CFEB (nCFEB=12): 996h = 2454 dec, 19632 Bytes
DDU WC, 15 DMB with 1 CFEB (nCFEB=15): BFAh = 3066 dec, 24528 Bytes