name	BB_adc_FSM		
clock	CLK	posedge	
reset_signal	RST	posedge	
reset_state	Idle		
default_state_is_x	1		
INPUTS			
CLK			Idle
RST			
STROBE			
READBB			
ADCBUSY			
OUTPUTS			
BBCONV	0	regdp	STROBE && READBB
DATAREADY	0	regdp	
hold[2:0]	0	regdp	
scnd		flag	Conv
STATES			ISTROBE BBCONV <= 1
BBCONV	0	output	(STROBE
DATAREADY	0	output	Data .
hold[2:0]	0	output	Data DATAREADY <= 1
scnd		output	(DATAREADY <= 1) ADCBUSY
TRANSITIONS			/
equation	1	def_type	
priority	1000		
			Wait_Busy \
			!ADCBUSY && scnd
			IADODIJOV.
			!ADCBUSY
			_
			Pause
			hold[2:0] <= hold + 1
			$\left(\begin{array}{c} scnd <= 1 \end{array} \right) hold == 3'd6$

STATE MACHINE