TMB 2005+2013 Design

TAMU & UCLA High Energy Physics

Version 5.09

13 Feb 2015

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Table of Contents

[TMB Overview 6](#_Toc411599917)

[CLCT Processing Algorithm 7](#_Toc411599918)

[Signal Synchronization 10](#_Toc411599919)

[CFEB Muonic Receiver Synchronization Stages 10](#_Toc411599920)

[ALCT Muonic Receiver Synchronization Stages 11](#_Toc411599921)

[ALCT Muonic Transmitter Synchronization Stages 12](#_Toc411599922)

[TTC Sequences 16](#_Toc411599923)

[Trigger State 16](#_Toc411599924)

[Bunch Crossing Counter 16](#_Toc411599925)

[Resync 16](#_Toc411599926)

[ALCT+CLCT Matching Algorithm 17](#_Toc411599927)

[Matching Logic 17](#_Toc411599928)

[VME Registers 20](#_Toc411599929)

[Addressing Modes 20](#_Toc411599930)

[Base Address 20](#_Toc411599931)

[Boot Register 20](#_Toc411599932)

[List of Register Addresses 21](#_Toc411599933)

[Definitions of Register Addresses 27](#_Toc411599934)

[TTC Commands 89](#_Toc411599935)

[TMB Board Status Operations 90](#_Toc411599936)

[ID Registers 90](#_Toc411599937)

[Digital Serial Numbers 90](#_Toc411599938)

[Power Supply ADC 90](#_Toc411599939)

[Clock Delays 90](#_Toc411599940)

[JTAG Chains 90](#_Toc411599941)

[RAT Module Status Register USER1 91](#_Toc411599942)

[RAT Module Control Register USER2 91](#_Toc411599943)

[User PROM Programming 92](#_Toc411599944)

[Introduction 92](#_Toc411599945)

[Register Initialization 92](#_Toc411599946)

[VME PROM-0 92](#_Toc411599947)

[JTAG PROM-1 93](#_Toc411599948)

[DMB Readout 97](#_Toc411599949)

[Full-Readout and Local-Readout Format (Long Header) 97](#_Toc411599950)

[Long Header-only Format 97](#_Toc411599951)

[Short Header-only Format 98](#_Toc411599952)

[Miniscope 98](#_Toc411599953)

[Blocked CFEB DiStrips List Format 99](#_Toc411599954)

[Header Word Descriptions 100](#_Toc411599955)

[Sample TMB Raw Hits Dump 114](#_Toc411599956)

[Configuration 116](#_Toc411599957)

[Shunt Settings 116](#_Toc411599958)

[Switch Settings 117](#_Toc411599959)

[Fuses 118](#_Toc411599960)

[Signal Summary 119](#_Toc411599961)

[CCB 119](#_Toc411599962)

[ALCT 120](#_Toc411599963)

[DMB 121](#_Toc411599964)

[CFEB 122](#_Toc411599965)

[MPC 123](#_Toc411599966)

[RPC 124](#_Toc411599967)

[VME 124](#_Toc411599968)

[JTAG 124](#_Toc411599969)

[LEDs & Testpoints 125](#_Toc411599970)

[TMB Total I/O Count 126](#_Toc411599971)

[Connectors 127](#_Toc411599972)

[TMB Connector Summary 127](#_Toc411599973)

[J0-J4 CFEB0-CFEB4 Connectors 128](#_Toc411599974)

[J5 ALCT Cable1 Connector (Receiver) 129](#_Toc411599975)

[J6 ALCT Cable2 Connector (Transmitter) 130](#_Toc411599976)

[J1-J6 SCSI-II 50-Pin Connector Pin Convention 131](#_Toc411599977)

[J7 Xilinx LVDS Xilinx X-Blaster Connector 132](#_Toc411599978)

[P1 Backplane VME64x J1/P1 Connector 133](#_Toc411599979)

[P2A Backplane CCB+DMB Connector 134](#_Toc411599980)

[P2A Backplane CCB+DMB Connector Continued 135](#_Toc411599981)

[P2B Backplane DMB Connector 136](#_Toc411599982)

[P3A Backplane MPC+RPC Connector 137](#_Toc411599983)

[P3B Backplane RPC+ALCT Connector 138](#_Toc411599984)

[Backplane Pin Diagram 139](#_Toc411599985)

[Front Panel Connector Locations 140](#_Toc411599986)

[CCB Front Panel 141](#_Toc411599987)

[Documentation Revision History 143](#_Toc411599988)

[Firmware Change Log 146](#_Toc411599989)

List of Figures

Figure 1: TMB Overview. 6

Figure 2: CFEB Muonic Receiver 13

Figure 3: ALCT Muonic Receiver 14

Figure 4: ALCT Muonic Transmitter 15

Figure 5: 50-Pin PCB Connector (Female) 131

Figure 6: 50 Pin Cable Connector (Male) 131

Figure 7: 50 Pin PCB Connector Pin Convention 131

List of Tables

Table 1: List of VME Register Addresses 21

Table 2: Fast Control Bus ccb\_cmd[5..0] Decoding Scheme 89

Table 3: Shunts 116

Table 4: Switch Settings 117

Table 5: Fuses for TMB2005 118

Table 6A: Fuses for TMB2013 118

Table 7: CCB Signal Summary 119

Table 8: ALCT Signal Summary 120

Table 9: DMB Signal Summary 121

Table 10: CFEB Signal Summary 122

Table 11: MPC Signal Summary 123

Table 12: RPC Signal Summary 124

Table 13: VME Signal Summary 124

Table 14: JTAG Signal Summary 124

Table 15: TMB Front Panel LEDs 125

Table 16: TMB Total I/O Count 126

Table 17: TMB2005 Connector Summary 127

Table 18: J0-J4 CFEB0/4-to-TMB Connectors 128

Table 19: J5 ALCT Cable1 Connector [J10 on ALCT board] 129

Table 20: J6 ALCT Cable2 Connector [J11 on ALCT board] 130

Table 21: J8 Xilinx LVDS X-Blaster Connector 132

Table 22: P1 VME64x Connector 133

Table 23: P2A Backplane CCB+DMB Connector 134

Table 24: P2B Backplane DMB Connector 136

Table 25: P3A Backplane MPC Connector 137

Table 26: P3B Backplane RPC+ALCT Connector 138

Table 27: Connector CCB Input connector P10 141

Table 28: CCB Output connector P11 141

Table 29: CCB Output connector P12 142

TMB Overview

**CLCT + TMB**

**Logic**

**PROM**

8

n

1

A2

**JTAG**

3

**DCFEB [6:0]**

7 Fiber Links

(expandable to 12 links)

TMB2013 only

73.2 Gb/s

**CFEB 0**

TMB2005

or

**DCFEB 0**

TMB2013

2480 MHz

40 MHz clock

**CFEB 4**

TMB2005

or

**DCFEB 6**

TMB2013

2480 MHz

40 MHz clock

5 CFEBs in TMB2005 or 7 DCFEBs in TMB2013

**…**

40 MHz clock

2880 MHz + 110 MHz

1580 MHz + 510 MHz

**ALCT**

**RPC**

4080 MHz

D16

A24 + GA5

**VME**

40 MHz clock

4640 MHz

4640 MHz

**CCB**

440 MHz

4440 MHz

40 MHz clock

**DMB**

3280 MHz

180 MHz

**MPC**

Figure : TMB Overview.

CLCT Processing Algorithm

bx -½: Latch 1st-in-time CFEB transmission

bx 0: Latch 2nd in-time CFEB transmission

* Demultiplex 1st-in-time and 2nd-in-time CFEB Triads
* Map cable-signal ordering into 5 CFEBs x 8 DiStrip Triads x 6 Layers (240 signals)
* Store CFEB Triads in Raw-hits RAM
* Multiplex CFEB Triads with internal pattern-injector RAM AND Triads with Hot Channel Mask to disable errant DiStrips
* Decode Triad start bits (240 processed in parallel)
* Triad decoder state machines run continuously to preclude missing any start bits
* Each ½-strip one-shot can fire again on the same clock cycle that the previous ½-strip pulse ends
* If a 2nd triad arrives for the same DiStrip while busy, the triad is decoded but the one-shot does not fire
* In that case, the triad-skipped counter is incremented

bx 1: Decode Triad strip bits

bx 2: Decode Triad ½-strip bits

bx 3: Fire ½-strip one-shots for 6bx (triad\_persist is programmable, 6bx is the default) OR 160 ½-strips on each layer for layer-trigger mode

* Stagger correction (if stagger\_hs\_csc =1) shifts alternate layers by -1hs

ly0 -0hs i.e. hs5🡪 hs5

ly1 -1hs i.e. hs6🡪 hs5

ly2 -0hs i.e. hs5 🡪 hs5 key layer ly2

ly3 -1hs i.e. hs6 🡪 hs5

ly4 -0hs i.e. hs5 🡪 hs5

ly5 -1hs i.e. hs6 🡪 hs5

* Pattern Finding: for each of 160 key ½-strips consider the 42 neighboring ½-strips (i.e. on key 5 use the following ½-strips)

hs 0123456789A

ly0[10:0] xxxxxkxxxxx 5+1+5 =11

ly1[ 7:3] xxkxx 2+1+2 = 5

ly2[ 5:5] k 0+1+0 = 1

ly3[ 7:3] xxkxx 2+1+2 = 5

ly4[ 9:1] xxxxkxxxx 4+1+4 = 9

ly5[10:0] xxxxxkxxxxx 5+1+5 =11

* For each of 160 key ½-strips, count layers with hits matching the 9 pattern templates.Pattern ID=1 is a layer-OR trigger, Pattern ID=0 is no-pattern-found

Hit pattern LUTs for 1 layer: - = don’t care, xx= one hit or the other or both

Pattern id=2 id=3 id=4 id=5 id=6 id=7 id=8 id=9 idA

Bend dir bd=0 bd=1 bd=0 bd=1 bd=0 bd=1 bd=0 bd=1 bd=0

| | | | | | | | |

ly0 --------xxx xxx-------- -------xxx- -xxx------- ------xxx-- --xxx------ -----xxx--- ---xxx----- ----xxx----

ly1 ------xx--- ---xx------ ------xx--- ---xx------ -----xx---- ----xx----- -----xx---- ----xx----- -----x-----

ly2 key -----x----- -----x----- -----x----- -----x----- -----x----- -----x----- -----x----- -----x----- -----x-----

ly3 ---xxx----- -----xxx--- ---xx------ ------xx--- ----xx----- -----xx---- ----xx----- -----xx---- -----x-----

ly4 -xxx------- -------xxx- -xxx------- -------xxx- ---xx------ ------xx--- ---xxx----- -----xxx--- ----xxx----

ly5 xxx-------- --------xxx -xxx------- -------xxx- --xxx------ ------xxx-- ---xxx----- -----xxx--- ----xxx----

| | | | | | | | |

// Extent 0123456789A 0123456789A 0123456789A 0123456789A 0123456789A 0123456789A 0123456789A 0123456789A 0123456789A

// Avg.bend - 8.0 hs + 8.0 hs -6.0 hs +6.0 hs -4.0 hs +4.0 hs -2.0 hs +2.0 hs 0.0 hs

// Min.bend -10.0 hs + 6.0 hs -8.0 hs +4.0 hs -6.0 hs +2.0 hs -4.0 hs 0.0 hs -1.0 hs

// Max.bend - 6.0 hs +10.0 hs -4.0 hs +8.0 hs -2.0 hs +6.0 hs 0.0 hs +4.0 hs +1.0 hs

bx 4:Result for each of 160 keys is a list of 9 pattern-ID numbers (pid) [2 to A] and corresponding number of layers [0 to 6] with matching hits (nhits)

* Find the best 1-of-9 pattern ID numbers for each key by comparing nhits
* Ignore bend direction: left and right bends have equal priority (bit 0 of pid implies bend direction)
* If two pattern IDs have the same nhits, take the higher pattern ID
* A key with no matching hits, would always return pid=A and nhits=0

bx 5: Pre-trigger if any 1-of-160 keys have nhits ≥ hit\_thresh\_pretrig and pid ≥ pid\_thresh\_pretrig

* Construct 5-bit active-cfeb list for DMB:
* cfebs with a key that has nhits ≥ hit\_thresh\_pretrig and pid ≥ pid\_thresh\_pretrig
* cfebs with a key that has nhits ≥ dmb\_thresh\_pretrig
* cfebs adjacent to a cfeb that has nhits ≥ hit\_thresh\_pretrig and pid ≥ pid\_thresh\_pretrrig within adjfeb\_dist

bx 6: Finding 1st CLCT:

* Construct 7-bit pattern quality for sorting: pat[7:0]
* pat[7:5]=nhits[2:0]
* pat[4:0]=pid[3:0]
* Ignore the bend direction bit (pid[0]), left and right bends have equal priority
* Store pat[7:0] for 160 keys for use later to find 2nd CLCT
* Start finding best 1-of-160 keys by sorting on the 6-bit number pat[7:1]
* If two keys have the same pat[7:1] take the lower key

bx 7: Find 1st CLCT:

* Finish finding best 1-of-160 keys by sorting on the 6-bit number pat[7:1]
* Store 1st CLCT info: key, pattern ID, and number of hits
* For empty events, key=0, pid=A and nhits=0. If clct\_blanking=1, then key=pid=hits=0

bx 8: Finding 2nd CLCT:

* Construct list of busy keys
* Mark keys near 1st CLCT as busy from 1st key-nspan to 1st key+pspan
* If clct\_sep\_src=1, pspan and nspan are set equal to clct\_sep\_vme, typically 10hs
* If clct\_sep\_src=0, pspan and nspan are read from RAM and depend on the pattern ID number
* This allows two non-bending tracks | | to be closer than bending tracks / \
* Start finding best 1-of-160 keys by sorting on the 6-bit number pat[7:1]
* Skip busy keys
* If two keys have the same pat[7:1] take the lower key

bx 9: Find 2nd CLCT:

* Finish finding best 1-of-160 keys by sorting on the 6-bit number pat[7:1]
* Store 2nd CLCT info: key, pattern ID, and number of hits
* For empty events, key=11, pid=A and nhits=0. If clct\_blanking=1, then key=pid=hits=0

bx 10: Drift Delay 1bx (waits for CSC drifting)

bx 11: Drift Delay 1bx

* If clct0 nhits < hit\_thresh\_postdrift OR pid < pid\_thresh\_post\_drift, discard event

bx 12: Match to ALCT window 0

* If alct matches, jump to bx15 logic, latency is shortened 2bx

bx 13: Match to ALCT window 1

* If alct matches, jump to bx15 logic, latency is shortened 1bx

bx 14: Match to ALCT window 2

* If ALCT does not arrive, and clct\_only mode is enabled, accept CLCT at window 2
* If ALCT does not arrive, and not in clct\_only mode, discard event

bx 15: Construct two LCTs from CLCT and ALCT data

* If event has 2 CLCTs and 1 ALCT, copy 1st ALCT into 2nd ALCT position
* If event has 1 CLCT and 2 ALCTs, copy 1st CLCT into 2nd CLCT position
* Calculate LCT quality
* Multiplex mpc injector ram data

bx 16: Transmit 1st-in-time LCT frame to MPC

bx 16½:Transmit 2nd-in-time LCT frame to MPC

Signal Synchronization

CFEB Muonic Receiver Synchronization Stages

CFEB Double Data Rate (DDR) receiver logic is designed to synchronize incoming comparator data to TMB’s main clock, while minimizing CLCT trigger-path latency. It has a programmable 0-16bx delay stage to compensate for differing CFEB cable lengths.

The logic is shown schematically (Figure 2) but the actual TMB logic is written in behavioral Verilog.

U1A: Latches incoming CFEB data din on the *falling* edge of clock\_iob.

* The user has already tuned the associated cfeb[n]\_rxd digital phase shifter so that clock\_iob always latches stable data.

U1B: Latches incoming din on the *rising* edge of clock\_iob.

* U1A and U1B comprise a single DDR I/O-Block flip-flop, and are only shown here separately for clarity.

U2: Latches data transferred from U1A on the *rising* edge of clock\_iob.

* U2 now holds din\_1st-in-time data, aligned with the *rising* edge of clock\_iob, while
* U1B holds din\_2nd-in-time data, also aligned with the *rising* edge of clock\_iob.
* In non-muonic firmware, this would be the end stage, because clock\_iob would be the same as TMB’s main clock.
* In muonic firmware versions, din\_1st and din\_2nd still need to be synchronized to TMB’s main clock. This is done by latching data on both the *rising* (positive) edge and *failing* (negative) edge of the main clock, then selecting one latch or the other with the posneg bit.
* If the positive edge flip-flops U11, U12 are out-of-time (creating a dead-spot in the din receive window) then the negedge flip-flops U3, U4 must be in-time. One set of latches, either U11, U12 or U3, U4 will always be in-time for a given phase of clock\_iob.

U3, U4: Latch din\_1st and din\_2nd on the *falling* edge TMB’s main clock\_1x.

U5,U6: Select either positive edge data from U2, U1B or negative edge data from U3, U4.

U7,U8: Delay data by 1-to-16 bx, according to delay[3:0] from a VME register.

* Setting address=0 for U7, U8 gives a 1bx delay, so delay-1 is used to form the address.

U14: Subtracts 1 from delay[3:0] to form the shift register address for U7, U8.

U9, U10: Bypass delays U7, U8 if the delay is 0, thus giving a 0-to-16bx delay span.

U11, U12: Latch data on the *rising* edge of TMBs main clock\_1x, and are the final synchronization stage.

ALCT Muonic Receiver Synchronization Stages

ALCT Double Data Rate (DDR) receiver logic is designed to synchronize incoming data to TMB’s main clock. It uses a small number of flip-flops, and is able to fit in a single FPGA column. It uses a different technique than the CFEB sync section, and does not have a delay stage.

The logic is shown schematically (Figure 3), but the actual TMB logic is written in behavioral Verilog.

U1A: Latches incoming ALCT data din on the *falling* (negative) edge of clock\_iob.

* The user has already tuned the associated alct\_rxd digital phase shifter so that clock\_iob always latches stable data.

U1B: Latches incoming din on the *rising* (positive) edge of clock\_iob.

* U1A and U1B comprise a single DDR I/O-Block flip-flop, and are only shown here separately for clarity.

U2: Latches ALCT data transferred from U1A on the *rising* (positive) edge of clock\_iob.

* U2 now holds din\_1st-in-time data, aligned with the *rising* (positive) edge of clock\_iob, while
* U1B holds din\_2nd-in-time data, also aligned with the *rising* (positive) edge of clock\_iob.
* In non-muonic firmware, this would be the end stage, because clock\_iob would be the same as TMB’s main clock.

U3, U4: Latch din\_1st and din\_2nd on either the *rising* (positive) or *falling* (negative) edge of TMB’s main clock\_1x.

* They are clocked at 2x the main clock frequency, but are enabled for only one edge direction, according to the value of the posneg bit.
* The edges of clock\_2x are closely aligned to the edges of clock\_1x.

U7:

* If posneg=1, U7 inverts a logic accessible copy of clock\_1x, called clock\_lac.
* If posneg=0, U7 passes clock\_lac un-inverted.
* Because clock\_lac is delayed by about 2ns after clock\_1x, posneg=1 enables U3, U4 to latch data on the edge of clock\_2x that corresponds to the *rising* edge of clock\_1x, and posneg=0 enables latching on the *falling* edge.

**U5, U6:** Latch data on the *rising* edge of TMB’s main clock\_1x, and are the final synchronization stage.

ALCT Muonic Transmitter Synchronization Stages

ALCT Double Data Rate (DDR) transmitter logic is designed to synchronize TMB’s outgoing data to the ALCT board’s clock. It has a programmable 0-16bx delay stage, and a data-path multiplexer for sending test patterns to ALCT.

The logic is shown schematically (Figure 4), but the actual TMB logic is written in behavioral Verilog.

U1, U2: Select the transmitter data source, either ALCT data or the test pattern generator, according to the value of sync\_mode.

U3,U4: Delay data by 1-to-16 bx, according to the VME-set delay-1 (the subtractor is not shown).

U3, U4: Delay data by 1-to-16 bx, according to delay[3:0] from a VME register.

* Setting address=0 for U3, U4 gives a 1bx delay, so delay-1 is used to form the address.

U15: Subtracts 1 from delay[3:0] to form the shift register address for U3, U4.

U5, U6: Bypass delays U3, U4 if the delay is 0, thus giving a 0-to-16 bx delay span.

U7, U8: Latch data on the *rising* edge of TMB’s main clock\_1x, and are the final main-clock stage.

* In non-muonic firmware, this would be the end stage, because clock\_iob would be the same as TMB’s main clock.

U9, U10: Latch data on either the *rising* or *falling* edge of TMBs main clock\_1x.

* They are clocked at 2x the main clock frequency, but are enabled for only one edge direction, according to the value of the posneg bit.
* The edges of clock\_2x are closely aligned to the edges of clock\_1x.

U14:

* If posneg=1, U14 inverts a logic accessible copy of clock\_1x, called clock\_lac.
* If posneg=0, U14 passes clock\_lac un-inverted.
* Because clock\_lac is delayed by about 2ns after clock\_1x, posneg=1 enables U9, U10 to latch data on the edge of clock\_2x that corresponds to the *rising* edge of clock\_1x, and posneg=0 enables latching on the *falling* edge.

U12: Latches 1st-in-time data on the *rising* edge of clock\_iob. It is a DDR I/O Block flip-flop that transmits 1st-in-time data on the *rising* edge of clock\_iob, and 2nd-in-time on the *falling* edge.

U11: Holds 2nd-in-time data for ½ cycle while waiting for U12 to transmit 1st-in-time data.

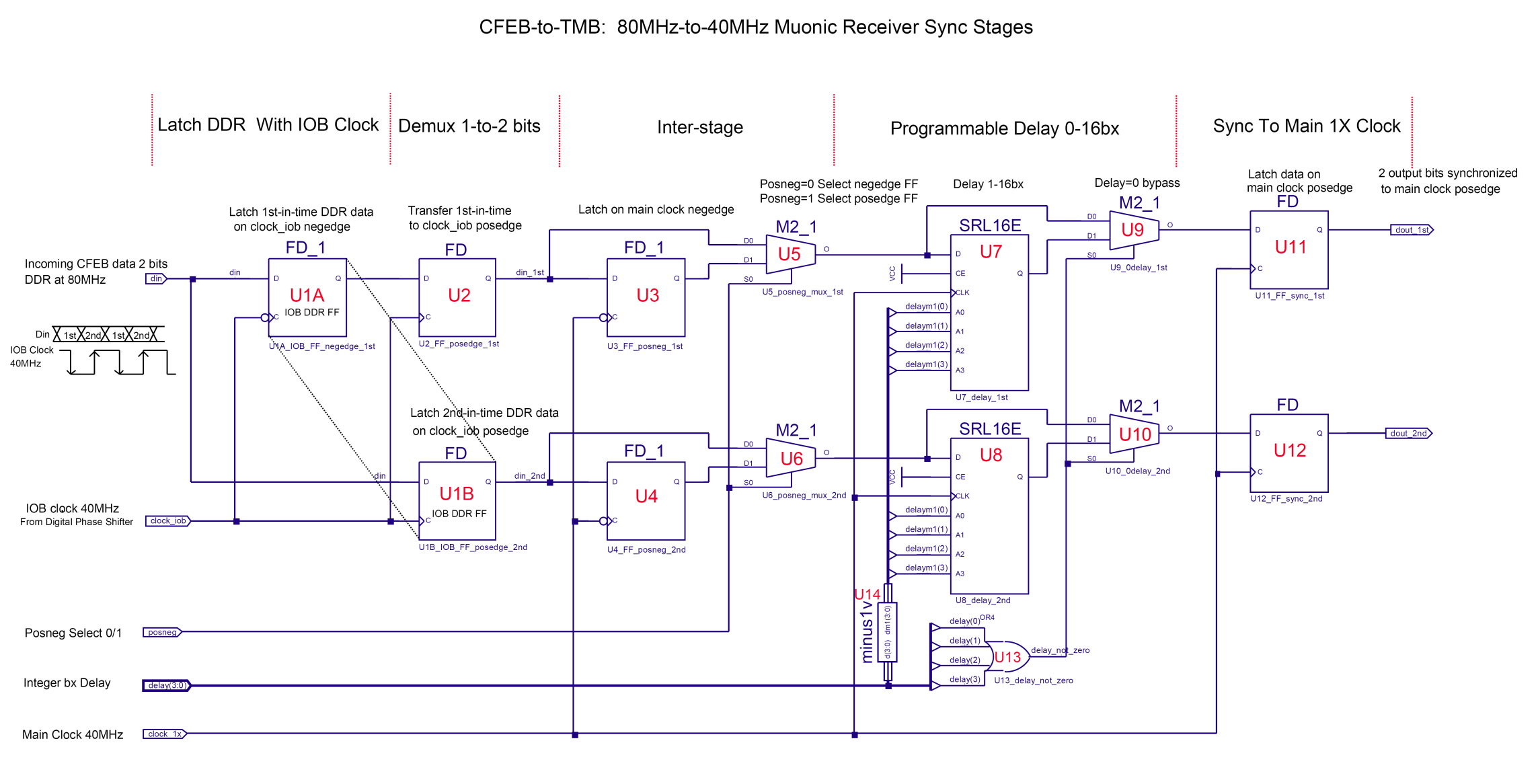


Figure : CFEB Muonic Receiver

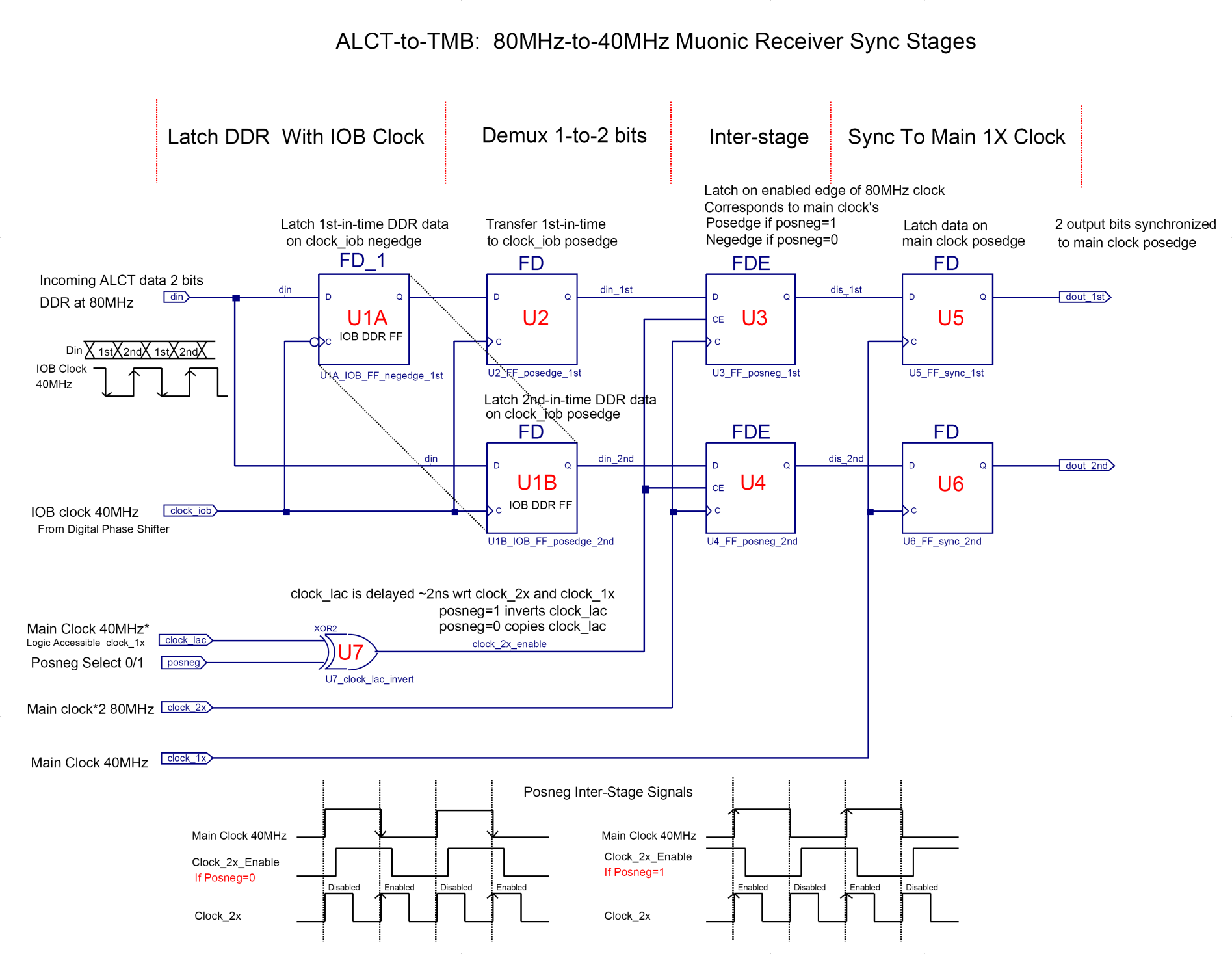


Figure : ALCT Muonic Receiver

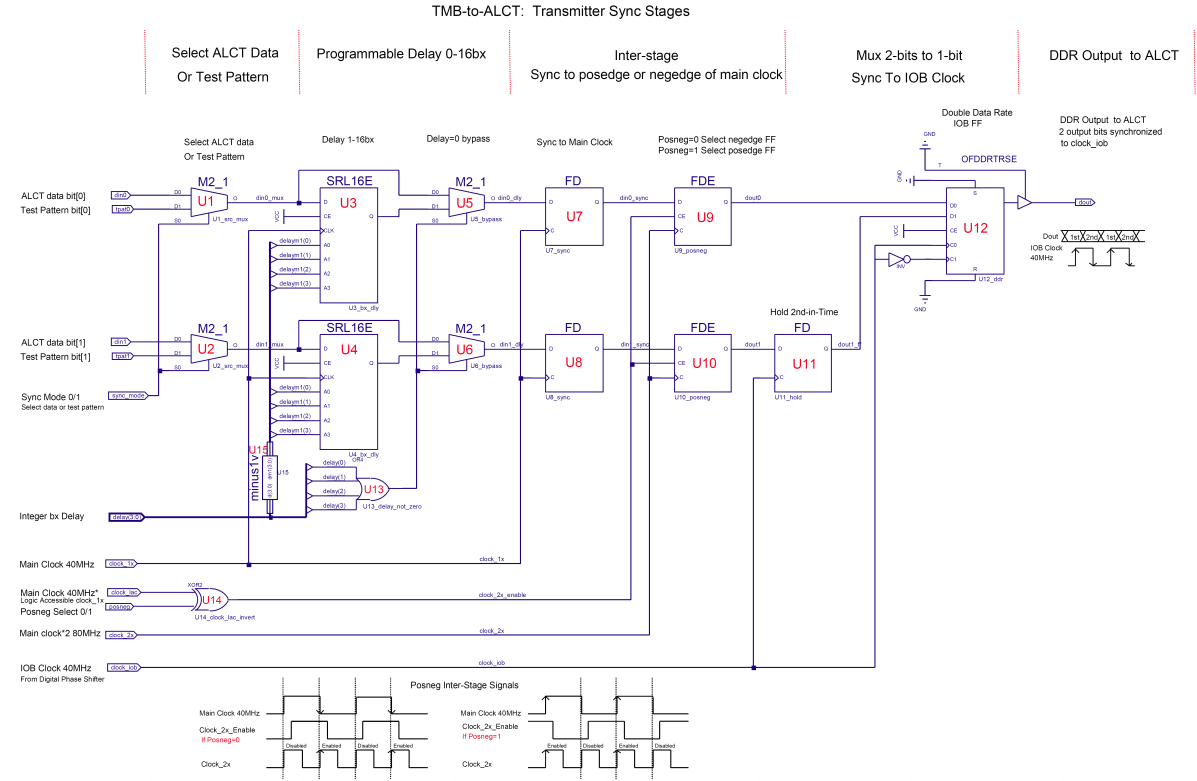


Figure : ALCT Muonic Transmitter

TTC Sequences

Trigger State

Start/Stop Triggering Sequence:

On hard\_reset go to the StopTrigger state: TMBs CLCT processing machine goes to “idle”.

On ttc\_start\_trigger, wait for the next BX0 (if ttc starts are allowed)

On the next ttc\_bx0, resume triggering.

On ttc\_stop\_trigger (if ttc stops are allowed) or ttc\_resync go the StopTrigger state.

Bunch Crossing Counter

Bunch Counter Reset:

On ttc\_resync or ttc\_bxreset, preset the BXN, and hold the count.

On the next BX0 resume counting bunch crossings.

On subsequent BX0s, check that BXN is again at the preset value, if not, set sync\_error.

TMB further checks that when BXN is at the preset value, that a BX0 arrived, if not, set sync\_error.

Resync

L1A Counter Reset:

On ttc\_resync or ccb\_evcntreset, clear L1A event counters.

Buffer Reset:

ttc\_resync clears TMBs buffer-pointers, aborts any readout in progress, and returns various state machines to their idle states (a similar condition to after power-up or hard-reset).

ALCT+CLCT Matching Algorithm

Matching Logic

**LCT Duplication:**

// Fill in missing ALCT if CLCT has 2 muons, missing CLCT if ALCT has 2 muons

wire no\_alct = !alct0\_vpf;

wire no\_clct = !clct0\_vpf;

wire one\_alct = alct0\_vpf && !alct1\_vpf;

wire one\_clct = clct0\_vpf && !clct1\_vpf;

wire two\_alct = alct0\_vpf && alct1\_vpf;

wire two\_clct = clct0\_vpf && clct1\_vpf;

wire dupe\_alct = one\_alct && two\_clct;

wire dupe\_clct = one\_clct && two\_alct;

wire [MXALCT-1:0] alct\_dummy = clct0\_real[18:17] << 11; // Inserts clct bxn into

wire [MXCLCT-1:0] clct\_dummy = 0; // frame for clct\_only events

wire [MXALCT-1:0] alct0 = (no\_alct ) ? alct\_dummy : alct0\_real; // Substitute dummy alct

wire [MXALCT-1:0] alct1 = (dupe\_alct) ? alct0\_real : alct1\_real;

wire [MXCLCT-1:0] clct0 = (no\_clct ) ? clct0\_real : clct0\_real; // Do not

wire [MXCLCT-1:0] clct1 = (dupe\_clct) ? clct0\_real : clct1\_real;

wire first\_vpf = alct0\_vpf || clct0\_vpf; // First muon exists

wire second\_vpf = alct1\_vpf || clct1\_vpf; // Second muon exists

LCT Quality:

module lct\_quality (ACC,A,C,A4,C4,P,CPAT,Q);

// Ports

input ACC; // ALCT accelerator muon bit

input A; // bit: ALCT was found

input C; // bit: CLCT was found

input A4; // bit (N\_A>=4), where N\_A=number of ALCT layers

input C4; // bit (N\_C>=4), where N\_C=number of CLCT layers

input [3:0] P; // 4-bit CLCT pattern number that is presently 1 for n-layer triggers,

// 2-10 for current patterns, 11-15 "for future expansion".

input CPAT; // bit for cathode .pattern trigger., i.e. (P>=2 && P<=10) at present

output [3:0] Q; // 4-bit TMB quality output

// Quality-by-quality definition

reg [3:0] Q;

always @\* begin

if ( !ACC && A4 && C4 && P==10 ) Q=15; // HQ muon, straight

else if ( !ACC && A4 && C4 && (P==9 || P==8) ) Q=14; // HQ muon, slight bend

else if ( !ACC && A4 && C4 && (P==7 || P==6) ) Q=13; // HQ muon, more

else if ( !ACC && A4 && C4 && (P==5 || P==4) ) Q=12; // HQ muon, more

else if ( !ACC && A4 && C4 && (P==3 || P==2) ) Q=11; // HQ muon, more

// Q=10; // reserved for HQ muons with future patterns

// Q=9; // reserved for HQ muons with future patterns

else if ( ACC && A4 && C4 && CPAT ) Q=8; // HQ muon, but accel ALCT

else if ( A && !A4 && C4 && CPAT ) Q=7; // HQ cathode, but marginal anode

else if ( && A4 && C && !C4 && CPAT ) Q=6; // HQ anode, but marginal cathode

else if ( A && !A4 && C && !C4 && CPAT ) Q=5; // marginal anode and cathode

// Q=4; // reserved for LQ muons with 2D information in the future

else if ( A && C && P==1 ) Q=3; // any match but layer CLCT

else if ( !A && C ) Q=2; // some CLCT, no ALCT (unmatched)

else if ( A && !C ) Q=1; // some ALCT, no CLCT (unmatched)

else Q=0; // should never be assigned

end

MPC Format:

assign mpc0\_frame0[6:0] = alct0\_key[6:0];

assign mpc0\_frame0[10:7] = clct0\_pat[3:0];

assign mpc0\_frame0[14:11] = lct0\_quality[3:0] \* lct0\_vpf;

assign mpc0\_frame0[15] = lct0\_vpf;

assign mpc0\_frame1[7:0] = {clct0\_cfeb[2:0],clct0\_key[4:0]};

assign mpc0\_frame1[8] = clct0\_bend;

assign mpc0\_frame1[9] = clct\_sync\_err & tmb\_sync\_err\_en[0];

assign mpc0\_frame1[10] = alct0\_bxn[0];

assign mpc0\_frame1[11] = clct\_bx0 \* lct0\_vpf;

assign mpc0\_frame1[15:12] = csc\_id[3:0]\* lct0\_vpf;

assign mpc1\_frame0[6:0] = alct1\_key[6:0];

assign mpc1\_frame0[10:7] = clct1\_pat[3:0];

assign mpc1\_frame0[14:11] = lct1\_quality[3:0] \* lct1\_vpf;

assign mpc1\_frame0[15] = lct1\_vpf;

assign mpc1\_frame1[7:0] = {clct1\_cfeb[2:0],clct1\_key[4:0]};

assign mpc1\_frame1[8] = clct1\_bend;

assign mpc1\_frame1[9] = clct\_sync\_err & tmb\_sync\_err\_en[1] & lct1\_vpf;

assign mpc1\_frame1[10] = alct1\_bxn[0];

assign mpc1\_frame1[11] = clct\_bx0 \* lct1\_vpf;

assign mpc1\_frame1[15:12] = csc\_id[3:0] \* lct1\_vpf;

Transmission to MPC is 1st Frame[31:0] = {mpc1\_frame0[15:0],mpc0\_frame0[15:0]}

2nd Frame[31:0] = {mpc1\_frame1[15:0],mpc0\_frame1[15:0]}

| Signal | 1st in Time | 2nd in Time | P3Apin | Test Point |
| --- | --- | --- | --- | --- |
| mpc\_tx[00] | alct\_first\_key[0] | clct\_first\_key[0] | A1 | TP331-1 |
| mpc\_tx[01] | alct\_first\_key[1] | clct\_first\_key[1] | B1 | TP331-2 |
| mpc\_tx[02] | alct\_first\_key[2] | clct\_first\_key[2] | D1 | TP331-3 |
| mpc\_tx[03] | alct\_first\_key[3] | clct\_first\_key[3] | E1 | TP331-4 |
| mpc\_tx[04] | alct\_first\_key[4] | clct\_first\_key[4] | A2 | TP331-5 |
| mpc\_tx[05] | alct\_first\_key[5] | clct\_first\_key[5] | B2 | TP331-6 |
| mpc\_tx[06] | alct\_first\_key[6] | clct\_first\_key[6] | D2 | TP331-7 |
| mpc\_tx[07] | clct\_first\_pat[0] | clct\_first\_key[7] | E2 | TP331-8 |
| mpc\_tx[08] | clct\_first\_pat[1] | clct\_first\_bend | A3 | TP332-1 |
| mpc\_tx[09] | clct\_first\_pat[2] | clct\_first\_sync\_err | B3 | TP332-2 |
| mpc\_tx[10] | clct\_first\_pat[3] | alct\_first\_bxn[0] | D3 | TP332-3 |
| mpc\_tx[11] | lct\_first\_quality[0] | clct\_first\_bx0\_local | E3 | TP332-4 |
| mpc\_tx[12] | lct\_first\_quality[1] | csc\_id[0] | A4 | TP332-5 |
| mpc\_tx[13] | lct\_first\_quality[2] | csc\_id[1] | B4 | TP332-6 |
| mpc\_tx[14] | lct\_first\_quality[3] | csc\_id[2] | D4 | TP332-7 |
| mpc\_tx[15] | first\_vpf | csc\_id[3] | E4 | TP332-8 |
| mpc\_tx[16] | alct\_second\_key[0] | clct\_second\_key[0] | A5 | TP341-1 |
| mpc\_tx[17] | alct\_second\_key[1] | clct\_second\_key[1] | B5 | TP341-2 |
| mpc\_tx[18] | alct\_second\_key[2] | clct\_second\_key[2] | D5 | TP341-3 |
| mpc\_tx[19] | alct\_second\_key[3] | clct\_second\_key[3] | E5 | TP341-4 |
| mpc\_tx[20] | alct\_second\_key[4] | clct\_second\_key[4] | A6 | TP341-5 |
| mpc\_tx[21] | alct\_second\_key[5] | clct\_second\_key[5] | B6 | TP341-6 |
| mpc\_tx[22] | alct\_second\_key[6] | clct\_second\_key[6] | D6 | TP341-7 |
| mpc\_tx[23] | clct\_second\_pat[0] | clct\_second\_key[7] | E6 | TP341-8 |
| mpc\_tx[24] | clct\_second\_pat[1] | lct\_second\_bend | A7 | TP342-1 |
| mpc\_tx[25] | clct\_second\_pat[2] | clct\_second\_sync\_err | B7 | TP342-2 |
| mpc\_tx[26] | clct\_second\_pat[3] | alct\_second\_bxn[0] | D7 | TP342-3 |
| mpc\_tx[27] | lct\_second\_quality[0] | clct\_second\_bx0\_local | E7 | TP342-4 |
| mpc\_tx[28] | lct\_second\_quality[1] | csc\_id[0] | A8 | TP342-5 |
| mpc\_tx[29] | lct\_second\_quality[2] | csc\_id[1] | B8 | TP342-6 |
| mpc\_tx[30] | lct\_second\_quality[3] | csc\_id[2] | D8 | TP342-7 |
| mpc\_tx[31] | second\_vpf | csc\_id[3] | E8 | TP342-8 |

VME Registers

Addressing Modes

TMB2005 responds to A24D16 VME addressing modes:

* Address Modifier 3916, A24 non-privileged mode
* Address Modifier 3D16, A24 supervisor mode

It does not respond to byte-addressing modes, so all valid addresses must be even numbers.

Base Address

TMB2005s “base address” bits A[23:19] select which TMB is being addressed by the VME crate controller. The base address is determined either by the 5 VME-backplane-slot Geographic Address bits or by the Local Address set by two on-board hexadecimal rotary switches. Shunt SH62 selects between Geographic [1-2] and Local [2-3] modes.

* A[23:19] = VME Crate Slot Geographic Address, (Slot= 2 to 21)10 SH62 [1-2]
* A[23:19] = Hexadecimal Switch Address SW2x16+SW1 SH62 [2-3]

Multiple TMBs can be addressed simultaneously using a Global Address:

* A[23:19] = 2610 Addresses all TMBs in parallel
* A[23:19] = 2710 Address all peripheral crate modules

Boot Register

When geographic addressing is used, the S2/S1 hexadecimal switches should be set to 1Ah, which allows the hardware Boot Register to respond to the slot 2610 global address.

The Boot Register responds to all even VME addresses + base between 70000h and 7FFFEh to allow block-mode VME writes.

List of Register Addresses

The addresses are hexadecimal and should be added to base.

Table 1: List of VME Register Addresses

| Address | Register Name | Description |
| --- | --- | --- |
| 70000 | ADR\_BOOT | Hardware Bootstrap Register |
|  |  |  |
| 00 | ADR\_IDREG0 | ID Register 0 |
| 02 | ADR\_IDREG1 | ID Register 1 |
| 04 | ADR\_IDREG2 | ID Register 2 |
| 06 | ADR\_IDREG3 | ID Register 3 |
|  |  |  |
| 08 | ADR\_VME\_STATUS | VME Status Register |
| 0A | ADR\_VME\_ADR0 | VME Address read-back |
| 0C | ADR\_VME\_ADR1 | VME Address read-back |
|  |  |  |
| 0E | ADR\_LOOPBK | Loop-back Register |
| 10 | ADR\_USR\_JTAG | User JTAG |
| 12 | ADR\_PROM | PROM |
|  |  |  |
| 14 | ADR\_DDDSM | 3D3444 State Machine Register + Clock DCMs |
| 16 | ADR\_DDD0 | 3D3444 Delay Chip 0 |
| 18 | ADR\_DDD1 | 3D3444 Delay Chip 1 |
| 1A | ADR\_DDD2 | 3D3444 Delay Chip 2 |
| 1C | ADR\_DDDOE | 3D3444 Delay Chip Output Enables |
| 1E | ADR\_RATCTRL | RAT Module Control |
|  |  |  |
| 20 | ADR\_STEP | Step Register |
| 22 | ADR\_LED | Front Panel +On-Board LEDs |
| 24 | ADR\_ADC | ADCs |
| 26 | ADR\_DSN | Digital Serials |
|  |  |  |
| 28 | ADR\_MOD\_CFG | TMB Configuration |
| 2A | ADR\_CCB\_CFG | CCB Configuration |
| 2C | ADR\_CCB\_TRIG | CCB Trigger Control |
| 2E | ADR\_CCB\_STAT0 | CCB Status |
|  |  |  |
| 30 | ADR\_ALCT\_CFG | ALCT Configuration |
| 32 | ADR\_ALCT\_INJ | ALCT Injector Control |
| 34 | ADR\_ALCT0\_INJ | ALCT Injected ALCT0 |
| 36 | ADR\_ALCT1\_INJ | ALCT Injected ALCT1 |
| 38 | ADR\_ALCT\_STAT | ALCT Sequencer Control/Status |
| 3A | ADR\_ALCT0\_RCD | ALCT LCT0 Received by TMB |
| 3C | ADR\_ALCT1\_RCD | ALCT LCT1 Received by TMB |
| 3E | ADR\_ALCT\_FIFO | ALCT FIFO RAM Status |
|  |  |  |
| 40 | ADR\_DMB\_MON | DMB Monitored signals |
|  |  |  |
| 42 | ADR\_CFEB\_INJ | CFEB Injector Control |
| 44 | ADR\_CFEB\_INJ\_ADR | CFEB Injector RAM address |
| 46 | ADR\_CFEB\_INJ\_WDATA | CFEB Injector Write Data |
| 48 | ADR\_CFEB\_INJ\_RDATA | CFEB Injector Read Data |
|  |  |  |
| 4A | ADR\_HCM001 | CFEB0 Ly0,Ly1 Hot Channel Mask |
| 4C | ADR\_HCM023 | CFEB0 Ly2,Ly3 Hot Channel Mask |
| 4E | ADR\_HCM045 | CFEB0 Ly4,Ly5 Hot Channel Mask |
| 50 | ADR\_HCM101 | CFEB1 Ly0,Ly1 Hot Channel Mask |
| 52 | ADR\_HCM123 | CFEB1 Ly2,Ly3 Hot Channel Mask |
| 54 | ADR\_HCM145 | CFEB1 Ly4,Ly5 Hot Channel Mask |
| 56 | ADR\_HCM201 | CFEB2 Ly0,Ly1 Hot Channel Mask |
| 58 | ADR\_HCM223 | CFEB2 Ly2,Ly3 Hot Channel Mask |
| 5A | ADR\_HCM245 | CFEB2 Ly4,Ly5 Hot Channel Mask |
| 5C | ADR\_HCM301 | CFEB3 Ly0,Ly1 Hot Channel Mask |
| 5E | ADR\_HCM323 | CFEB3 Ly2,Ly3 Hot Channel Mask |
| 60 | ADR\_HCM345 | CFEB3 Ly4,Ly5 Hot Channel Mask |
| 62 | ADR\_HCM401 | CFEB4 Ly0,Ly1 Hot Channel Mask |
| 64 | ADR\_HCM423 | CFEB4 Ly2,Ly3 Hot Channel Mask |
| 66 | ADR\_HCM445 | CFEB4 Ly4,Ly5 Hot Channel Mask |
|  |  |  |
| 68 | ADR\_SEQ\_TRIG\_EN | Sequencer Trigger Source Enables |
| 6A | ADR\_SEQ\_TRIG\_DLY0 | Sequencer Trigger Source Delays |
| 6C | ADR\_SEQ\_TRIG\_DLY1 | Sequencer Trigger Source Delays |
| 6E | ADR\_SEQ\_ID | Sequencer Board + CSC ID |
|  |  |  |
| 70 | ADR\_SEQ\_CLCT | Sequencer CLCT Configuration |
| 72 | ADR\_SEQ\_FIFO | Sequencer FIFO Configuration |
| 74 | ADR\_SEQ\_L1A | Sequencer L1A Configuration |
| 76 | ADR\_SEQ\_OFFSET0 | Sequencer Counter Offsets |
| 78 | ADR\_SEQ\_CLCT0 | Sequencer Latched CLCT0 |
| 7A | ADR\_SEQ\_CLCT1 | Sequencer Latched CLCT1 |
| 7C | ADR\_SEQ\_TRIG\_SRC | Sequencer Trigger Source Read-back |
|  |  |  |
| 7E | ADR\_DMB\_RAM\_ADR | Sequencer RAM Address |
| 80 | ADR\_DMB\_RAM\_WDATA | Sequencer RAM Write Data |
| 82 | ADR\_DMB\_RAM\_WDCNT | Sequencer RAM Word Count |
| 84 | ADR\_DMB\_RAM\_RDATA | Sequencer RAM Read Data |
|  |  |  |
| 86 | ADR\_TMB\_TRIG | TMB Trigger Configuration / MPC Accept |
|  |  |  |
| 88 | ADR\_MPC0\_FRAME0 | MPC0 Frame 0 Data sent to MPC |
| 8A | ADR\_MPC0\_FRAME1 | MPC0 Frame 1 Data sent to MPC |
| 8C | ADR\_MPC1\_FRAME0 | MPC1 Frame 0 Data sent to MPC |
| 8E | ADR\_MPC1\_FRAME1 | MPC1 Frame 1 Data sent to MPC |
|  |  |  |
| 90 | ADR\_MPC\_INJ | MPC Injector Control |
| 92 | ADR\_MPC\_RAM\_ADR | MPC Injector RAM address |
| 94 | ADR\_MPC\_RAM\_WDATA | MPC Injector RAM Write Data |
| 96 | ADR\_MPC\_RAM\_RDATA | MPC Injector RAM Read Data |
|  |  |  |
| 98 | ADR\_SCP\_CTRL | Scope control |
| 9A | ADR\_SCP\_RDATA | Scope read data |
|  |  |  |
| 9C | ADR\_CCB\_CMD | CCB TTC Command Generator |
| 9E | ADR\_BUF\_STAT0 | Buffer Status |
| A0 | ADR\_BUF\_STAT1 | Buffer Status |
| A2 | ADR\_BUF\_STAT2 | Buffer Status |
| A4 | ADR\_BUF\_STAT3 | Buffer Status |
| A6 | ADR\_BUF\_STAT4 | Buffer Status |
|  |  |  |
| A8 | ADR\_ALCT\_FIFO1 | ALCT Raw hits RAM Control |
| AA | ADR\_ALCT\_FIFO2 | ALCT Raw hits RAM data |
|  |  |  |
| AC | ADR\_SEQMOD | Sequencer Trigger Modifiers |
| AE | ADR\_SEQSM | Sequencer Machine State |
| B0 | ADR\_SEQCLCTM | Sequencer CLCT msbs |
| B2 | ADR\_TMBTIM | TMB Timing for ALCT\*CLCT coincidence |
| B4 | ADR\_LHC\_CYCLE | LHC Cycle period, Maximum BXN+1 |
|  |  |  |
| B6 | ADR\_RPC\_CFG | RPC Configuration |
| B8 | ADR\_RPC\_RDATA | RPC Sync Mode Read Data |
| BA | ADR\_RPC\_RAW\_DELAY | RPC Raw Hits Delay + RPC BXN Differences |
| BC | ADR\_RPC\_INJ | RPC Injector Control |
| BE | ADR\_RPC\_INJ\_ADR | RPC Injector RAM Addresses |
| C0 | ADR\_RPC\_INJ\_WDATA | RPC Injector Write Data |
| C2 | ADR\_RPC\_INJ\_RDATA | RPC Injector Read Data |
| C4 | ADR\_RPC\_TBINS | RPC FIFO Time Bins |
| C6 | ADR\_RPC0\_HCM | RPC0 Hot Channel Mask |
| C8 | ADR\_RPC1\_HCM | RPC1 Hot Channel Mask |
|  |  |  |
| CA | ADR\_BX0\_DELAY | BX0 to MPC Delays |
| CC | ADR\_NON\_TRIG\_RO | Non-triggering Event Enables |
|  |  |  |
| CE | ADR\_SCP\_TRIG | Scope Trigger Source Channel |
|  |  |  |
| D0 | ADR\_CNT\_CTRL | Status Counter Control |
| D2 | ADR\_CNT\_RDATA | Status Counter Data |
|  |  |  |
| D4 | ADR\_JTAGSM0 | JTAG State Machine Control (reads JTAG PROM) |
| D6 | ADR\_JTAGSM1 | JTAG State Machine Word Count |
| D8 | ADR\_JTAGSM2 | JTAG State Machine Checksum |
|  |  |  |
| DA | ADR\_VMESM0 | VME State Machine Control (reads VME PROM) |
| DC | ADR\_VMESM1 | VME State Machine Word Count |
| DE | ADR\_VMESM2 | VME State Machine Checksum |
| E0 | ADR\_VMESM3 | Number of VME Addresses Written by VMESM |
| E2 | ADR\_VMESM4 | VME State Machine Write-Data Check |
|  |  |  |
| E4 | ADR\_DDDRSM | RAT 3D3444 State Machine Control |
| E6 | ADR\_DDDR0 | RAT 3D3444 RPC Delays |
|  |  |  |
| E8 | ADR\_UPTIME | Uptime Counter |
| EA | ADR\_BDSTATUS | Board Status Summary |
|  |  |  |
| EC | ADR\_BXN\_CLCT | CLCT BXN At CLCT-Pretrigger |
| EE | ADR\_BXN\_ALCT | ALCT BXN At ALCT-Valid-Pattern-Flag |
|  |  |  |
| F0 | ADR\_LAYER\_TRIG | Layer-Trigger Mode |
|  |  |  |
| F2 | ADR\_ISE\_VERSION | ISE Version + Service Pack |
|  |  |  |
| F4 | ADR\_TEMP0 | Pattern Finder Pre-Trigger |
| F6 | ADR\_TEMP1 | CLCT Separation |
| F8 | ADR\_TEMP2 | CLCT Separation RAM Data |
|  |  |  |
| FA | ADR\_PARITY |  |
| FC | ADR\_CCB\_STAT1 |  |
|  |  |  |
| FE | ADR\_BXN\_L1A | CLCT BXN at last L1A arrival |
| 100 | ADR\_L1A\_LOOKBACK | L1A Lookback distance |
| 102 | ADR\_SEQ\_DEBUG | Sequencer debug signals |
|  |  |  |
| 104 | ADR\_ALCT\_SYNC\_CTRL | ALCT sync mode control |
| 106 | ADR\_ALCT\_SYNC\_TXDATA\_1ST | ALCT sync mode transmit data 1st |
| 108 | ADR\_ALCT\_SYNC\_TXDATA\_2ND | ALCT sync mode transmit data 2nd |
|  |  |  |
| 10A | ADR\_SEQ\_OFFSET1 | Sequencer Counter Offsets Continued |
| 10C | ADR\_MINISCOPE | Internal 16 Channel Digital Miniscope |
|  |  |  |
| 10E | ADR\_PHASER0 | ALCT rxd delay digital phase shifter |
| 110 | ADR\_PHASER1 | ALCT txd delay digital phase shifter |
| 112 | ADR\_PHASER2 | CFEB0 rxd delay digital phase shifter |
| 114 | ADR\_PHASER3 | CFEB1 rxd delay digital phase shifter |
| 116 | ADR\_PHASER4 | CFEB2 rxd delay digital phase shifter |
| 118 | ADR\_PHASER5 | CFEB3 rxd delay digital phase shifter |
| 11A | ADR\_PHASER6 | CFEB4 rxd delay digital phase shifter |
|  |  |  |
| 11C | ADR\_DELAY0\_INT | CFEB0-3 DDR RxD Interstage delays |
| 11E | ADR\_DELAY1\_INT | CFEB4 DDR RxD Interstage delays Continued |
|  |  |  |
| 120 | ADR\_SYNC\_ERR\_CTRL | Synchronization Error Control |
|  |  |  |
| 122 | ADR\_CFEB\_BADBITS\_CTRL | CFEB Bad Bit Control/Status |
| 124 | ADR\_CFEB\_BADBITS\_TIMER | CFEB Bad Bit Check Interval |
|  |  |  |
| 126 | ADR\_CFEB0\_BADBITS\_LY01 | CFEB0 Bad Bits Array |
| 128 | ADR\_CFEB0\_BADBITS\_LY23 | CFEB0 Bad Bits Array |
| 12A | ADR\_CFEB0\_BADBITS\_LY45 | CFEB0 Bad Bits Array |
|  |  |  |
| 12C | ADR\_CFEB1\_BADBITS\_LY01 | CFEB1 Bad Bits Array |
| 12E | ADR\_CFEB1\_BADBITS\_LY23 | CFEB1 Bad Bits Array |
| 130 | ADR\_CFEB1\_BADBITS\_LY45 | CFEB1 Bad Bits Array |
|  |  |  |
| 132 | ADR\_CFEB2\_BADBITS\_LY01 | CFEB2 Bad Bits Array |
| 134 | ADR\_CFEB2\_BADBITS\_LY23 | CFEB2 Bad Bits Array |
| 136 | ADR\_CFEB2\_BADBITS\_LY45 | CFEB2 Bad Bits Array |
|  |  |  |
| 138 | ADR\_CFEB3\_BADBITS\_LY01 | CFEB3 Bad Bits Array |
| 13A | ADR\_CFEB3\_BADBITS\_LY23 | CFEB3 Bad Bits Array |
| 13C | ADR\_CFEB3\_BADBITS\_LY45 | CFEB3 Bad Bits Array |
|  |  |  |
| 13E | ADR\_CFEB4\_BADBITS\_LY01 | CFEB4 Bad Bits Array |
| 140 | ADR\_CFEB4\_BADBITS\_LY23 | CFEB4 Bad Bits Array |
| 142 | ADR\_CFEB4\_BADBITS\_LY45 | CFEB4 Bad Bits Array |
|  |  |  |
| 144 | ADR\_ALCT\_STARTUP\_DELAY | ALCT startup delay milliseconds for Spartan-6 |
| 146 | ADR\_ALCT\_STARTUP\_STATUS | ALCT startup delay machine status |
| Virtex-6 VME Registers: | | |
| 148 | ADR\_V6\_SNAP12\_QPLL | Virtex-6 SNAP12 Serial interface + QPLL status |
|  |  |  |
| 14A | ADR\_V6\_GTX\_RX\_ALL | Virtex-6 GTX common control and status |
| 14C | ADR\_V6\_GTX\_RX0 | Virtex-6 GTX0 control and status |
| 14E | ADR\_V6\_GTX\_RX1 | Virtex-6 GTX1 control and status |
| 150 | ADR\_V6\_GTX\_RX2 | Virtex-6 GTX2 control and status |
| 152 | ADR\_V6\_GTX\_RX3 | Virtex-6 GTX3 control and status |
| 154 | ADR\_V6\_GTX\_RX4 | Virtex-6 GTX4 control and status |
| 156 | ADR\_V6\_GTX\_RX5 | Virtex-6 GTX5 control and status |
| 158 | ADR\_V6\_GTX\_RX6 | Virtex-6 GTX6 control and status |
|  |  |  |
| 15A | ADR\_V6\_SYSMON | Virtex-6 Sysmon ADC |
|  |  |  |
| 15C | ADR\_V6\_CFEB\_BADBITS\_CTRL | CFEB Bad Bit Control/Status extends Adr 122 |
|  |  |  |
| 15E | ADR\_V6\_CFEB5\_BADBITS\_LY01 | CFEB5 Bad Bit Array |
| 160 | ADR\_V6\_CFEB5\_BADBITS\_LY23 | CFEB5 Bad Bit Array |
| 162 | ADR\_V6\_CFEB5\_BADBITS\_LY45 | CFEB5 Bad Bit Array |
|  |  |  |
| 164 | ADR\_V6\_CFEB6\_BADBITS\_LY01 | CFEB6 Bad Bit Array |
| 166 | ADR\_V6\_CFEB6\_BADBITS\_LY23 | CFEB6 Bad Bit Array |
| 168 | ADR\_V6\_CFEB6\_BADBITS\_LY45 | CFEB6 Bad Bit Array |
|  |  |  |
| 16A | ADR\_V6\_PHASER7 | Phaser 7 cfeb5\_rxd phase |
| 16C | ADR\_V6\_PHASER8 | Phaser 8 cfeb6\_rxd phase |
|  |  |  |
| 16E | ADR\_V6\_HCM501 | CFEB5 Ly0,Ly1 Hot Channel Mask |
| 170 | ADR\_V6\_HCM523 | CFEB5 Ly2,Ly3 Hot Channel Mask |
| 172 | ADR\_V6\_HCM545 | CFEB5 Ly4,Ly5 Hot Channel Mask |
|  |  |  |
| 174 | ADR\_V6\_HCM601 | CFEB6 Ly0,Ly1 Hot Channel Mask |
| 176 | ADR\_V6\_HCM623 | CFEB6 Ly2,Ly3 Hot Channel Mask |
| 178 | ADR\_V6\_HCM645 | CFEB6 Ly4,Ly5 Hot Channel Mask |
|  |  |  |
| 17A | ADR\_V6\_EXTEND | DCFEB 7-bit extensions to 5 bit fields in 0x42,68 |
| VME Registers to access and control FIFOs with last trigger decisions sent to MPCs | | |
| 17C | ADR\_MPC0\_FRAME0\_FIFO | MPC0 Frame0 Data Sent to MPC stored in FIFO |
| 17E | ADR\_MPC0\_FRAME1\_FIFO | MPC0 Frame1 Data Sent to MPC stored in FIFO |
| 180 | ADR\_MPC1\_FRAME0\_FIFO | MPC1 Frame0 Data Sent to MPC stored in FIFO |
| 182 | ADR\_MPC1\_FRAME1\_FIFO | MPC1 Frame1 Data Sent to MPC stored in FIFO |
| 184 | ADR\_MPC\_FRAMES\_FIFO\_CTRL | Control of FIFO Storage for Data Sent to MPC |
| VME Registers to access startup timers | | |
| 186 | ADR\_TMB\_MMCM\_LOCK\_TIME | TMB Clock Startup Timer |
| 188 | ADR\_TMB\_POWER\_UP\_TIME | TMB Power-up Timer |
| 18A | ADR\_TMB\_LOAD\_CFG\_TIME | TMB Load Config Timer |
| 18C | ADR\_ALCT\_PHASER\_LOCK\_TIME | ALCT Phaser MMCM Lock Timer |
| 18E | ADR\_ALCT\_LOAD\_CFG\_TIME | ALCT Load Config Timer |
| 190 | ADR\_GTX\_RST\_DONE\_TIME | GTX Reset Done Timer |
| 192 | ADR\_GTX\_SYNC\_DONE\_TIME | GTX Sync Done Timer |

Definitions of Register Addresses

Adr 7000016 ADR\_BOOT Hardware Bootstrap Register

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R=tdo | R=ready | hard  reset  RPC/RAT | /mez  clock  enable | /fpga  vme\_en | /en\_fpga  reset\_alct | hard  reset  TMB | hard  reset  ALCT | JTAG source  vme/fpga | sel3 | sel2 | sel1 | sel0 | tck | tms | Tdi |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Dir | Signal | Default | Description |
| [ 0] | RW | jtag\_vme1 (tdi) | 0 | vme tdi |
| [ 1] | RW | jtag\_vme2 (tms) | 0 | vme tms |
| [ 2] | RW | jtag\_vme3 (tck) | 0 | vme tck |
| [ 3] | RW | sel\_vme0 | 0 | 00XX ALCT JTAG Chain |
| [ 4] | RW | sel\_vme1 | 0 | 01XX TMB Mezzanine FPGA + FPGA PROMs Chain |
| [ 5] | RW | sel\_vme2 | 0 | 10XX TMB User PROMs JTAG chain |
| [ 6] | RW | sel\_vme3 | 0 | 11XX TMB FPGA User JTAG chain |
| [ 7] | RW | vme/usr\_en | 0 | 1=JTAG sourced by Bootstrap Register, 0= from FPGA |
| [ 8] | RW | hard\_reset\_alct\_vme | 0 | 1=Hard reset to ALCT FPGA |
| [ 9] | RW | hard\_reset\_tmb\_vme | 0 | 1=Hard reset to TMB FPGA |
| [10] | RW | /en\_fpga\_reset\_alct | 0 | 0=Allow TMB FPGA to hard reset ALCT |
| [11] | RW | /fpga\_vme\_en | 0 | 0=Allow TMB FPGA to issue VME commands |
| [12] | RW | /mez\_clock\_en | 0 | 0=Enable TMB FPGA mezzanine clock |
| [13] | RW | hard\_reset\_rpc | 0 | 1=Hard reset to RPC (RAT) FPGA |
| [14] | R | vme\_ready | x | 1=FPGA vme logic indicates ready |
| [15] | R | jtag\_vme0 (tdo) | 0 | vme tdo |
| [14] | W | unassigned | - | No connection on PCB |
| [15] | W | unassigned | - | No connection on PCB |

Adr 00 ADR\_IDREG0 ID Register 0

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | ga4 | ga3 | ga2 | ga1 | ga0 | fvers3 | fvers2 | fvers1 | fvers0 | ftype3 | ftype2 | ftype1 | ftype0 |

|  |  |  |  |
| --- | --- | --- | --- |
| Bits | Dir | Typical | Description |
| [03:00] | R | C | Firmware type, C=Normal CLCT/TMB, D=Debug loopback |
| [07:04] | R | D | Firmware version code |
| [12:08] | R | 15 | Geographic address for this board |
| [15:13] | R | 0 | Unassigned |

Adr 02 ADR\_IDREG1 ID Register 1

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| month  msd3 | month  msd2 | month  msd1 | month  msd0 | month  lsd3 | month  lsd2 | month  lsd1 | month  lsd0 | day  msd3 | day  msd2 | day  msd1 | day  msd0 | day  lsd3 | day  lsd2 | day  lsd1 | day  lsd0 |

|  |  |  |  |
| --- | --- | --- | --- |
| Bits | Dir | Typical | Description |
| [07:00] | R | 09 | DD Firmware Version Day (BCD) |
| [15:08] | R | 04 | MM Firmware Version Month (BCD) |

Adr 04 ADR\_IDREG2 ID Register 2

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| year  digit3  3 | year  digit3  2 | year  digit3  1 | year  digit3  0 | year  digit2  3 | year  digit2  2 | year  digit2  1 | year  digit2  0 | year  digit1  3 | year  digit1  2 | year  digit1  1 | year  digit1  0 | year  digit0  3 | year  digit0  2 | year  digit0  1 | year  digit0  0 |

|  |  |  |  |
| --- | --- | --- | --- |
| Bits | Dir | Typical | Description |
| [15:00] | R | 2007 | YYYY Firmware Version Year (BCD) |

Adr 06 ADR\_IDREG3 ID Register 3

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| rev  code  15 | rev  code  14 | rev  code  13 | rev  code  12 | rev  code  11 | rev  code  10 | rev  code  9 | rev  code  8 | rev  code  7 | rev  code  6 | rev  code  5 | rev  code  4 | rev  code  3 | rev  code  2 | rev  code  1 | rev  code  0 |

|  |  |  |  |
| --- | --- | --- | --- |
| Bits | Dir | Typical | Description |
| [15:00] | R |  | Firmware Revcode (as stored in raw hits header) |

Adr 08 ADR\_VME\_STATUS VME Status Register

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TMB  ready | local/geo | iack | acfail | sysreset | sysfail | sysclk | ds1 | as | lword | gap | ga4 | ga3 | ga2 | ga1 | ga0 |

|  |  |  |  |
| --- | --- | --- | --- |
| Bits | Dir | Typical | Description |
| [04:00] | R |  | Crate slot Geographic Address |
| [05] | R |  | Crate slot Geographic Address Parity |
| [06] | R |  | VME signal lword |
| [07] | R |  | VME signal as |
| [08] | R |  | VME signal ds1 |
| [09] | R |  | VME signal sysclk |
| [10] | R |  | VME signal sysfail |
| [11] | R |  | VME signal sysreset |
| [12] | R |  | VME signal acfail |
| [13] | R |  | VME signal iack |
| [14] | R |  | 1=Address mode set to local, 0=Geographic |
| [15] | R |  | 1=TMB reports ready to boot register |

Adr 0A ADR\_VME\_ADR0 VME Address Read-Back

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| a15 | a14 | a13 | a12 | a11 | a10 | a9 | a8 | a7 | a6 | a5 | a4 | a3 | a2 | a1 | lword |

|  |  |  |  |
| --- | --- | --- | --- |
| Bits | Dir | Typical | Description |
| [15:00] | R | a[15:0] | VME Address captured at last write cycle {a[15:1},lword} |

Adr 0C ADR\_VME\_ADR1 VME Address Read-Back

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TMB  ready | local/geo | iack | acfail | sysreset | sysfail | sysclk | ds1 | as | lword | gap | ga4 | ga3 | ga2 | ga1 | ga0 |

|  |  |  |  |
| --- | --- | --- | --- |
| Bits | Dir | Typical | Description |
| [07:00] | R | a[23:16] | VME Address captured at last write cycle |
| [13:08] | R | am[5:0] | VME Address modifier |
| [15:14] | R | 0 | Unassigned |

Adr 0E ADR\_LOOPBK Loop-Back Control Register

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | dmb  tx  res  2 | dmb  tx  res  1 | dmb  tx  res  0 | gtl\_  oe | gtl\_  loop | dmb\_  oe | dmb\_  loop | rpc  loop  bdtest | rpc\_  loop\_  tmb | rpc\_  loop\_  rat | alct\_  txoe | alct\_  rxoe | alct\_  loop | cfeb\_oe |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [00] | R | cfeb\_oe | 1 | 1=CFEB output enable |
| [01] | R | alct\_loop | 0 | 0=No ALCT loop-back |
| [02] | RW | alct\_rxoe | 1 | 1=Enable RAT ALCT LVDS receiver, 0=power down |
| [03] | RW | alct\_txoe | 1 | 1=Enable RAT ALCT LVDS transmitter, 0=power down |
| [04] | R | rpc\_loop\_rat | 0 | 1=RAT FPGA enters loop-back mode |
| [05] | R | rpc\_loop\_bdtest | 0 | 1=En RPC Loop-back (no RAT ), used only in bdtest firmware |
| [06] | R | rpc\_loop\_tmb | 0 | 1=TMBs RAT backplane ICs loop-back mode |
| [07] | R | dmb\_loop | 0 | 0=No DMB loop-back |
| [08] | R | dmb\_oe | 0 | 0=DMB driver enable |
| [09] | R | gtl\_loop | 0 | 0=No GTL loop-back |
| [10] | R | gtl\_oe | 0 | 0=Enable GTL outputs |
| [13:11] | RW | dmb\_tx\_reserved[2:0] | 0 | dmb\_tx[48:46] unused, set to 0 |
| [15:14] | RW | -- |  | Unassigned |

Adr 10 ADR\_USR\_JTAG User JTAG Register

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| tdo  usr | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  | sel3  usr | sel2  usr | sel1  usr | sel0  usr | tck  usr | tms  usr | tdi  usr |

|  |  |  |  |
| --- | --- | --- | --- |
| Bits | Dir | Signal | Description |
| [00] | RW | tdi\_usr | User JTAG Chain TDI (output from FPGA) |
| [01] | RW | tms\_usr | User JTAG Chain TMS |
| [02] | RW | tck\_usr | User JTAG Chain TCK |
| [06:03] | RW | sel\_usr[3:0] | User JTAG Chain Select, 0=ALCT,1=Mez,2=UserPROMs,3=UserChain |
| [13:07] | RW | -- | Unassigned |
| [14] | RW | wr\_usr\_jtag\_dis | 1=disable write access to ADR\_USR\_JTAG, set in Adr D4[11] |
| [15] | R | tdo\_usr | User JTAG Chain TDO (input to FPGA) |

Adr 12 ADR\_PROM User PROMs Register

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | prom\_  src | prom1  ce | prom1  oe | prom1  clk | prom0  ce | prom0  oe | prom0  clk | prom\_  led7 | prom\_  led6 | prom\_  led5 | prom\_  led4 | prom\_  led3 | prom\_  led2 | prom\_  led1 | prom\_  led0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [07:00] | RW | prom\_led[7:0] | CD | PROM data bus shared with On-Board LEDs |
| [08] | RW | prom0\_clk | 0 | PROM 0 clock |
| [09] | RW | prom0\_oe | 0 | PROM 0 output enable |
| [10] | RW | prom0\_ce | 1 | PROM 0 /chip\_enable |
| [11] | RW | prom1\_clk | 0 | PROM 1 clock |
| [12] | RW | prom1\_oe | 0 | PROM 1 output enable |
| [13] | RW | prom1\_ce | 1 | PROM 1 /chip\_enable |
| [14] | RW | prom\_src | 0 | Data bus 0=on-board LEDs, 1=enabled PROM |
| [15] | RW | -- | 0 | Unassigned |

Adr 14 ADR\_DDDSM 3D3444 State Machine Control + DCM Lock Status

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| rpc  lock | dcc  lock | mpc  lock | alctd  lock | alct  rxclk  lock | tmb  clock1  lock | tmb0d  lock | tmb  clock0  lock | ddd  verify | dddsm  busy | auto  start | serial  from | serial  to ddd | adr  latch | ddd  clock | ddd  start |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [00] | RW | ddd\_start\_vme | 0 | Start DDD State Machine |
| [01] | RW | ddd\_clock | 0 | DDD manual-mode clock |
| [02] | RW | ddd\_adr\_latch | 1 | DDD manual-mode address latch, active low |
| [03] | RW | ddd\_serial\_in | 0 | Serial data to DDD chain |
| [04] | RW | ddd\_serial\_out | 0 | Serial data from DDD chain |
| [05] | RW | ddd\_auto\_start | 1 | DDD State Machine autostart state |
| [06] | R | ddd\_busy | 0 | DDD State Machine busy |
| [07] | R | ddd\_verify\_ok | 1 | DDD data read back verified OK |
| [08] | R | lock\_tmb\_clock0 | 1 | TMB clock 0 DCM locked |
| [09] | R | lock\_tmb\_clock0d | 1 | TMB clock 0d DCM locked |
| [10] | R | lock\_tmb\_clock1 | 1 | TMB clock 1 DCM locked |
| [11] | R | lock\_alct\_rxclock | 1 | ALCT rxclock DCM locked |
| [12] | R | lock\_alct\_clockd | 1 | ALCT rxclockd DCM locked |
| [13] | R | lock\_mpc\_clock | 1 | CFEB rxd clock DCM locked (was mpc) |
| [14] | R | lock\_dcc\_clock | 1 | DCC clock DCM locked |
| [15] | R | lock\_rpc\_clock | 1 | RPC clock DCM locked |

Adr 16 ADR\_DDD0 3D3444 Chip 0 Delays, 1 step = 2ns

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| delay\_ch3 | delay\_ch3 | delay\_ch3 | delay\_ch3 | delay\_ch2 | delay\_ch2 | delay\_ch2 | delay\_ch2 | delay\_ch1 | delay\_ch1 | delay\_ch1 | delay\_ch1 | delay\_ch0 | delay\_ch0 | delay\_ch0 | delay\_ch0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [03:00] | RW | delay\_ch0[3:0] | 0 | alct\_tof\_delay, shift entire ALCT in clockspace |
| [07:04] | RW | delay\_ch1[3:0] | 1 | alct\_rxclock delay, not used in muonic firmware |
| [11:08] | RW | delay\_ch2[3:0] | 6 | DMB tx clock |
| [15:12] | RW | delay\_ch3[3:0] | 9 | RPC tx clock |

Adr 18 ADR\_DDD1 3D3444 Chip 1 Delays, 1 step = 2ns

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| delay\_ch7 | delay\_ch7 | delay\_ch7 | delay\_ch7 | delay\_ch6 | delay\_ch6 | delay\_ch6 | delay\_ch6 | delay\_ch5 | delay\_ch5 | delay\_ch5 | delay\_ch5 | delay\_ch4 | delay\_ch4 | delay\_ch4 | delay\_ch4 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [03:00] | RW | delay\_ch4[3:0] | 0 | tmb\_clock1, not used |
| [07:04] | RW | delay\_ch5[3:0] | 0 | mpc\_clock not used |
| [11:08] | RW | delay\_ch6[3:0] | 0 | cfeb\_tof\_delay, shift all cfebs in clockspace |
| [15:12] | RW | delay\_ch7[3:0] | 7 | CFEB 0 clock |

Adr 1A ADR\_DDD2 3D3444 Chip 2 Delays, 1 step = 2ns

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| delay\_ch11 | delay\_ch11 | delay\_ch11 | delay\_ch11 | delay\_ch10 | delay\_ch10 | delay\_ch10 | delay\_ch10 | delay\_ch9 | delay\_ch9 | delay\_ch9 | delay\_ch9 | delay\_ch8 | delay\_ch8 | delay\_ch8 | delay\_ch8 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [03:00] | RW | delay\_ch8[3:0] | 7 | CFEB 1 clock |
| [07:04] | RW | delay\_ch9[3:0] | 7 | CFEB 2 clock |
| [11:08] | RW | delay\_ch10[3:0] | 7 | CFEB 3 clock |
| [15:12] | RW | delay\_ch11[3:0] | 7 | CFEB 4 clock |

Adr 1C ADR\_DDDOE 3D3444 Chip Output Enables

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | cfeb  4 | cfeb  3 | cfeb  2 | cfeb  1 | cfeb  0 | dcc | mpc | tmb1 | rpc  tx | dmb  tx | alct  rx | alct  tx |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [11:00] | RW | ddd\_oe[11:0] | FFF | Bit(n)=1=Enable DDD output channel n |
| [15:12] | RW | Unassigned | 0 | Unassigned |

Adr 1E ADR\_RATCTRL RAT Module Control

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | rpc  dsn en | rpc  free | rpc  lptm | rpc  posneg | rpc  sync |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [0] | RW | rpc\_sync | 0 | 1=RPC 80MHz sync pattern mode |
| [1] | RW | rpc\_posneg | 0 | 1=shift RPC data ½ cycle in RAT FPGA + dsn |
| [2] | RW | rpc\_lptmb | 0 | Not used (for matching rpc\_tx array) |
| [3] | RW | rpc\_free\_tx[0] | 0 | Unassigned |
| [4] | RW | rat\_dsn\_en | 0 | 1=Enable RAT dsn readout |
| [15:5] | RW | -- | 0 | Unassigned |

Adr 20 ADR\_STEP Clock Single-Step + Hard Resets

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | /tmb  hard | /alct  hard | alct  clken | cfeb4  clken | cfeb3  clken | cfeb2  clken | cfeb1  clken | cfeb0  clken | step  run | step  cfeb | step  rpc | step  dmb | step  alct |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [00] | RW | step\_alct | 0 | Step ALCT clock |
| [01] | RW | step\_dmb | 0 | Step DMB clock |
| [02] | RW | step\_rpc | 0 | Step RPC clock |
| [03] | RW | step\_cfeb | 0 | Step CFEB clock |
| [04] | RW | step\_run | 0 | 0=run mode, 1=step clocks |
| [05] | RW | cfeb\_clock\_en0 | 1 | 1=enable CFEB0 clock |
| [06] | RW | cfeb\_clock\_en1 | 1 | 1=enable CFEB1 clock |
| [07] | RW | cfeb\_clock\_en2 | 1 | 1=enable CFEB2 clock |
| [08] | RW | cfeb\_clock\_en3 | 1 | 1=enable CFEB3 clock |
| [09] | RW | cfeb\_clock\_en4 | 1 | 1=enable CFEB4 clock |
| [10] | RW | alct\_clock\_en | 1 | 1=enable ALCT clock |
| [11] | RW | /alct\_hard\_reset\_en | 1 | 1=disable ALCT hard reset |
| [12] | RW | /tmb\_hard\_reset\_en | 1 | 1=disable TMB hard reset |
| [15:13] | RW | -- | 0 | Unassigned |

Adr 22 ADR\_LED Front Panel + On-Board LED Register

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| led  bd7 | led  bd6 | led  bd5 | led  bd4 | led  bd3 | led  bd2 | led  bd1 | led  bd0 | VME | NL1A | NMAT | INVP | L1A | CLCT | ALCT | LCT |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Color | Description |
| [00] | RW | led\_fp\_lct | Blue | LCT TMB matched ALCT+CLCT |
| [01] | RW | led\_fp\_lct | Green | ALCT found a muon |
| [02] | RW | led\_fp\_clct | Green | CLCT found a muon |
| [03] | RW | led\_fp\_l1a | Green | L1A level 1 accept |
| [04] | RW | led\_fp\_invp | Amber | INVP invalid pattern after CSC drift |
| [05] | RW | led\_fp\_nmat | Amber | NMAT no match after ALCT or CLCT triggered |
| [06] | RW | led\_fp\_nl1a | Red | NL1A no L1A after trigger |
| [07] | RW | led\_fp\_vme | Green | VME power-up = on, off=vme access flash |
| [08] | RW | led\_bd0 | Blue | Buffer busy[0] |
| [09] | RW | led\_bd1 | Green | Buffer busy[1] |
| [10] | RW | led\_bd2 | Green | Buffer busy[2] |
| [11] | RW | led\_bd3 | Green | Buffer busy[3] |
| [12] | RW | led\_bd4 | Green | Buffer busy[4] |
| [13] | RW | led\_bd5 | Green | Buffer busy[5] |
| [14] | RW | led\_bd6 | Green | Buffer busy[6] |
| [15] | RW | led\_bd7 | Red | Buffer busy[7] |

Adr 24 ADR\_ADC ADC + Power Comparator Register

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | smb  data | smb  clk | ADC  /cs | ADC  din | ADC  sclock | ADC  dout | /tcrit | V1.5 | V1.8 | V3.3 | V5.0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [00] | R | vstat\_5p0v | 1 | 1 = 5.0V power supply OK |
| [01] | R | vstat\_3p3v | 1 | 1 = 3.3V power supply OK |
| [02] | R | vstat\_1p8v | 1 | 1 = 1.8V power supply OK |
| [03] | R | vstat\_1p5v | 1 | 1 = 1.5V power supply OK |
| [04] | R | /t\_crit | 1 | 1 = FPGA and Board Temperature OK |
| [05] | R | adc\_dout | 0 | Voltage monitor ADC serial data receive |
| [06] | RW | adc\_sclock | 0 | Voltage monitor ADC serial clock |
| [07] | RW | adc\_din | 0 | Voltage monitor ADC serial data transmit |
| [08] | RW | /adc\_cs | 1 | Voltage monitor ADC chip select |
| [09] | RW | smb\_clk | 0 | Temperature monitor ADC serial clock |
| [10] | RW | smb\_data | 1 | Temperature monitor ADC serial data, open drain |
| [15:11] | RW | -- | 0 | Unassigned |

Adr 26 ADR\_DSN Digital Serial Numbers

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | RAT  DSN  Data | RAT  DSN  Busy | RAT  DSN  Init | RAT  DSN  Write | RAT  DSN  Start | Mez  DSN  Data | Mez  DSN  Busy | Mez  DSN  Init | Mez  DSN  Write | Mez  DSN  Start | TMB  DSN  Data | TMB  DSN  Busy | TMB  DSN  Init | TMB  DSN  Write | TMB  DSN  Start |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [00] | RW | tmb\_sn\_start | 0 | TMB Digital serial SM start |
| [01] | RW | tmb\_sn\_write | 0 | TMB Digital serial write pulse |
| [02] | RW | tmb\_sn\_init | 0 | TMB Digital serial Init pulse |
| [03] | R | tmb\_sn\_busy | - | TMB State DSN State Machine busy |
| [04] | R | tmb\_sn\_data | - | TMB State DSN read data |
| [05] | RW | mez\_sn\_start | 0 | Mez Digital Serial State Machine start |
| [06] | RW | mez\_sn\_write | 0 | Mez Digital Serial Write pulse |
| [07] | RW | mez\_sn\_init | 0 | Mez Digital Serial Init pulse |
| [08] | R | mez\_sn\_busy | - | Mez State DSN State Machine busy |
| [09] | R | mez\_sn\_data | - | Mez State DSN read data |
| [10] | RW | rat\_sn\_start | 0 | RAT Digital Serial State Machine start |
| [11] | RW | rat\_sn\_write | 0 | RAT Digital Serial Write pulse |
| [12] | RW | rat\_sn\_init | 0 | RAT Digital Serial Init pulse |
| [13] | R | rat\_sn\_busy | - | RAT State DSN State Machine busy |
| [14] | R | rat\_sn\_data | - | RAT State DSN read data |
| [15] | RW | - | 0 | Unassigned |

Adr 28 ADR\_MOD\_CFG TMB Module Configuration

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| mez  done | ddd  auto | power  up | global  reset  enable | cfeb6  exists | cfeb5  exists | cfeb4  exists | cfeb3  exists | cfeb2  exists | cfeb1  exists | cfeb0  exists | bdled  cylon | bdled  vme | fpled  flash | fpled  cylon | fpled  vme |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [00] | RW | led\_fp\_src\_vme | 0 | 1=Front Panel LEDs sourced from VME register |
| [01] | RW | led\_fp\_cylon | 0 | 1=FP LED Cylon mode, cool |
| [02] | RW | led\_flash\_on\_stop | 1 | 1=Flash Front Panel LEDs on TTT stop\_trigger |
| [03] | RW | led\_bd\_src\_vme | 0 | 1=On-Board LEDs sourced from VME register |
| [04] | RW | led\_bd\_cylon | 0 | 1=BD LED Cylon mode, cool |
| [11:5] | R | cfeb\_exists[6:0] | 7F | CFEB(n) instantiated in this firmware version |
| [12] | RW | global\_reset\_en | 1 | 1=fire global reset if main DLL loses lock |
| [13] | R | power\_up |  | Power-up FF |
| [14] | R | ddd\_autostart |  | 1=3D3444 auto-start enabled, copy of Adr14[05] |
| [15] | R | mez\_done |  | 1=Mezzanine FPGA loaded from PROM |

Adr 2A ADR\_CCB\_CFG CCB Configuration

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| adb  pulse  async | adb  pulse  sync | alct  hard  reset | tmb  hard  reset | tmb  resout2 | tmb  resout1 | tmb  resout0 | tmb  res1 | tmb  res0 | l1a  vme | clct  status  en | alct  status  en | ccb  status  oe | int  l1aen | disabl  tx | ignore  rx |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [00] | RW | ccb\_ignore\_rx | 0 | 1=Ignore Received CCB backplane inputs |
| [01] | RW | ccb\_disable\_tx | 0 | 1=Disble transmitted CCB backplane outputs |
| [02] | RW | ccb\_int\_l1a\_en | 0 | 1=Enable internal L1A emulator |
| [03] | RW | ccb\_status\_oe\_vme | 0 | 1=Enable ALCT+CLCT status to CCB front panel |
| [04] | RW | alct\_status\_en | 0 | 1=Enable ALCT status GTL outputs (req [03]=1) |
| [05] | RW | clct\_status\_en | 0 | 1=Enable CLCT status GTL outputs (req [03]=1) |
| [06] | RW | l1accept\_vme | 0 | 1=fire ccb\_l1accept oneshot |
| [08:07] | R | tmb\_reserved[1:0] |  | Future use |
| [11:09] | R | tmb\_reserved\_out[2:0] |  | Future use |
| [12] | R | tmb\_hard\_reset |  | Reload TMB FPGA |
| [13] | R | alct\_hard\_reset |  | Reload ALCT FPGA |
| [14] | R | alct\_adb\_pulse\_sync |  | ALCT synchronous test pulse from CCB |
| [15] | R | alct\_adb\_pulse\_async |  | ALCT asynchronous test pulse from CCB |
|  |  |  |  |  |
| [12] | W | vme\_evcntres | 0 | Event counter reset || ccb\_evcntres |
| [13] | W | vme\_bcntres | 0 | Bunch crossing reset || ccb\_bcntres |
| [14] | W | vme\_bx0 | 0 | Bx0 signal || ccb\_bx0 |
| [15] | W | vme\_bx0\_emu\_en | 0 | Bx0 Emulator enable |

Adr 2C ADR\_CCB\_TRIG CCB Trigger Control

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| l1a  delay  vme7 | l1a  delay  vme6 | l1a  delay  vme5 | l1a  delay  vme4 | l1a  delay  vme3 | l1a  delay  vme2 | l1a  delay  vme1 | l1a  delay  vme0 | Ignore  start/  stop | ccb  exttrig  bypas | ext  trig  both | clct  ext trg  vme | alct  ext trg  vme | seq  trig  l1aen | clct  ext trg  l1aen | alct  ext trg  l1aen |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [00] | RW | alct\_ext\_trig\_l1aen | 0 | 1=Request ccb l1a on alct ext\_trig |
| [01] | RW | clct\_ext\_trig\_l1aen | 0 | 1=Request ccb l1a on clct ext\_trig |
| [02] | RW | seq\_trig\_l1aen | 1 | 1=Request ccb l1a on sequencer trigger |
| [03] | RW | alct\_ext\_trig\_vme | 0 | 1=Fire alct\_ext\_trig oneshot |
| [04] | RW | clct\_ext\_trig\_vme | 0 | 1=Fire clct\_ext\_trig oneshot |
| [05] | RW | ext\_trig\_both | 0 | 1=clct\_ext\_trig fires alct + alct fires clct\_trig, DC |
| [06] | RW | ccb\_allow\_extbypass | 0 | 1=Allow clct\_exttrig\_ccb when ccb\_ignore\_rx=1 |
| [07] | RW | ccb\_ignore\_startstop | 0 | 1=Ignore ttc\_trig\_start, ttc\_trig\_stop |
| [15:08] | RW | l1a\_delay\_vme | 7216 | Internal L1A delay (not same as sequencer L1A) |

Adr 2E ADR\_CCB\_STAT0 CCB Status

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ccb  bx0 | ccb  bcntrs | ccb  res4 | ccb  res3 | ccb  res2 | ccb  qpll  locked | ccb  ttcrx  ready | ccb  clock  en | ccb  cmd7 | ccb  cmd6 | ccb  cmd5 | ccb  cmd4 | ccb  cmd3 | ccb  cmd2 | ccb  cmd1 | ccb  cmd0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [07:00] | R | ccb\_cmd[7:0] |  | CCB Command word from TTC |
| [08] | R | ccb\_clock40\_enable | 1 | 1=TMB 40MHz clock from CCB enabled |
| [09] | R | ccb\_reserved[0] | 1 | ccb\_ttcrx\_ready TTC ready signal from CCB |
| [10] | R | ccb\_reserved[1] | 1 | ccb\_qpll\_locked PLL locked signal from CCB |
| [13:09] | R | ccb\_reserved[4:2] |  | Future use |
| [14] | R | ccb\_bcntres |  | Bunch counter reset from CCB (backplane) |
| [15] | R | ccb\_bx0 |  | Bunch crossing 0 from CCB (backplane) |

Adr 30 ADR\_ALCT\_CFG ALCT Configuration

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | cfeb  muon  ic | alct  muon  ic | alct  clk  vme | alct  clk  ccb | alct  seq  cmd3 | alct  seq  cmd2 | alct  seq  cmd1 | alct  seq  cmd0 | assert  alct  ext inj | assert  alct  ext trg | alct  ext inj  en | alct  ext trg  en |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [00] | RW | cfg\_alct\_ext\_trig\_en | 1 | 1=Enable alct\_ext\_trig from CCB |
| [01] | RW | cfg\_alct\_ext\_inject\_en | 0 | 1=Enable alct\_ext\_inject from CCB |
| [02] | RW | cfg\_alct\_ext\_trig | 0 | 1=Assert alct\_ext\_trig |
| [03] | RW | cfg\_alct\_ext\_inject | 0 | 1=Assert alct\_ext\_inject |
| [07:04] | RW | alct\_seq\_cmd[3:0] | 0 | ALCT Sequencer command |
| [08] | RW | alct\_clock\_en\_use\_ccb |  | 1=alct\_clock\_en\_vme = ccb\_clock40\_enable |
| [09] | RW | alct\_clock\_en\_use\_vme |  | sets alct\_clock\_en cable signal if [8]=0 |
| [10] | R | alct\_muonic | 1 | ALCT board has independent time-of-flight delay |
| [11] | R | cfeb\_muonic | 0 | CFEBs have independent time-of-flight delay |
| [15:12] | RW | -- | 0 | Unassigned |

Adr 32 ADR\_ALCT\_INJ ALCT Injector Control

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | inject  delay  4 | inject  delay  3 | inject  delay  2 | inject  delay  1 | inject  delay  0 | l1a  inj  ram | alct  inj  ram | link  inject  w clct | start  inject | clear  alct |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [00] | RW | alct\_clear | 0 | 1=Blank ALCT received data |
| [01] | RW | alct\_inject\_mux | 0 | 1=Start ALCT injector State Machine |
| [02] | RW | alct\_sync\_clct | 0 | 1=Link ALCT injector with CLCT inject command |
| [03] | RW | alct\_inj\_ram\_en | 0 | 1=Link ALCT injector to CFEB injector RAM |
| [04] | RW | l1a\_inj\_ram\_en | 0 | 1=Link L1A injector to CFEB injector RAM |
| [09:05] | RW | alct\_inj\_delay[4:0] | 13 | Injector delay |
| [15:10] | RW | -- | 0 | Unassigned |

Adr 34 ADR\_ALCT0\_INJ ALCT0 1st Muon To Inject

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 1st  bxn  1 | 1st  bxn  0 | 1st  key  6 | 1st  key  5 | 1st  key  4 | 1st  key  3 | 1st  key  2 | 1st  key  1 | 1st  key  0 | 1st  amu | 1st  qualty  1 | 1st  qualty  0 | 1st  vpf |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [00] | RW | alct\_first\_valid | 1 | Valid pattern flag |
| [02:01] | RW | alct\_first\_quality[1:0] | 3 | Pattern quality |
| [03] | RW | alct\_first\_amu | 0 | Accelerator muon flag |
| [10:04] | RW | alct\_first\_key[6:0] | 7 | Injected ALCT0 key wire-group |
| [12:11] | RW | alct\_first\_bxn[1:0] | 1 | Injected ALCT0 bunch crossing number |
| [15:13] | RW | -- | 0 | Unassigned |

Adr 36 ADR\_ALCT1\_INJ ALCT1 2nd Muon To Inject

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 2nd  bxn  1 | 2nd  bxn  0 | 2nd  key  6 | 2nd  key  5 | 2nd  key  4 | 2nd  key  3 | 2nd  key  2 | 2nd  key  1 | 2nd  key  0 | 2nd  amu | 2nd  qualty  1 | 2nd  qualty  0 | 2nd  vpf |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [00] | RW | alct\_second\_valid | 1 | Valid pattern flag |
| [02:01] | RW | alct\_second\_quality[1:0] | 2 | Pattern quality |
| [03] | RW | alct\_second\_amu | 0 | Accelerator muon flag |
| [10:04] | RW | alct\_second\_key[6:0] | 6110 | Injected ALCT1 key wire-group |
| [12:11] | RW | alct\_second\_bxn[1:0] | 1 | Injected ALCT1 bunch crossing number |
| [15:13] | RW | -- | 0 | Unassigned |

Adr 38 ADR\_ALCT\_STAT ALCT Sequencer Control/Status

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| alct  txdint  delay  3 | alct  txdint  delay  2 | alct  txdint  delay  1 | alct  txdint  delay  0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | alct  sync  eccerr  1 | alct  sync  eccerr  0 | alct  ecc  blank | alct  ecc  en | alct  cfg  done |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [00] | R | alct\_cfg\_done | 1 | ALCT FPGA loaded from PROM |
| [01] | RW | alct\_ecc\_en | 1 | ALCT ECC trigger data correction enable |
| [02] | RW | alct\_ecc\_err\_blank | 1 | Blank alcts with uncorrected ecc errors |
| [04:03] | R | alct\_sync\_ecc\_err[1:0] | 0 | ALCT sync-mode ECC error code |
| [11:05] | RW | -- | 0 | Unassigned |
| [15:12] | RW | alct\_txd\_int\_delay[3:0] | 0 | Delay data transmitted to ALCT by integer bx |

Adr 3A ADR\_ALCT0\_RCD ALCT 1st Muon Received by TMB

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 1st  bxn  1 | 1st  bxn  0 | 1st  key  6 | 1st  key  5 | 1st  key  4 | 1st  key  3 | 1st  key  2 | 1st  key  1 | 1st  key  0 | 1st  amu | 1st  qualty  1 | 1st  qualty  0 | 1st  vpf |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [00] | R | alct\_first\_valid | 1 | Valid pattern flag |
| [02:01] | R | alct\_first\_quality[1:0] | 0-3 | Pattern quality |
| [03] | R | alct\_first\_amu | 0 | Accelerator muon flag |
| [10:04] | R | alct\_first\_key[6:0] | 0-111 | ALCT0 key wire-group |
| [12:11] | R | alct\_first\_bxn[1:0] | 0-3 | ALCT0 bunch crossing number |
| [15:13] | R | -- | 0 | Unassigned |

Adr 3C ADR\_ALCT1\_RCD ALCT 2nd Muon Received by TMB

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 2nd  bxn  1 | 2nd  bxn  0 | 2nd  key  6 | 2nd  key  5 | 2nd  key  4 | 2nd  key  3 | 2nd  key  2 | 2nd  key  1 | 2nd  key  0 | 2nd  amu | 2nd  qualty  1 | 2nd  qualty  0 | 2nd  vpf |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [00] | R | alct\_second\_valid | 1 | Valid pattern flag |
| [02:01] | R | alct\_second\_quality[1:0] | 0-3 | Pattern quality |
| [03] | R | alct\_second\_amu | 0 | Accelerator muon flag |
| [10:04] | R | alct\_second\_key[6:0] | 0-111 | ALCT1 key wire-group |
| [12:11] | R | alct\_second\_bxn[1:0] | 0-3 | ALCT1 bunch crossing number |
| [15:13] | R | -- | 0 | Unassigned |

Adr 3E ADR\_ALCT\_FIFO ALCT FIFO RAM Status

(Split with Adr A2 ADR\_ALCT\_FIFO1 and A4 ADR\_ALCT\_FIFO2)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | alct  data17 | alct  data16 | alct  wdcnt  10 | alct  wdcnt  9 | alct  wdcnt  8 | alct  wdcnt  7 | alct  wdcnt  6 | alct  wdcnt  5 | alct  wdcnt  4 | alct  wdcnt  3 | alct  wdcnt  2 | alct  wdcnt  1 | alct  wdcnt  0 | alct  RAM  done | alct  RAM  busy |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal |  | Description |
| [00] | R | alct\_raw\_busy |  | ALCT raw hits FIFO busy writing ALCT data |
| [01] | R | alct\_raw\_done |  | ALCT raw hits ready for VME readout |
| [12:02] | R | alct\_raw\_wdcnt[10:0] |  | ALCT raw hits word count stored in RAM |
| [14:13] | R | alct\_raw\_rdata[17:16] |  | ALCT raw hits data MSBs |
| [15] | R | -- | 0 | Unassigned |

Adr 40 ADR\_DMB\_MON DMB Monitored Signals

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 2nd  bxn  1 | 2nd  bxn  0 | 2nd  key  6 | 2nd  key  5 | 2nd  key  4 | 2nd  key  3 | 2nd  key  2 | 2nd  key  1 | 2nd  key  0 | 2nd  amu | 2nd  qualty  1 | 2nd  qualty  0 | 2nd  vpf |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [02:00] | R | dmb\_cfeb\_calibrate[2:0] | 0 | DMB calibration |
| [03] | R | dmb\_l1a\_release | 0 | DMB test |
| [08:04] | R | dmb\_reserved\_out[4:0] | 0 | DMB future use |
| [11:09] | R | dmb\_reserved\_in[2:0] | 0 | DMB future use |
| [15:12] | R | dmb\_rx\_ff[3:0] | 0 | DMB received |

Adr 42 ADR\_CFEB\_INJ CFEB Injector Control

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| inj  start | inj  mask  4 | inj  mask  3 | inj  mask  2 | inj  mask  1 | inj  mask  0 | inj  febsel  4 | inj  febsel  3 | inj  febsel  2 | inj  febsel  1 | inj  febsel  0 | mask  all  cfeb4 | mask  all  cfeb3 | mask  all  cfeb2 | mask  all  cfeb1 | mask  all  cfeb0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [04:00] | RW | mask\_all[4:0] | 111112 | 1=Enable, 0=Turn off CFEBn inputs  See Adr68 p43 |
| [09:05] | RW | inj\_febsel[4:0] | 0 | 1=Select CFEBn for RAM read/write |
| [14:10] | RW | injector\_mask[4:0] | 111112 | Enable CFEBn for injector trigger |
| [15] | RW | inj\_trig\_vme | 0 | Start pattern injector |

Adr 44 ADR\_CFEB\_INJ\_ADR CFEB Injector RAM Address

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| inj  adr  9 | inj  adr  8 | inj  adr  7 | inj  adr  6 | inj  adr  5 | inj  adr  4 | inj  adr  3 | inj  adr  2 | inj  adr  1 | inj  adr  0 | inj  ren  2 | inj  ren  1 | inj  ren  0 | inj  wen  2 | inj  wen  1 | inj  wen  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [02:00] | RW | inj\_wen[2:0] | 0 | 1=Write enable injector RAMn (Ly01,23,45) |
| [05:03] | RW | inj\_ren[2:0] | 0 | 1=Read enable Injector RAMn |
| [15:06] | RW | inj\_rwadr[9:0] | 0 | Injector RAM read/write address |

Adr 46 ADR\_CFEB\_INJ\_WDATA CFEB Injector Write Data

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| inj  wdata  15 | inj  wdata  14 | inj  wdata  13 | inj  wdata  12 | inj  wdata  11 | inj  wdata  10 | inj  wdata  9 | inj  wdata  8 | inj  wdata  7 | inj  wdata  6 | inj  wdata  5 | inj  wdata  4 | inj  wdata  3 | inj  wdata  2 | inj  wdata  1 | inj  wdata  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [07:00] | RW | inj\_wdata[7:0] | 0 | Triad bit for addressed Tbin Ly0 (or 2,4) |
| [15:08] | RW | inj\_wdata[15:8] | 0 | Triad bit for addressed Tbin Ly1 (or 3,5) |

Adr 48 ADR\_CFEB\_INJ\_RDATA CFEB Injector Read Data

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| inj  rdata  15 | inj  rdata  14 | inj  rdata  13 | inj  rdata  12 | inj  rdata  11 | inj  rdata  10 | inj  rdata  9 | inj  rdata  8 | inj  rdata  7 | inj  rdata  6 | inj  rdata  5 | inj  rdata  4 | inj  rdata  3 | inj  rdata  2 | inj  rdata  1 | inj  rdata  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [07:00] | R | inj\_rdata[7:0] | 0 | Triad bit for addressed Tbin Ly0 (or 2,4) |
| [15:08] | R | inj\_rdata[15:8] | 0 | Triad bit for addressed Tbin Ly1 (or 3,5) |

Adr 4A ADR\_HCM001 CFEB0 Ly0,Ly1 Hot Channel Mask

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ly1  distrip  7 | ly1  distrip  6 | ly1  distrip  5 | ly1  distrip  4 | ly1  distrip  3 | ly1  distrip  2 | ly1  distrip  1 | ly1  distrip  0 | ly0  distrip  7 | ly0  distrip  6 | ly0  distrip  5 | ly0  distrip  4 | ly0  distrip  3 | ly0  distrip  2 | ly0  distrip  1 | ly0  distrip  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [07:00] | RW | cfeb0\_ly0\_hcm[7:0] | 111111112 | 1=Enable DiStrip[7:0] Layer 0 |
| [15:08] | RW | cfeb0\_ly1\_hcm[7:0] | 111111112 | 1=Enable DiStrip[7:0] Layer 1 |

Adr 4C ADR\_HCM023 CFEB0 Ly2,Ly3 Hot Channel Mask

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| [07:00] | RW | cfeb0\_ly2\_hcm[7:0] | 111111112 | 1=Enable DiStrip[7:0] Layer 2 |
| [15:08] | RW | cfeb0\_ly3\_hcm[7:0] | 111111112 | 1=Enable DiStrip[7:0] Layer 3 |

Adr 4E ADR\_HCM045 CFEB0 Ly4,Ly5 Hot Channel Mask

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| [07:00] | RW | cfeb0\_ly4\_hcm[7:0] | 111111112 | 1=Enable DiStrip[7:0] Layer 4 |
| [15:08] | RW | cfeb0\_ly5\_hcm[7:0] | 111111112 | 1=Enable DiStrip[7:0] Layer 5 |

Adr 50 ADR\_HCM101 CFEB1 Ly0,Ly1 Hot Channel Mask

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| [07:00] | RW | cfeb1\_ly0\_hcm[7:0] | 111111112 | 1=Enable DiStrip[7:0] Layer 0 |
| [15:08] | RW | cfeb1\_ly1\_hcm[7:0] | 111111112 | 1=Enable DiStrip[7:0] Layer 1 |

Adr 52 ADR\_HCM123 CFEB1 Ly2,Ly3 Hot Channel Mask

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| [07:00] | RW | cfeb1\_ly2\_hcm[7:0] | 111111112 | 1=Enable DiStrip[7:0] Layer 2 |
| [15:08] | RW | cfeb1\_ly3\_hcm[7:0] | 111111112 | 1=Enable DiStrip[7:0] Layer 3 |

Adr 54 ADR\_HCM145 CFEB1 Ly4,Ly5 Hot Channel Mask

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| [07:00] | RW | cfeb1\_ly4\_hcm[7:0] | 111111112 | 1=Enable DiStrip[7:0] Layer 4 |
| [15:08] | RW | cfeb1\_ly5\_hcm[7:0] | 111111112 | 1=Enable DiStrip[7:0] Layer 5 |

Adr 56 ADR\_HCM201 CFEB2 Ly0,Ly1 Hot Channel Mask

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| [07:00] | RW | cfeb2\_ly0\_hcm[7:0] | 111111112 | 1=Enable DiStrip[7:0] Layer 0 |
| [15:08] | RW | cfeb2\_ly1\_hcm[7:0] | 111111112 | 1=Enable DiStrip[7:0] Layer 1 |

Adr 58 ADR\_HCM223 CFEB2 Ly2,Ly3 Hot Channel Mask

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| [07:00] | RW | cfeb2\_ly2\_hcm[7:0] | 111111112 | 1=Enable DiStrip[7:0] Layer 2 |
| [15:08] | RW | cfeb2\_ly3\_hcm[7:0] | 111111112 | 1=Enable DiStrip[7:0] Layer 3 |

Adr 5A ADR\_HCM245 CFEB2 Ly4,Ly5 Hot Channel Mask

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| [07:00] | RW | cfeb2\_ly4\_hcm[7:0] | 111111112 | 1=Enable DiStrip[7:0] Layer 4 |
| [15:08] | RW | cfeb2\_ly5\_hcm[7:0] | 111111112 | 1=Enable DiStrip[7:0] Layer 5 |

Adr 5C ADR\_HCM301 CFEB3 Ly0,Ly1 Hot Channel Mask

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ly1  distrip  7 | ly1  distrip  6 | ly1  distrip  5 | ly1  distrip  4 | ly1  distrip  3 | ly1  distrip  2 | ly1  distrip  1 | ly1  distrip  0 | ly0  distrip  7 | ly0  distrip  6 | ly0  distrip  5 | ly0  distrip  4 | ly0  distrip  3 | ly0  distrip  2 | ly0  distrip  1 | ly0  distrip  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [07:00] | RW | cfeb3\_ly0\_hcm[7:0] | 111111112 | 1=Enable DiStrip[7:0] Layer 0 |
| [15:08] | RW | cfeb3\_ly1\_hcm[7:0] | 111111112 | 1=Enable DiStrip[7:0] Layer 1 |

Adr 5E ADR\_HCM323 CFEB3 Ly2,Ly3 Hot Channel Mask

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| [07:00] | RW | cfeb3\_ly2\_hcm[7:0] | 111111112 | 1=Enable DiStrip[7:0] Layer 2 |
| [15:08] | RW | cfeb3\_ly3\_hcm[7:0] | 111111112 | 1=Enable DiStrip[7:0] Layer 3 |

Adr 60 ADR\_HCM345 CFEB3 Ly4,Ly5 Hot Channel Mask

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| [07:00] | RW | cfeb3\_ly4\_hcm[7:0] | 111111112 | 1=Enable DiStrip[7:0] Layer 4 |
| [15:08] | RW | cfeb3\_ly5\_hcm[7:0] | 111111112 | 1=Enable DiStrip[7:0] Layer 5 |

Adr 62 ADR\_HCM401 CFEB4 Ly0,Ly1 Hot Channel Mask

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| [07:00] | RW | cfeb4\_ly0\_hcm[7:0] | 111111112 | 1=Enable DiStrip[7:0] Layer 0 |
| [15:08] | RW | cfeb4\_ly1\_hcm[7:0] | 111111112 | 1=Enable DiStrip[7:0] Layer 1 |

Adr 64 ADR\_HCM423 CFEB4 Ly2,Ly3 Hot Channel Mask

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| [07:00] | RW | cfeb4\_ly2\_hcm[7:0] | 111111112 | 1=Enable DiStrip[7:0] Layer 2 |
| [15:08] | RW | cfeb4\_ly3\_hcm[7:0] | 111111112 | 1=Enable DiStrip[7:0] Layer 3 |

Adr 66 ADR\_HCM445 CFEB4 Ly4,Ly5 Hot Channel Mask

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| [07:00] | RW | cfeb4\_ly4\_hcm[7:0] | 111111112 | 1=Enable DiStrip[7:0] Layer 4 |
| [15:08] | RW | cfeb4\_ly5\_hcm[7:0] | 111111112 | 1=Enable DiStrip[7:0] Layer 5 |

Adr 68 ADR\_SEQ\_TRIG\_EN Sequencer Trigger Source Enables \*\*

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| cfeben  source | cfeben  4 | cfeben  3 | cfeben  2 | cfeben  1 | cfeben  0 | all  cfebs  active | ext  trig  inject | vme  trig | alct  ext  trig  en | clct  ext  trig  en | adb  ext  trig  en | adb  ext  trig  en | alct\*clct  match  trig  en | alct  pat  trig  en | clct  pat  trig  en |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [00] | RW | clct\_pat\_trig\_en | 1 | 1=Allow CLCT pattern triggers (CLCT Active FEB) |
| [01] | RW | alct\_pat\_trig\_en | 0 | 1=Allow ALCT pattern triggers (ALCT Active FEB) |
| [02] | RW | alct\_match\_trig\_en | 0 | 1=ALCT\*CLCT pattern triggers |
| [03] | RW | adb\_ext\_trig\_en | 0 | 1=Allow ADB external triggers from CCB |
| [04] | RW | dmb\_ext\_trig\_en | 0 | 1=Allow DMB external triggers |
| [05] | RW | clct\_ext\_trig\_en | 0 | 1=Allow CLCT external triggers (scintillator) from CCB |
| [06] | RW | alct\_ext\_trig\_en | 0 | 1=Allow ALCT external triggers from CCB |
| [07] | RW | vme\_ext\_trig | 0 | 1=Initiate Sequencer trigger (write 0 to recover) |
| [08] | RW | ext\_trig\_inject | 0 | 1=Change clct\_ext\_trig to fire pattern injector |
| [09] | RW | all\_cfebs\_active | 0 | 1=Make all CFEBs active when triggered |
| [14:10] | RW\* | cfeb\_en | 111112 | 1=Enable CFEB[n] to trigger and send active\_feb\_flag |
| [15] | RW | cfeb\_en\_source | 1 | 1=cfeb\_en set by mask\_all[4:0] in Adr 42, 0=set by 68 |

\* normally, cfeb\_en is copied from mask\_all in Adr42 so that masked-off cfebs do not trigger TMB or send active feb to DMB. That prevents the CFEB pattern injector from triggering, so setting\_cfeb\_en\_source=0, allows cfeb\_en to be written independently via Adr68[14:10].

\*\* See adr F0 p68 for layer-trigger mode

Adr 6A ADR\_SEQ\_TRIG\_DLY0 Sequencer Trigger Source Delays

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| adb  delay  3 | adb  delay  2 | adb  delay  1 | adb  delay  0 | alct  aff  delay  3 | Alct  aff  delay  2 | alct  aff  delay  1 | alct  aff  delay  0 | alct  pretrig  delay | alct  pretrig  delay  2 | alct  pretrig  delay  1 | alct  pretrig  delay  0 | alct  width  3 | alct  width  2 | alct  width  1 | alct  width  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [03:00] | RW | alct\_trig\_width[3:0] | 3 | ALCTCLCT Pre-trigger window width |
| [07:04] | RW | alct\_pre\_trig\_dly | 0 (2) | ALCT Pre-trigger delay for ALCT\*CLCT |
| [11:08] | RW | alct\_pat\_trig\_dly[3:0] | 0 | Delay alct\_pat\_trig (active feb flag from ALCT) |
| [15:12] | RW | adb\_ext\_trig\_dly[3:0] | 1 | Delay adb\_ext\_trig from CCB |

Adr 6C ADR\_SEQ\_TRIG\_DLY1 Sequencer Trigger Source Delays

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | alct  ext  delay  3 | alct  ext  delay  2 | alct  ext  delay  1 | alct  ext  delay  0 | clct  ext  delay  3 | clct  ext  delay  2 | clct  ext  delay  1 | clct  ext  delay  0 | dmb  ext  delay  3 | dmb  ext  delay  2 | dmb  ext  delay  1 | dmb  ext  delay  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [03:00] | RW | dmb\_ext\_trig\_dly[3:0] | 1 | Delay dmb\_ext\_trig from DMB |
| [07:04] | RW | clct\_ext\_trig\_dly[3:0] | 7 | Delay clct\_ext\_trig (scintillator) from CCB |
| [11:08] | RW | alct\_ext\_trig\_dly[3:0] | 7 | Delay alct\_ext\_trig from CCB |
| [15:12] | RW | - | 0 | Unused |

Adr 6E ADR\_SEQ\_ID Sequencer Board + CSC Ids

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | run  id  3 | run  id  2 | run  id  1 | run  id  0 | csd  id  3 | csd  id  2 | csd  id  1 | csd  id  0 | board  id  4 | board  id  3 | board  id  2 | board  id  1 | board  id  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [04:00] | RW | board\_id[4:0] | 21 | Board ID = VME Slot Geographic Adr |
| [08:05] | RW | csc\_id[3:0] | 5 | CSC Chamber ID number |
| [12:09] | RW | run\_id[3:0] | 0 | Run ID number |
| [15:13] | RW | -- | 0 | Unassigned |

Adr 70 ADR\_SEQ\_CLCT Sequencer CLCT Configuration

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| pretrig  halt | drft  delay  0 | drft  delay  0 | hit  thresh  post  2 | hit  thresh  post  1 | hit  thresh  post  0 | dmb  thresh  2 | dmb  thresh  1 | dmb  thresh  0 | hs  thresh  2 | hs  thresh  1 | hs  thresh  0 | triad  persist  3 | triad  persist  2 | triad  persist  1 | triad  persist  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [03:00] | RW | triad\_persist | 6 | Triad One-Shot Persistence (6=150ns) |
| [06:04] | RW | hit\_thresh\_pretrig[2:0] | 4 | Pattern hits pre-trigger threshold |
| [09:07] | RW | dmb\_thresh\_pretrig[2:0] | 4 | Minimum pattern hits 0-6 for DMB active-febs |
| [12:10] | RW | hit\_thresh\_postdrift[2:0] | 4 | Minimum pattern hits allowed after drift |
| [14:13] | RW | drift\_delay[1:0] | 2 | CSC Drift delay, number 25ns clock periods |
| [15] | RW | pretrig\_halt | 0 | Pretrigger and halt until unhalt arrives |

Adr 72 ADR\_SEQ\_FIFO Sequencer FIFO Configuration

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| bcb  read  enable | 0 | fifo  no  raw  hits | fifo  pretrig  4 | fifo  pretrig  3 | fifo  pretrig  2 | fifo  pretrig  1 | fifo  pretrig  0 | fifo  tbins  4 | fifo  tbins  3 | fifo  tbins  2 | fifo  tbins  1 | fifo  tbins  0 | fifo  mode  2 | fifo  mode  1 | fifo  mode  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [02:00] | RW | fifo\_mode[2:0] | 1 | FIFO Mode:  0=no CFEB raw hits full header  1=all CFEB raw hits full header  2=local CFEB raw hits full header  3=no CFEB raw hits short header  4=no CFEB raw hits no header |
| [07:03] | RW | fifo\_tbins[4:0] | 7 | Number FIFO time bins to read out |
| [12:08] | RW | fifo\_pretrig[4:0] | 2 | Number FIFO time bins before pretrigger |
| [13] | RW | fifo\_no\_raw\_hits | 0 | 1=do not wait to store raw hits [a no\_daq mode] |
| [14] | RW | -- | 0 | Unassigned |
| [15] | RW | bcb\_read\_enable | 0 | 1=enable cfeb blocked distrip bits in dmb readout |

Adr 74 ADR\_SEQ\_L1A Sequencer L1A Configuration

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| l1a  intern  dly  2 | l1a  intern  dly  1 | l1a  intern  dly  0 | l1a  intern | l1a  windo  3 | l1a  windo  2 | l1a  windo  1 | l1a  windo  0 | l1a  delay  7 | l1a  delay  6 | l1a  delay  5 | l1a  delay  4 | l1a  delay  3 | l1a  delay  2 | l1a  delay  1 | l1a  delay  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [07:00] | RW | l1a\_delay[7:0] | 12810 | Level1 Accept delay from pretrig status output |
| [11:08] | RW | l1a\_window[3:0] | 3 | Level1 Accept window width after delay |
| [12] | RW | l1a\_internal | 0 | Generate internal Level 1, overrides external |
| [15:13] | RW | l1a\_internal\_dly[2:0] | 0 | Window position for internal L1A |

Adr 76 ADR\_SEQ\_OFFSET0 Sequencer Counter Offsets

(see Adr10A p72 for L1A bxn offset)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| bxn  offset  11 | bxn  offset  10 | bxn  offset  9 | bxn  offset  8 | bxn  offset  7 | bxn  offset  6 | bxn  offset  5 | bxn  offset  4 | bxn  offset  3 | bxn  offset  2 | bxn  offset  1 | bxn  offset  0 | l1a  offset  3 | l1a  offset  2 | l1a  offset  1 | l1a  offset  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [03:00] | RW | l1a\_offset[3:0] | 0 | L1A counter preset value |
| [15:04] | RW | bxn\_offset\_pretrig[11:0] | 0 | BXN offset at reset for pretrigger bxn |

Adr 78 ADR\_SEQ\_CLCT0 Sequencer Latched CLCT0 (LSBs)

(Split with Adr B0 ADR\_SEQCLCTM)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| hs  key  7 | hs  key  6 | hs  key  5 | hs  key  4 | hst  key  3 | hs  key  2 | hs  key  1 | hs  key  0 | hs pid  3 | hs pid  2 | hs pid  1 | hs pid  0 | hs hits  2 | hs hits  1 | hs hits  0 | vpf |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | | Description | |
| [00] | R | clct0[0] clct\_1st\_valid | | 1 | | Valid pattern flag |
| [03:01] | R | clct0[3:1] hs\_hit\_1st[2:0] | | 4-6 | | Hits on pattern: 0 to 6 |
| [07:04] | R | clct0[7:4] hs\_pid\_1st[3:0] | | 0-10 | | Pattern shape 0 to 10 |
| [15:08] | R | clct0[15:8] hs\_key\_1st[7:0] | | 0-15910 | | Key ½-strip |

Adr 7A ADR\_SEQ\_CLCT1 Sequencer Latched CLCT1 (LSBs)

(Split with Adr B0 ADR\_SEQCLCTM)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| hs  key  7 | hs  key  6 | hs  key  5 | hs  key  4 | hst  key  3 | hs  key  2 | hs  key  1 | hs  key  0 | hs pid  3 | hs pid  2 | hs pid  1 | hs pid  0 | hs hits  2 | hs hits  1 | hs hits  0 | vpf |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [00] | R | clct1[0] clct\_2nd\_valid | 1 | Valid pattern flag |
| [03:01] | R | clct1[3:1] hs\_hit\_2nd[2:0] | 4-6 | Hits on pattern: 0 to 6 |
| [07:04] | R | clct1[7:4] hs\_pid\_2nd[3:0] | 0-10 | Pattern shape 0 to 10 |
| [15:08] | R | clct1[15:8] hs\_key\_2nd[7:0] | 0-15910 | Key ½-strip |

Adr 7C ADR\_SEQ\_TRIG\_SRC Sequencer Trigger Source Read-back

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | me1b  pretrig | me1a  pre  trig | layer  trig | vme  trig | alct  ext  trig  en | clct  ext  trig  en | adb  ext  trig  en | adb  ext  trig  en | alct\*clct  pat  trig  en | alct  pat  trig  en | clct  pat  trig  en |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [00] | R | clct\_pat\_trig\_en | 1 | CLCT pattern triggered sequencer |
| [01] | R | alct\_pat\_trig\_en | 0 | ALCT pattern triggered sequencer |
| [02] | R | alct\_match\_trig\_en | 0 | ALCT\*CLCT pattern triggered sequencer |
| [03] | R | adb\_ext\_trig\_en | 0 | ADB external triggered sequencer |
| [04] | R | dmb\_ext\_trig\_en | 0 | DMB external triggered sequencer |
| [05] | R | clct\_ext\_trig\_en | 0 | CLCT (CCB scintillator) external triggered sequencer |
| [06] | R | alct\_ext\_trig\_en | 0 | ALCT (CCB) external triggered sequencer |
| [07] | R | vme\_ext\_trig | 0 | VME triggered sequencer |
| [08] | R | layer\_trig | 0 | Layer trigger |
| [09] | R | me1a\_only\_pretrig | 0 | CLCT pattern trigger was on ME1A only |
| [10] | R | me1b\_only\_pretrig | 0 | CLCT pattern trigger was on ME1B only |
| [13:11] | R | -- | 0 | Unassigned |

Adr 7E ADR\_DMB\_RAM\_ADR Sequencer RAM Address

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| dmb  wdata  17 | dmb  wdata  16 | dmb  reset | dmb  wr | dmb  adr  11 | dmb  adr  10 | dmb  adr  9 | dmb  adr  8 | dmb  adr  7 | dmb  adr  6 | dmb  adr  5 | dmb  adr  4 | dmb  adr  3 | dmb  adr  2 | dmb  adr  1 | dmb  adr  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [11:00] | RW | dmb\_adr[11:0] | 0 | Raw hits RAM VME read/write address |
| [12] | RW | dmb\_wr | 0 | Raw hits RAM VME write enable |
| [13] | RW | dmb\_reset | 0 | Raw hits RAM VME address reset |
| [15:14] | RW | dmb\_wdata[17:16] | 0 | Raw hits RAM VME write data MSBs |

Adr 80 ADR\_DMB\_RAM\_WDATA Sequencer RAM Write Data

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| dmb  wdata  15 | dmb  wdata  14 | dmb  wdata  13 | dmb  wdata  12 | dmb  wdata  11 | dmb  wdata  10 | dmb  wdata  9 | dmb  wdata  8 | dmb  wdata  7 | dmb  wdata  6 | dmb  wdata  5 | dmb  wdata  4 | dmb  wdata  3 | dmb  wdata  2 | dmb  wdata  1 | dmb  wdata  16 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [15:00] | RW | dmb\_wdata[15:0] | 0 | Raw hits RAM VME write data (msb in adr 76) |

Adr 82 ADR\_DMB\_RAM\_WDCNT Sequencer RAM Word Count

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | dmb  busy | dmb  rdata  17 | dmb  wdata  16 | dmb  wdcnt  11 | dmb  wdcnt  10 | dmb  wdcnt  9 | dmb  wdcnt  8 | dmb  wdcnt  7 | dmb  wdcnt  6 | dmb  wdcnt  5 | dmb  wdcnt  4 | dmb  wdcnt  3 | dmb  wdcnt  2 | dmb  wdcnt  1 | dmb  wdcnt  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [11:00] | R | dmb\_wdcnt[11: 0] | 0 | Raw hits RAM VME word count |
| [13:12] | R | dmb\_rdata[17:16]; | 0 | Raw hits RAM VME read data MSBs |
| [14] | R | dmb\_busy | 0 | Raw hits RAM VME |
| [15] | R | -- | 0 | Unassigned |

Adr 84 ADR\_DMB\_RAM\_RDATA Sequencer RAM Read Data

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| dmb  rdata  15 | dmb  rdata  14 | dmb  rdata  13 | dmb  rdata  12 | dmb  rdata  11 | dmb  rdata  10 | dmb  rdata  9 | dmb  rdata  8 | dmb  rdata  7 | dmb  rdata  6 | dmb  rdata  5 | dmb  rdata  4 | dmb  rdata  3 | dmb  rdata  2 | dmb  rdata  1 | dmb  rdata  16 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [15:00] | R | dmb\_rdata[15:0] | 0 | Raw hits RAM VME read data (msb in adr 7A) |

Adr 86 ADR\_TMB\_TRIG TMB Trigger Configuration / MPC Accept

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| mpc  oe | mpc  idle  blank | mpc  sel\_ttc  bx0 | mpc  reserved  1 | mpc  reserved  0 | mpc  accept  1 | mpc  accept  0 | mpc  delay  3 | mpc  delay  2 | mpc  delay  1 | mpc  delay  0 | allow  clct+alct  match | allow  clct  only | allow  alct  only | sync  err en  1 | sync  err en  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [01:00] | RW | tmb\_sync\_err\_en[1:0] | 112 | Allow sync\_err to MPC for either muon |
| [02] | RW | tmb\_allow\_alct | 0 | Allow ALCT-only L1A (not used in current version) |
| [03] | RW | tmb\_allow\_clct | 1 | Allow CLCT0-only L1A |
| [04] | RW | tmb\_allow\_match | 1 | Allow ALCT+CLCT match pre-trigger |
| [08:05] | RW | mpc\_rx\_delay[3:0] | 7 | MPC accept response delay |
| [10:09] | R | mpc\_accept[1:0] | - | MPC accept latched after delay |
| [12:11] | R | mpc\_reserved[1:0] | - | MPC reserved latched after delay |
| [13] | RW | mpc\_sel\_ttc\_bx0 | 1 | 1=MPC gets ttc\_bx0, 0=bx0\_local |
| [14] | RW | mpc\_idle\_blank | 0 | 1=blank mpc data & bx0 except when triggered |
| [15] | RW | mpc\_oe | 1 | 1=enable outputs to MPC, 0=aset FFs to 1s |

Adr 88 ADR\_MPC0\_FRAME0 MPC0 Frame0 Data Sent to MPC

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 1st  vpf | lct  1st q  3 | lct  1st q  2 | lct  1st q  1 | lct  1st q  0 | clct  1st pat  3 | clct  1st pat  2 | clct  1st pat  1 | clct  1st pat  0 | alct  1st wg  6 | alct  1st wg  5 | alct  1st wg  4 | alct  1st wg  3 | alct  1st wg  2 | alct  1st wg  1 | alct  1st wg  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [06:00] | R | alct\_first\_key[6:0] | 0-11110 | ALCT first key wire-group |
| [10:07] | R | clct\_first\_pat[3:0] | 0-10 | CLCT first pattern number |
| [14:11] | R | lct\_first\_quality[3:0] | 8 | LCT first muon quality |
| [15] | R | first\_vpf | 1 | First valid pattern flag |

Adr 8A ADR\_MPC0\_FRAME1 MPC0 Frame1 Data Sent to MPC

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| csc  id  3 | csc  id  2 | csc  id  1 | csc  id  0 | tmb  bx0  local | alct  1st  bxn  0 | sync  err | clct  1st  bend | clct  1st  key  7 | clct  1st  key  6 | clct  1st  key  5 | clct  1st  key  4 | clct  1st  key  3 | clct  1st  key  2 | clct  1st  key  1 | clct  1st  key  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [07:00] | R | clct\_first\_key[7:0] | 0-15910 | CLCT first muon key ½-strip |
| [08] | R | clct\_first\_bend | 0 | CLCT first muon bend direction |
| [09] | R | sync\_err | 0 | BXN does not match at BX0 |
| [10] | R | alct\_first\_bxn[0] | 0-1 | ALCT first muon bunch crossing number |
| [11] | R | clct\_first\_bx0\_local | 0-1 | 1=TMBs bxn[11:0]==0 |
| [15:12] | R | csc\_id[3:0] | 1-9 | CSC chamber ID |

Adr 8C ADR\_MPC1\_FRAME0 MPC1 Frame0 Data Sent to MPC

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 2nd  vpf | lct  2nd q  3 | lct  2nd q  2 | lct  2nd q  1 | lct  2nd q  0 | clct  2nd pat  3 | clct  2nd pat  2 | clct  2nd pat  1 | clct  2nd pat  0 | alct  2nd wg  6 | alct  2nd wg  5 | alct  2nd wg  4 | alct  2nd wg  3 | alct  2nd wg  2 | alct  2nd wg  1 | alct  2nd wg  0 |

5

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [06:00] | R | alct\_second\_key[6:0] | 0-11110 | ALCT second key wire-group |
| [10:07] | R | clct\_second\_pat[3:0] | 0-10 | CLCT second pattern number |
| [14:11] | R | lct\_second\_quality[3:0] | 8 | LCT second muon quality |
| [15] | R | second\_vpf | 1 | Second valid pattern flag |

Adr 8E ADR\_MPC1\_FRAME1 MPC1 Frame1 Data Sent to MPC

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| csc  id  3 | csc  id  2 | csc  id  1 | csc  id  0 | tmb  bx0  local | alct  2nd  bxn  0 | sync  err | clct  2nd  bend | clct  2nd  key  7 | clct  2nd  key  6 | clct  2nd  key  5 | clct  2nd  key  4 | clct  2nd  key  3 | clct  2nd  key  2 | clct  2nd  key  1 | clct  2nd  key  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [07:00] | R | clct\_second\_key[7:0] | 0-15910 | CLCT second muon key ½-strip |
| [08] | R | clct\_second\_bend | 0 | CLCT second muon bend direction |
| [09] | R | sync\_err | 0 | BXN does not match at BX0 |
| [10] | R | alct\_second\_bxn[0] | 0-1 | ALCT second muon bunch crossing number |
| [11] | R | clct\_second\_bx0\_local | 0-1 | 1=TMBs bxn[11:0]==0 |
| [15:12] | R | csc\_id[3:0] | 1-9 | CSC chamber ID |

Adr 90 ADR\_MPC\_INJ MPC Injector Control

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| mpc  inj  clct  bx0 | mpc  inj  alct  bx0 | mpc  reserv  1 | mpc  reserv  0 | mpc  accept  1 | mpc  accept  0 | ttc  inj  enable | mpc  inject | mpc  nfram  7 | mpc  nfram  6 | mpc  nfram  5 | mpc  nfram  4 | mpc  nfram  3 | mpc  nfram  2 | mpc  nfram  1 | mpc  nfram  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [07:00] | RW | mpc\_nframes[7:0] | 5 | Number frames to inject |
| [08] | RW | mpc\_inject | 0 | 1=Start MPC test pattern injector |
| [09] | RW | ttc\_mpc\_inj\_en | 1 | 1=Enable injector start by TTC command |
| [11:10] | R | mpc\_accept[1:0] | - | MPC accept stored at injector RAM address |
| [13:12] | R | mpc\_reserved[1:0] | - | MPC reserved stored at injector RAM address |
| [14] | RW | mpc\_inj\_alct\_bx0 | 0 | 1=Fire alct\_bx0 one-shot |
| [15] | RW | mpc\_inj\_clct\_bx0 | 0 | 1=Fire clct\_bx0 one-shot |

Adr 92 ADR\_MPC\_RAM\_ADR MPC Injector RAM Address

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| mpc  adr  7 | mpc  adr  6 | mpc  adr  5 | mpc  adr  4 | mpc  adr  3 | mpc  adr  2 | mpc  adr  1 | mpc  adr  0 | mpc  ren  3 | mpc  ren  2 | mpc  ren  1 | mpc  ren  0 | mpc  wen  3 | mpc  wen  2 | mpc  wen  1 | mpc  wen  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [03:00] | RW | mpc\_wen[3:0] | 0 | Select RAM to write |
| [07:04] | RW | mpc\_ren[3:0] | 0 | Select RAM to read |
| [15:08] | RW | mpc\_adr[7:0] | 0 | Injector RAM read/write address |

Adr 94 ADR\_MPC\_RAM\_WDATA MPC Injector RAM Write Data

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| mpc  wdata  7 | mpc  wdata  6 | mpc  wdata  5 | mpc  wdata  4 | mpc  wdata  3 | mpc  wdata  2 | mpc  wdata  1 | mpc  wdata  0 | mpc  wdata  3 | mpc  wdata  2 | mpc  wdata  1 | mpc  wdata  0 | mpc  wdata  3 | mpc  wdata  2 | mpc  wdata  1 | mpc  wdata  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [15:00] | RW | mpc\_wdata[15:0] | 0 | MPC Injector RAM write data |

Adr 96 ADR\_MPC\_RAM\_RDATA MPC Injector RAM Read Data

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| mpc  rdata  7 | mpc  rdata  6 | mpc  rdata  5 | mpc  rdata  4 | mpc  rdata  3 | mpc  rdata  2 | mpc  rdata  1 | mpc  rdata  0 | mpc  rdata  3 | mpc  rdata  2 | mpc  rdata  1 | mpc  rdata  0 | mpc  rdata  3 | mpc  rdata  2 | mpc  rdata  1 | mpc  rdata  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [15:00] | R | mpc\_rdata[15:0] | 0 | MPC Injector RAM read data |

Adr 98 ADR\_SCP\_CTRL Scope Control

(see Adr9A p50 SCP\_RDATA and adr CE p60 SCP\_TRIG)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 |  | trig  done | waitin  for  trigger | ram  sel  3 | ram  sel  2 | ram  sel  1 | ram  sel  0 | tbins  2 | tbins  1 | tbins  0 | no  write | auto | force  trig | run  stop | trig en |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [00] | RW | scp\_ch\_trig\_en | 1 | 1=Enable channel triggers, see AdrCE p60 for ch |
| [01] | RW | scp\_runstop | 0 | 1=Run, 0=Stop |
| [02] | RW | scp\_force\_trig | 0 | 1=Force a trigger (to trig: set 0,1,0 in 3 writes) |
| [03] | RW | scp\_auto | 0 | Sequencer readout mode 1=insert in DMB data |
| [04] | RW | scp\_nowrite | 0 | 1=Preserve initial RAM test pattern for debug |
| [07:05] | RW | scp\_tbins[2:0] | 4 | Auto mode tbins per channel code,  actual tbins/ch=(scp\_tbins+1)\*64, spans 64-512 |
| [11:08] | RW | scp\_ram\_sel[3:0] | 0 | RAM bank address 0-9 for VME readout |
| [12] | R | scp\_waiting | - | Scope waiting for trigger |
| [13] | R | scp\_trig\_done | - | Scope triggered, ready for readout |
| [15:14] | RW | - |  | Unassigned |

Adr 9A ADR\_SCP\_RDATA Scope Read data

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| rdata  15 | rdata  14 | rdata  13 | rdata  12 | rdata  11 | rdata  10 | rdata  9 | radr8  rdata8 | radr7  rdata7 | radr6  rdata6 | radr5  rdata5 | radr4  rdata4 | radr3  rdata3 | radr2  rdata2 | radr1  rdata1 | radr0  rdata0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal |  | Description |
| [08:00] | W | scp\_radr[8:0] |  | Scope data read address=tbin for selected RAM |
| [15:00] | R | scp\_rdata[15:0] |  | See channel assignments below |

Scope Channel Assignments

// Pre-trigger to DMB

assign scp\_ch[0] = (clct\_sm == pretrig); // Trigger alignment marker, scope triggers on this ch usually

assign scp\_ch[1] = triad\_tp[0]; // Triad test point at input to raw hits RAM

assign scp\_ch[2] = any\_cfeb\_hit; // Any CFEB over threshold

assign scp\_ch[3] = active\_feb\_flag; // Active feb flag to DMB

assign scp\_ch[8:4] = active\_feb\_list[4:0]; // Active feb list to DMB

// Pre-trigger CLCT\*ALCT matching

assign scp\_ch[9] = alct\_active\_feb; // ALCT active feb flag, should precede alct0\_vpf

assign scp\_ch[10] = alct\_pretrig\_window; // ALCT\*CLCT pretrigger matching window

// Pre-trigger Processing

assign scp\_ch[13:11] = clct\_sm\_vec[2:0]; // Pre-trigger state machine

assign scp\_ch[14] = wr\_buf\_ready; // Write buffer ready

assign scp\_ch[15] = (clct\_sm == pretrig); // Skip channels 15,31,47,63,79,95,111,127,143,159

assign scp\_ch[27:16] = bxn\_counter[11:0]; // BXN counter

assign scp\_ch[28] = discard\_nowrbuf; // Event discard, no write buffer

// CLCT Pattern Finder Output

assign scp\_ch[29] = 0;

assign scp\_ch[30] = 0;

assign scp\_ch[31] = (clct\_sm == pretrig); // Skip channels 15,31,47,63,79,95,111,127,143,159

assign scp\_ch[34:32] = hs\_hit\_1st[2:0]; // CLCT0 number hits after drift

assign scp\_ch[38:35] = hs\_pid\_1st[3:0]; // CLCT0 Pattern number

assign scp\_ch[46:39] = hs\_key\_1st[7:0]; // CLCT0 ½-strip ID number

assign scp\_ch[47] = (clct\_sm == pretrig); // Skip channels 15,31,47,63,79,95,111,127,143,159

assign scp\_ch[50:48] = hs\_hit\_2nd[2:0]; // CLCT1 number hits after drift

assign scp\_ch[54:51] = hs\_pid\_2nd[3:0]; // CLCT1 Pattern number

assign scp\_ch[62:55] = hs\_key\_2nd[7:0]; // CLCT1 ½-strip ID number

assign scp\_ch[63] = (clct\_sm == pretrig); // Skip channels 15,31,47,63,79,95,111,127,143,159

// CLCT Builder

assign scp\_ch[64] = clct0\_really\_valid; // CLCT0 is over threshold, not forced by an external trigger

assign scp\_ch[65] = clct0\_vpf; // CLCT0 vpf

assign scp\_ch[66] = clct1\_vpf; // CLCT1 vpf

assign scp\_ch[67] = clct\_push\_xtmb; // CLCT sent to TMB matching

assign scp\_ch[68] = discard\_invp; // CLCT discarded, below threshold after drift

// TMB Matching

assign scp\_ch[69] = alct0\_valid; // ALCT0 vpf direct from 80MHz receiver, before alct\_delay

assign scp\_ch[70] = alct1\_valid; // ALCT1 vpf direct from 80MHz receiver, before alct\_delay

assign scp\_ch[71] = alct\_vpf\_tprt; // ALCT vpf in TMB after pipe delay, unbuffered real time

assign scp\_ch[72] = clct\_vpf\_tprt; // CLCT vpf in TMB

assign scp\_ch[73] = clct\_window\_tprt; // CLCT matching window in TMB

assign scp\_ch[77:74] = tmb\_match\_win[3:0]; // Location of alct in clct window

assign scp\_ch[78] = tmb\_alct\_discard; // ALCT pair was not used for LCT

assign scp\_ch[79] = (clct\_sm == pretrig); // Skip channels 15,31,47,63,79,95,111,127,143,15

assign scp\_ch[80] = tmb\_clct\_discard; // CLCT pair was not used for LCT

// TMB Match Results

assign scp\_ch[81] = tmb\_trig\_pulse; // TMB Triggered on ALCT or CLCT or both

assign scp\_ch[82] = tmb\_trig\_keep; // ALCT or CLCT or both triggered, and trigger is allowed

assign scp\_ch[83] = tmb\_match; // ALCT and CLCT matched in time

assign scp\_ch[84] = tmb\_alct\_only; // Only ALCT triggered

assign scp\_ch[85] = tmb\_clct\_only; // Only CLCT triggered

assign scp\_ch[86] = discard\_tmbreject; // TMB discarded event

// MPC

assign scp\_ch[87] = mpc\_xmit\_lct0; // MPC LCT0 sent

assign scp\_ch[88] = mpc\_xmit\_lct1; // MPC LCT1 sent

assign scp\_ch[89] = mpc\_response\_ff; // MPC accept is ready

assign scp\_ch[91:90] = mpc\_accept\_ff[1:0]; // MPC muon accept response

// L1A

assign scp\_ch[92] = l1a\_pulse; // L1A strobe from ccb or internal

assign scp\_ch[93] = l1a\_window\_open; // L1A window open duh

assign scp\_ch[94] = l1a\_match; // L1A strobe match in window

assign scp\_ch[95] = (clct\_sm == pretrig); // Skip channels 15,31,47,63,79,95,111,127,143,159

// Buffer push at L1A

assign scp\_ch[96] = buf\_push; // Allocate write buffer space for this event

assign scp\_ch[103:97] = buf\_push\_adr[6:0]; // Address of write buffer to allocate

// DMB Readout

assign scp\_ch[104] = dmb\_dav; // DAV to DMB

assign scp\_ch[105] = dmb\_busy; // Readout in progress

assign scp\_ch[110:106] = read\_sm\_vec[4:0]; // Readout state machine

assign scp\_ch[111] = (clct\_sm == pretrig); // Skip channels 15,31,47,63,79,95,111,127,143,159

assign scp\_ch[126:112] = seq\_wdata[14:0]; // DMB dump image, very cool

assign scp\_ch[127] = (clct\_sm == pretrig); // Skip channels 15,31,47,63,79,95,111,127,143,159

assign scp\_ch[128] = seq\_wdata[15]; // DMB dump image, very cool

// CLCT+TMB Pipelines

assign scp\_ch[132:129] = wr\_buf\_adr[3:0]; // Event address counter

assign scp\_ch[133] = wr\_push\_xtmb; // Buffer write strobe after drift time

assign scp\_ch[137:134] = wr\_adr\_xtmb[3:0]; // Buffer write address after drift time

assign scp\_ch[138] = wr\_push\_rtmb; // Buffer write strobe at TMB matching time

assign scp\_ch[142:139] = wr\_adr\_rtmb[3:0]; // Buffer write address at TMB matching time

assign scp\_ch[143] = (clct\_sm == pretrig); // Skip channels 15,31,47,63,79,95,111,127,143,159

assign scp\_ch[144] = wr\_push\_xmpc; // Buffer write strobe at MPC xmit to sequencer

assign scp\_ch[148:145] = wr\_adr\_xmpc[3:0]; // Buffer write address at MPC xmit to sequencer

assign scp\_ch[149] = wr\_push\_rmpc; // Buffer write strobe at MPC received

assign scp\_ch[153:150] = wr\_adr\_rmpc[3:0]; // Buffer write address at MPC received

// Buffer pop at readout completion

assign scp\_ch[154] = buf\_pop; // Specified buffer is to be released

assign scp\_ch[158:155] = buf\_pop\_adr[3:0]; // Address of read buffer to release

assign scp\_ch[159] = (clct\_sm == pretrig); // Skip channels 15,31,47,63,79,95,111,127,143,159

Adr 9C ADR\_CCB\_CMD CCB TTC Command Generator (Internal)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ccb  cmd  7 | ccb  cmd  6 | ccb  cmd  5 | ccb  cmd  4 | ccb  cmd  3 | ccb  cmd  2 | ccb  cmd  1 | ccb  cmd  0 | 0 | fmm  state  2 | fmm  state  1 | fmm  state  0 | subadr  strobe | data  strobe | brcst  strobe | dis  con  ccb |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [00] | RW | vme\_ccb\_cmd\_enable | 0 | 1=Disconnect CCB backplane ccb\_cmd[7:0] |
| [01] | RW | vme\_ccb\_cmd\_strobe | 0 | 1=Assert internal ccb\_cmd brcst strobe |
| [02] | RW | vme\_ccb\_data\_strobe | 0 | 1=Assert internal ccb\_cmd data strobe |
| [03] | RW | vme\_ccb\_subaddr\_strobe | 0 | 1=Assert internal ccb\_cmd sub-adr strobe |
| [06:04] | R | fmm\_state[2:0] | - | FMM machine states:  0: fmm\_startup  1: fmm\_resync  2: fmm\_stop  3: fmm\_wait\_bx0  4 : fmm\_run |
| [07] | RW | - |  | Unassigned |
| [15:08] | RW | vme\_ccb\_cmd[7:0] | 0 | TTC command to generate |

Adr 9E ADR\_BUF\_STAT0 Buffer Status

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| buffer  disp  7 | buffer  disp  6 | buffer  disp  5 | buffer  disp  4 | buffer  disp  3 | buffer  disp  2 | buffer  disp  1 | buffer  disp  0 | buf  stalled  once | buf  q  adrerr | buf  q  udferr | buf  q  ovferr | buf  q  empty | buf  q  full | buf  stalled | wr  buf  ready |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [00] | R | wr\_buf\_ready | 1 | Write buffer is ready |
| [01] | R | buf\_stalled | 0 | Buffer write pointer hit a fence and stalled |
| [02] | R | buf\_q\_full | 0 | All raw hits ram in use, ram writing must stop |
| [03] | R | buf\_q\_empty | 0 | No fences remain in buffer queue |
| [04] | R | buf\_q\_ovf\_err | 0 | Tried to push new event when queue full |
| [05] | R | buf\_q\_udf\_err | 0 | Tried to pop event when queue empty |
| [06] | R | buf\_q\_adr\_err | 0 | Fence adr popped from queue doesn’t match expected adr |
| [07] | R | buf\_stalled\_once | 0 | Buffer stalled at least once since last resync |
| [15:08] | R | buf\_display[7:0] | 0 | Buffer fraction in use, for in-board LED display |

Adr A0 ADR\_BUF\_STAT1 Buffer Status

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | buf  adr  10 | buf  adr  9 | buf  adr  8 | buf  adr  7 | buf  adr  6 | buf  adr  5 | buf  adr  4 | buf  adr  3 | buf  adr  2 | buf  adr  1 | buf  adr  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [10:00] | R | wr\_buf\_adr[10:0] | - | Current address of event & header write buffer |
| [15:11] | R | - | 0 | Unassigned |

Adr A2 ADR\_BUF\_STAT2 Buffer Status

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | buf  fence  dist  10 | buf  fence  dist  9 | buf  fence  dist  8 | buf  fence  dist  7 | buf  fence  dist  6 | buf  fence  dist  5 | buf  fence  dist  4 | buf  fence  dist  3 | buf  fence  dist  2 | buf  fence  dist  1 | buf  fence  dist  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [10:00] | R | buf\_fence\_dist[10:0] | - | Distance to 1st fence address |
| [15:11] | R | - | 0 | Unassigned |

Adr A4 ADR\_BUF\_STAT3 Buffer Status

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | buf  fence  cntr  11 | buf  fence  cnt  10 | buf  fence  cnt  9 | buf  fence  cnt  8 | buf  fence  cnt  7 | buf  fence  cnt  6 | buf  fence  cnt  5 | buf  fence  cnt  4 | buf  fence  cnt  3 | buf  fence  cnt  2 | buf  fence  cnt  1 | buf  fence  cnt  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [11:00] | R | buf\_fence\_cnt[11:0] | - | Number of fences in fence RAM currently |
| [15:12] | R | - | 0 | Unassigned |

Adr A6 ADR\_BUF\_STAT4 Buffer Status

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | buf  fence  peak  11 | buf  fence  peak  10 | buf  fence  peak  9 | buf  fence  peak  8 | buf  fence  peak  7 | buf  fence  peak  6 | buf  fence  peak  5 | buf  fence  peak  4 | buf  fence  peak  3 | buf  fence  peak  2 | buf  fence  peak  1 | buf  fence  peak  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [11:00] | R | buf\_fence\_cnt\_peak [11:0] | - | Peak number of fences in fence RAM |
| [15:12] | R | - | 0 | Unassigned |

Adr A8 ADR\_ALCTFIFO1 ALCT Raw Hits RAM Control

(Split with Adr 3E ADR\_ALCT\_FIFO0 and Adr A4 ADR\_ALCT\_FIFO2)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | alct  demux  mode | 0 | alct  radr  10 | alct  radr  9 | alct  radr  8 | alct  radr  7 | alct  radr  6 | alct  radr  5 | alct  radr  4 | alct  radr  3 | alct  radr  2 | alct  radr  1 | alct  radr  0 | alct  raw  reset |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [00] | RW | alct\_raw\_reset | 0 | Reset ALCT raw hits FIFO controller |
| [11:01] | RW | alct\_raw\_radr[10:0] | 0 | ALCT raw hits RAM read address or demux wd |
| [12] | RW | -- | 0 | Unassigned |
| [13] | RW | alct\_demux\_mode | 0 | 0=alctfifo2 has RAM data, 1=fifo2=demux data |
| [15:14] | RW | -- | 0 | Unassigned |

Adr AA ADR\_ALCTFIFO2 ALCT Raw Hits RAM data (LSBs)

(Split with Adr 3E ADR\_ALCT\_FIFO0 and Adr A2 ADR\_ALCT\_FIFO1)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| alct  fifo  15 | alct  fifo  14 | alct  fifo  13 | alct  fifo  12 | alct  fifo  11 | alct  fifo  10 | alct  fifo  9 | alct  fifo  8 | alct  fifo  7 | alct  fifo  6 | alct  fifo  5 | alct  fifo  4 | alct  fifo  3 | alct  fifo  2 | alct  fifo  1 | alct  fifo  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [15:00] | R | alct\_raw\_rdata[15:0]  OR alct\_1st\_vme[14:1]  alct\_1st\_vme[28:15]  alct\_2nd\_vme[14:1]  alct\_2nd\_vme[28:15] |  | ALCT FIFO data (msbs in adr\_alct\_fifo)  alct\_raw\_radr=0 and alct\_demux\_mode=1  alct\_raw\_radr=1  alct\_raw\_radr=2  alct\_raw\_radr=3 |

Adr AC ADR\_SEQMOD Sequencer Trigger Modifiers

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| event  clear  vme | active  feb  src | Scint  veto  state | Clear  scint  veto | L1A  alct  only | L1A  tmb  nol1a | L1A  no  tmb | L1A  tmb  trig | valid  clct  requir | wr  buf  requir | hdr  wr  cont | wrbuf  auto  clr | flush  timer  3 | flush  timer  2 | flush  timer  1 | flush  timer  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [03:00] | RW | clct\_flush\_delay[3:0] | 1 | Trigger sequencer flush state timer |
| [04] | RW | wr\_buf\_autoclr\_en | 1 | 1=Enable frozen buffer auto clear |
| [05] | RW | hdr\_wr\_continuous | 0 | 1=allow continuous header buffer writing for invalid triggers |
| [06] | RW | wr\_buf\_required | 1 | Require wr\_buffer available to pre-trigger |
| [07] | RW | valid\_clct\_required | 1 | Require valid CLCT after drift delay |
| [08] | RW | l1a\_allow\_match | 1 | Readout allows tmb trig pulse in L1A window |
| [09] | RW | l1a\_allow\_notmb | 0 | Readout allows notmb trig pulse in L1A window |
| [10} | RW | l1a\_allow\_nol1a | 0 | Readout allows tmb trig pulse outside L1A wind |
| [11] | RW | l1a\_allow\_alct\_only | 0 | Allow ALCT-only events to readout at L1A |
| [12] | RW | scint\_veto\_clr | 0 | Clear scintillator veto FF |
| [13] | R | scint\_veto\_vme | 0 | Scintillator veto FF state |
| [14] | RW | active\_feb\_src | 0 | Active feb flag source, 0=pretrig, 1=tmb match |
| [15] | RW | event\_clear\_vme | 0 | Event clear for aff,clct,mpc VME diagnostic registers |

Adr AE ADR\_SEQSM Sequencer Machine State

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | buf\_q  adr  err | buf\_q  ovf | buf\_q  empty | buf\_q  full | read  sm  2 | read  sm  4 | read  sm  3 | read  sm  2 | read  sm  1 | read  sm  0 | clct  sm  2 | clct  sm  1 | clct  sm  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal |  | Description |
| [02:00] | R | clct\_sm[2:0] |  | CLCT Trigger machine state |
| [07:03] | R | read\_sm[4:0] |  | Readout machine state |
| [08] | R | buf\_q\_full |  | All raw hits ram in use, ram writing must stop |
| [09] | R | buf\_q\_empty |  | No fences remain in buffer queue |
| [10] | R | buf\_q\_ovf\_err |  | Tried to push new event when queue full |
| [11] | R | buf\_q\_adr\_err |  | Tried to pop event when queue empty |
| [15:12] | R | -- | 0 | Unassigned |

Adr B0 ADR\_SEQCLCTM Sequencer CLCT (MSBs)

(Split with Adr 78 ADR\_SEQCLCT0 and Adr 7A ADR\_SEQCLCT1)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| sync  err | clock  lock  lost | 0 | 0 | 0 | 0 | active  cfeb  6 | active  cfeb  5 | active  cfeb  4 | active  cfeb  3 | active  cfeb  2 | active  cfeb  1 | active  cfeb  0 | sync  err | clct  bxn  1 | clct  bxn  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typ | Description |
| [01:00] | R | clctc[1:0] bxn\_counter | - | Bunch crossing number at pretrigger, common to clct0/1 |
| [02] | R | clctc[2] sync\_err | 0 | BX0 disagrees with BXN counter, common to clct0/1 |
| [9:3] | R | clctf[6:0] | - | Active feb list latched at TMB alct\*clct matching time |
| [13:10] | R | -- | 0 | Unassigned |
| [14] | R | clock\_lock\_lost FF | 0 | 40MHz main clock lost lock, global\_reset asserted |
| [15] | R | sync\_err (direct) | 0 | Sync error: bxn counter==0 does not match bx0 |

Adr B2 ADR\_TMBTIM TMB Timing for ALCT\*CLCT Coincidence

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | mpctx  delay  3 | mpctx  delay  2 | mpctx  delay  1 | mpctx  delay  0 | clct  wind  3 | clct  wind  2 | clct  wind  1 | clct  wind  0 | alct  delay  3 | alct  delay  2 | alct  delay  1 | alct  delay  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [03:00] | RW | alct\_delay[3:0] | 1 | Delay ALCT for CLCT match window |
| [07:04] | RW | clct\_window[3:0] | 3 | CLCT match window width |
| [11:08] | RW | mpc\_tx\_delay[3:0] | 0 | MPC transmit delay |
| [15:12] | RW | -- | 0 | Unassigned |

Adr B4 ADR\_LHC\_CYCLE LHC Cycle Period, Maximum BXN Count

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | lhc  cycle  11 | lhc  cycle  10 | lhc  cycle  9 | lhc  cycle  8 | lhc  cycle  7 | lhc  cycle  6 | lhc  cycle  5 | lhc  cycle  4 | lhc  cycle  3 | lhc  cycle  2 | lhc  cycle  1 | lhc  cycle  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [11:00] | RW | lhc\_cycle[11:0] | 3564 | Maximum bxn+1  3564(hDEC) for LHC  924(h39C) for beam test |
| [15:12] | RW | -- | 0 | Unassigned |

Adr B6 ADR\_RPC\_CFG RPC Configuration

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | rpc  done | read  bxn  2 | read  bxn  1 | read  bxn  0 | read  bank  1 | read  bank  0 | bxn  offset3 | bxn  offset2 | bxn  offset1 | bxn  offset0 | read  enable | 0 | 0 | rpc1  exists | rpc0  exists |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [01:00] | RW | rpc\_exists[1:0] | 3 | Bit (n) = 1 = RPC(n) Exists |
| [03:02] | RW | -- | 0 | Unused |
| [04] | RW | rpc\_read\_enable | 1 | 1=Include Existing RPCs in DMB Readout |
| [08:05] | RW | rpc\_bxn\_offset[3:0] | 0 | RPC BXN offset |
| [10:09] | RW | rpc\_bank[1:0] | 0 | RPC bank address, for reading rdata sync mode |
| [13:11] | R | rpc\_rbxn[2:0] | - | RPC rdata[18:16] msbs for sync mode, adr 1E |
| [14] | R | rpc\_done | 1 | RPC FPGA reports configuration done |
| [15] | RW | -- | 0 | Unassigned |

Adr B8 ADR\_RPC\_RDATA RPC Raw Hits Sync Mode Read Data

See Adr 1E p33

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| rdata  15 | rdata  14 | rdata  13 | rdata  12 | rdata  11 | rdata  10 | rdata  9 | rdata  8 | rdata  7 | rdata  6 | rdata  5 | rdata  4 | rdata  3 | rdata  2 | rdata  1 | rdata  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [15:00] | R | rpc\_rdata[15:0] | - | RPC RAM read data for sync mode |

Adr BA ADR\_RPC\_RAW\_DELAY RPC Raw Hits Data Delay + RPC BXN Differences

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| rpc1  bxn  diff3 | rpc1  bxn  diff2 | rpc1  bxn  diff1 | rpc1  bxn  diff0 | rpc0  bxn  diff3 | rpc0  bxn  diff2 | rpc0  bxn  diff1 | rpc0  bxn  diff0 | rpc1  delay  3 | rpc1  delay  2 | rpc1  delay  1 | rpc1  delay  0 | rpc0  delay  3 | rpc0  delay  2 | rpc0  delay  1 | rpc0  delay  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [03:00] | RW | rpc0\_delay[3:0] | 1 | RPC0 Raw hits data delay |
| [07:04] | RW | rpc1\_delay[3:0] | 1 | RPC1 Raw hits data delay |
| [11:08] | R | rpc0\_bxn\_diff[3:0]; | - | RPC bxn – Offset (in adr B6) |
| [15:12] | R | rpc1\_bxn\_diff[3:0]; | - | RPC bxn – Offset (in adr B6) |

Adr BC ADR\_RPC\_INJ RPC Injector Control

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | rpc  tbins  test | inj  rdata  18 | inj  rdata  17 | inj  rdata  16 | inj  wdata  18 | inj  wdata  17 | inj  wdata  16 | inj  sel | delay  rat  3 | delay  rat  2 | delay  rat  1 | delay  rat  0 | mask  rpc | mask  rat | mask  all |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [00] | RW | rpc\_mask\_all | 1 | 1=Enable RPC Inputs from RAT, 0=disable all |
| [01] | RW | injector\_mask\_rat | 0 | 1=Enable RAT for injector fire |
| [02] | RW | injector\_mask\_rpc | 1 | 1=Enable RPC injector RAM for injector fire |
| [06:03] | RW | inj\_delay\_rat[3:0] | 0 | CFEB/RPC injectors wait for RAT |
| [07] | RW | rpc\_inj\_sel | 0 | 1=Enable injector RAM write |
| [10:08] | RW | rpc\_inj\_wdata[18:16] | 0 | RPC injector write data MSBs, see adr C0 p58 |
| [13:11] | R | rpc\_inj\_rdata[18:16] | - | RPC injector read data MSBs, see adr C0 p58 |
| [14] | RW | rpc\_tbins\_test | 0 | Set write\_data=address test mode |
| [15] | RW | -- | 0 | Unassigned |

Adr BE ADR\_RPC\_INJ\_ADR RPC Injector RAM Addresses

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| inj  adr  7 | inj  adr  6 | inj  adr  5 | inj  adr  4 | inj  adr  3 | inj  adr  2 | inj  adr  1 | inj  adr  0 | 0 | 0 | inj  ren  1 | inj  ren  0 | 0 | 0 | inj  wen  1 | inj  wen  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [01:00] | RW | rpc\_inj\_wen[1:0] | 0 | 1=Write enable injector RAMn |
| [03:02] | RW | -- | 0 | Unused |
| [05:04] | RW | rpc\_inj\_ren[1:0] | 0 | 1=Read enable Injector RAMn |
| [15:06] | RW | inj\_rwadr[9:0] | 0 | Injector RAM read/write address |

Adr C0 ADR\_RPC\_INJ\_WDATA RPC Injector Write Data

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| inj  wdata  15 | inj  wdata  14 | inj  wdata  13 | inj  wdata  12 | inj  wdata  11 | inj  wdata  10 | inj  wdata  9 | inj  wdata  8 | inj  wdata  7 | inj  wdata  6 | inj  wdata  5 | inj  wdata  4 | inj  wdata  3 | inj  wdata  2 | inj  wdata  1 | inj  wdata  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [15:00] | RW | rpc\_inj\_wdata[15:0] | 0 | RPC RAM write data LSBs (see Adr BC msbs p58) |

Adr C2 ADR\_RPC\_INJ\_RDATA RPC Injector Read Data

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| inj  rdata  15 | inj  rdata  14 | inj  rdata  13 | inj  rdata  12 | inj  rdata  11 | inj  rdata  10 | inj  rdata  9 | inj  rdata  8 | inj  rdata  7 | inj  rdata  6 | inj  rdata  5 | inj  rdata  4 | inj  rdata  3 | inj  rdata  2 | inj  rdata  1 | inj  rdata  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [15:00] | R | rpc\_inj\_rdata[15:0] | - | RPC RAM read data LSBs (see Adr BC msbs p58) |

Adr C4 ADR\_RPC\_TBINS RPC FIFO Time Bins

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | rpc  de  couple | rpc  pre  4 | rpc  pre  3 | rpc  pre  2 | rpc  pre  1 | rpc  pre  0 | rpc  tbins  4 | rpc  tbins  3 | rpc  tbins  2 | rpc  tbins  1 | rpc  tbins  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [04:00] | RW | fifo\_tbins\_rpc[4:0] | 7 | Number RPC FIFO time bins to read out |
| [09:05] | RW | fifo\_pretrig\_rpc[4:0] | 2 | Number RPC FIFO time bins before pretrigger |
| [10] | RW | rpc\_decouple | 0 | 1=Independent rpc tbins, 0=copy cfeb tbins |
| [15:11] | RW | -- | 0 | Unused |

Adr C6 ADR\_RPC0\_HCM RPC0 Hot Channel Mask

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| enable  pad15 | enable  pad14 | enable  pad13 | enable  pad12 | enable  pad11 | enable  pad10 | enable  pad9 | enable  pad8 | enable  pad7 | enable  pad6 | enable  pad5 | enable  pad4 | enable  pad3 | enable  pad2 | enable  pad1 | enable  pad0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [15:00] | RW | rpc0\_hcm[15:0] | FFFF | Bit(n)=1=Enable RPC Pad(n), FFFF=enable all |

Adr C8 ADR\_RPC1\_HCM RPC1 Hot Channel Mask

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [15:00] | RW | rpc1\_hcm[15:0] | FFFF | Bit(n)=1=Enable RPC Pad(n), FFFF=enable all |

Adr CA ADR\_BX0\_DELAY BX0 to MPC Delays

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | bx0  match | bx0  vpf  test | alct  bx0  enable | clct  bx dly  3 | clct  bx dly  2 | clct  bx dly  1 | clct  bx dly  0 | alct  bx dly  3 | alct  bx dly  2 | alct  bx dly  1 | alct  bx dly  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [03:00] | RW | alct\_bx0\_delay[3:0] | 0 | ALCT bx0 delay to mpc transmitter |
| [07:04] | RW | clct\_bx0\_delay[3:0] | 0 | CLCT bx0 delay to mpc transmitter |
| [08] | RW | alct\_bx0\_enable | 1 | 1=Enable using alct bx0, else copy clct bx0 |
| [09] | RW | bx0\_vpf\_test | 0 | Sets clct\_bx0=lct0\_vpf for bx0 alignment tests |
| [10] | R | bx0\_match | 1 | 1=alct\_bx0==clct\_bx0, latched at clct\_bx0 |
| [15:11] | RW | -- | - | Unused |

Adr CC ADR\_NON\_TRIG\_RO Non-Triggering Event Enables + ME1A/B Reversal

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| csc  type  3 | csc  type  2 | csc  type  1 | csc  type  0 | 0 | 0 | reverse  me1b | reverse  me1a | reverse  csc | stagger  csc | csc  me1ab | cnt  non  me1ab | mpc  me1a  block | allow  match  ro | allow  clct  ro | allow  alct  ro |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default  Type A | Description |
| [00] | RW | tmb\_allow\_alct\_ro | 0 | 1=Allow ALCT-only non-triggering readout |
| [01] | RW | tmb\_allow\_clct\_ro | 0 | 1=Allow CLCT-only non-triggering readout |
| [02] | RW | tmb\_allow\_match\_ro | 1 | 1=Allow ALCT\*CLCT non-triggering readout |
| [03] | RW | mpc\_me1a\_block | 1 | Block ME1A LCTs from MPC, still queue for readout |
| [04] | RW | cnt\_non\_me1ab\_en | 1 | Allow clct pretrig counters count non me1ab |
| [05] | R | csc\_me1ab | 0 | 1= CSC is ME1A or ME1B. 0=normal CSC |
| [06] | R | stagger\_hs\_csc | 1 | 1=Staggered CSC, 0=non-staggered |
| [07] | R | reverse\_hs\_csc | 0 | 1=Reversed staggered CSC, non-me1 |
| [08] | R | reverse\_hs\_me1a | 0 | 1=reversed me1a hstrips |
| [09] | R | reverse\_hs\_me1b | 0 | 1=reversed me1b hstrips |
| [11:10] | RW | -- | 0 | Free 2 |
| [15:12] | R | csc\_type[3:0] | A | Firmware compile type  A=Normal CSC  B=Reversed CSC  C=Normal ME1B, Reversed ME1A  D=Reversed ME1B, Normal ME1A |

Firmware Compile Type Codes A,B,C,D:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| CSC\_type | stagger\_hs\_csc | reverse\_hs\_csc | reverse\_hs\_me1a | reverse\_hs\_me1b | csc\_me1ab |
| A | 1 | 0 | 0 | 0 | 0 |
| B | 0 | 1 | 0 | 0 | 0 |
| C | 0 | 0 | 1 | 0 | 1 |
| D | 0 | 0 | 0 | 1 | 1 |

Adr CE ADR\_SCP\_TRIG Scope Trigger Source Channel

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ch6 | ch5 | ch4 | ch3 | ch2 | ch1 | ch0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [06:00] | RW | trigger\_ch[6:0] | 0 | ch0=trigger on sequencer🡪 pretrig |
| [14:07] | RW | -- | 0 | Unassigned |
| [15] | RW | scp\_ch\_overlay | 0 | 0=normal ch assignments, 1=debug assigments |

Adr D0 ADR\_CNT\_CTRL Status Counter Control

(See also Adr D2)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| cnt  select  6 | cnt  select  5 | cnt  select  4 | cnt  select  3 | cnt  select  2 | cnt  select  1 | cnt  select  0 | cnt  adr  lsb | hdr  clr  resync | cnt  clr  resync | en  alct  debug | seq  cnt  ovf | alct  cnt  ovf | stop  on  ovf | snap  shot | clear  all |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [00] | RW | cnt\_all\_clear | - | Clear VME counters (also clr on ccb\_evcntres) |
| [01] | RW | cnt\_snapshot | - | Take snapshot of current counter state |
| [02] | RW | cnt\_stop\_on\_ovf | 0 | Stop all counters if any overflows |
| [03] | R | cnt\_any\_ovf\_alct | - | At least 1 alct counter overflowed |
| [04] | R | cnt\_any\_ovf\_seq | - | At least 1 sequencer counter overflowed |
| [05] | RW | cnt\_alct\_debug | 1 | 1=enable alct\_lct\_err counter |
| [06] | RW | cnt\_clear\_on\_resync | 0 | 1=Clear VME counters on ttc\_resync |
| [07] | RW | hdr\_clear\_on\_resync | 1 | 1=Clear header counters on ttc\_resync |
| [08] | RW | cnt\_adr\_lsb | - | Counter half select, 0=bits[15:0], 1=bits[29:16] |
| [15:09] | RW | cnt\_select[6:0] | - | Counter select address |

Counter Select Addresses (even cnt\_ad\_lsb=LSBs, odd cnt\_adr\_lsb=MSBs):

| Address10 | Counter Description | Bits | VME Clears |
| --- | --- | --- | --- |
| 00 | ALCT: alct0 vpf received | 30 | Y |
| 01 | ALCT: alct1 vpf received | 30 | Y |
| 02 | ALCT: alct data structure error | 30 | Y |
| 03 | ALCT: trigger path ECC 1-bit error corrected | 30 | Y |
| 04 | ALCT: trigger path ECC 2-bit error not corrected | 30 | Y |
| 05 | ALCT: trigger path ECC >2-bit error not corrected | 30 | Y |
| 06 | ALCT: trigger path ECC ≥2-bit error not corrected, ALCT data blanked | 30 | Y |
|  |  |  |  |
| 07 | ALCT: alct replied ECC 1-bit error corrected | 30 | Y |
| 08 | ALCT: alct replied ECC 2-bit error not corrected | 30 | Y |
| 09 | ALCT: alct replied ECC >2-bit error not corrected | 30 | Y |
| 10 | ALCT: raw hits readout | 30 | Y |
| 11 | ALCT: raw hits readout CRC error | 30 | Y |
| 12 |  | 30 | Y |
|  |  |  |  |
| 13 | CLCT: Pre-trigger was on any CFEB | 30 | Y |
| 14 | CLCT: Pre-trigger includes a CLCT on CFEB0 | 30 | Y |
| 15 | CLCT: Pre-trigger includes a CLCT on CFEB1 | 30 | Y |
| 16 | CLCT: Pre-trigger includes a CLCT on CFEB2 | 30 | Y |
| 17 | CLCT: Pre-trigger includes a CLCT on CFEB3 | 30 | Y |
| 18 | CLCT: Pre-trigger includes a CLCT on CFEB4 | 30 | Y |
| 19 | CLCT: Pre-trigger includes a CLCT on CFEB5 | 30 | Y |
| 20 | CLCT: Pre-trigger includes a CLCT on CFEB6 | 30 | Y |
|  |  |  |  |
| 21 | CLCT: Pre-trigger was on ME1A cfeb4 only | 30 | Y |
| 22 | CLCT: Pre-trigger was on ME1B cfebs0-3 only | 30 | Y |
| 23 | CLCT: Pretrig discarded, no wrbuf available, buffer stalled | 30 | Y |
| 24 | CLCT: Pretrig discarded, no alct in window | 30 |  |
| 25 | CLCT: CLCT discarded, clct0 had invalid pattern after drift | 30 | Y |
| 26 | CLCT: CLCT0 passed hit thresh but failed pid thresh after drift | 30 | Y |
| 27 | CLCT: CLCT1 passed hit thresh but failed pid thresh after drift | 30 | Y |
| 28 | CLCT: Bx pre-trigger machine waited for triads to dissipate before rearm | 30 | Y |
|  |  |  |  |
| 29 | CLCT: clct0 sent to TMB matching section | 30 | Y |
| 30 | CLCT: clct1 sent to TMB matching section | 30 | Y |
|  |  |  |  |
| 31 | TMB: TMB matching accepted a match, alct-only, or clct-only event | 30 | Y |
| 32 | TMB: CLCT\*ALCT matched trigger | 30 | Y |
| 33 | TMB: ALCT-only trigger | 30 | Y |
| 34 | TMB: CLCT-only trigger | 30 | Y |
|  |  |  |  |
| 35 | TMB: TMB matching rejected event | 30 | Y |
| 36 | TMB: TMB matching rejected event, but queued for non-trigger readout | 30 | Y |
| 37 | TMB: TMB matching discarded an ALCT pair | 30 | Y |
| 38 | TMB: TMB matching discarded a CLCT pair | 30 | Y |
| 39 | TMB: TMB matching discarded CLCT0 from ME1A | 30 | Y |
| 40 | TMB: TMB matching discarded CLCT1 from ME1A | 30 | Y |
|  |  |  |  |
| 41 | TMB: Matching found no ALCT | 30 | Y |
| 42 | TMB: Matching found no CLCT | 30 | Y |
| 43 | TMB: Matching found One ALCT | 30 | Y |
| 44 | TMB: Matching found One CLCT | 30 | Y |
| 45 | TMB: Matching found Two ALCTs | 30 | Y |
| 46 | TMB: Matching found Two CLCTs | 30 | Y |
|  |  |  |  |
| 47 | TMB: ALCT0 copied into ALCT1 to make 2nd LCT | 30 | Y |
| 48 | TMB: CLCT0 copied into CLCT1 to make 2nd LCT | 30 | Y |
| 49 | TMB: LCT1 has higher quality than LCT0, error | 30 | Y |
|  |  |  |  |
| 50 | TMB: Transmitted LCT0 to MPC | 30 | Y |
| 51 | TMB: Transmitted LCT1 to MPC | 30 | Y |
|  |  |  |  |
| 52 | TMB: MPC accepted LCT0 | 30 | Y |
| 53 | TMB: MPC accepted LCT1 | 30 | Y |
| 54 | TMB: MPC rejected both LCT0 & LCT1 | 30 | Y |
|  |  |  |  |
| 55 | L1A: L1A received | 30 | Y |
| 56 | L1A: L1A received, TMB in L1A window | 30 | Y |
| 57 | L1A: L1A received, no TMB in window | 30 | Y |
| 58 | L1A: TMB triggered, no L1A in window | 30 | Y |
| 59 | L1A: TMB readouts completed | 30 | Y |
| 60 | L1A: TMB readouts lost by 1-event-per-L1A limit | 30 | Y |
|  |  |  |  |
| 61 | STAT: CLCT Triads skipped | 30 | Y |
| 62 | STAT: Raw hits buffer had to be reset due to ovf, error | 30 | Y |
| 63 | STAT: TTC Resyncs received | 30 | Y |
| 64 | STAT: Sync error, bxn!=offset at bx0 arrival or no bx0 at bxn==offset | 30 | Y |
| 65 | STAT: Parity error in CFEB or RPC raw hits RAM, possible SEU | 30 | Y |
| Event counters that follow are in the TMB header:  They are cleared via TTC commands, such as event counter reset, and are not via direct VME command to Adr D0. | | | |
| 66 | HDR: Pre-trigger counter | 30 | N |
| 67 | HDR: CLCT counter | 30 | N |
| 68 | HDR: TMB trigger counter | 30 | N |
| 69 | HDR: ALCTs received counter | 30 | N |
| 70 | HDR: L1As received from ccb counter, 12 bits | 12 | N |
| 71 | HDR: Readout counter, 12 bits | 12 | N |
| 72 | HDR: Orbit counter | 30 | N |
|  |  |  |  |
| 73 | ALCT: Structure error, Expected alct0[10:1]=0 when alct0\_vpf=0 | 8 | Y |
| 74 | ALCT: Structure error, Expected alct1[10:1]=0 when alct1\_vpf=0 | 8 | Y |
| 75 | ALCT: Structure error, Expected alct0\_vpf=1 when alct1\_vpf=1 | 8 | Y |
| 76 | ALCT: Structure error, Expected alct0[10:1]>0 when alct0\_vpf=1 | 8 | Y |
| 77 | ALCT: Structure error, Expected alct1[10:1]>0 when alct1\_vpf=1 | 8 | Y |
| 78 | ALCT: Structure error, Expected alct1!=alct0 when alct0\_vpf=1 | 8 | Y |
|  |  |  |  |
| 79 | CCB: TTCrx lock lost | 8 | Y |
| 80 | CCB: qPLL lock lost | 8 | Y |
|  |  |  |  |
| 81 | GTX: Optical receiver error gtx\_rx\_err\_count0 | 16 | N |
| 82 | GTX: Optical receiver error gtx\_rx\_err\_count1 | 16 | N |
| 83 | GTX: Optical receiver error gtx\_rx\_err\_count2 | 16 | N |
| 84 | GTX: Optical receiver error gtx\_rx\_err\_count3 | 16 | N |
| 85 | GTX: Optical receiver error gtx\_rx\_err\_count4 | 16 | N |
| 86 | GTX: Optical receiver error gtx\_rx\_err\_count5 | 16 | N |
| 87 | GTX: Optical receiver error gtx\_rx\_err\_count6 | 16 | N |

Adr D2 ADR\_CNT\_RDATA Status Counter Data [See Adr D0 p61]

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| rdata  15 | rdata  14 | rdata  13 | rdata  12 | rdata  11 | rdata  10 | rdata  9 | rdata  8 | rdata  7 | rdata  6 | rdata  5 | rdata  4 | rdata  3 | rdata  2 | rdata  1 | rdata  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [15:00] | R | cnt\_rdata[15:0] | - | Data for selected counter (see adr D0 p61) |

Adr D4 ADR\_JTAGSM0 JTAG State Machine Control (reads JTAG PROM)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| throt  3 | throt  2 | throt  1 | throt  0 | dis | jsm  jtag  oe | jsm  ok | vme  ready | jsm tck  ok | jsm  wdcnt  ok | jsm  cksum  ok | jsm  abort | jsm  busy | jsmsel/  vsm  jtag  auto | jsm  reset | jsm  start |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [00] | RW | jsm\_start | 0 | Manual cycle start command |
| [01] | RW | jsm\_sreset | 0 | Status signal reset |
| [02] | RW | jsm\_sel | 0 | 1=select new JTAG format, 0=select old format |
| [03] | R | jsm\_busy | 0 | State machine busy writing |
| [04] | R | jsm\_aborted | 0 | State machine aborted reading PROM |
| [05] | R | jsm\_cksum\_ok | 1 | Check-sum matches PROM contents |
| [06] | R | jsm\_wdcnt\_ok | 1 | Word count matches PROM contents |
| [07] | R | jsm\_tck\_fpga\_ok | 1 | FPGA jtag tck detected |
| [08] | R | vme\_ready | 1 | TMB VME registers done loading from PROM |
| [09] | R | jsm\_ok | 1 | JTAG state machine completed without errors |
| [10] | R | jsm\_jtag\_oe | 0 | Enable jtag drivers else tri-state |
| [11] | RW | wr\_usr\_jtag\_dis | 0 | 1=disable write access to ADR\_USR\_JTAG adr10 |
| [15:12] | RW | jsm\_throttle[3:0] | 0 | JTAGspeed, 0=fastest,20MHz read,10MHz TCK |

Adr D6 ADR\_JTAGSM1 JTAG State Machine Word Count

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| wdcnt  15 | wdcnt  14 | wdcnt  13 | wdcnt  12 | wdcnt  11 | wdcnt  10 | wdcnt  9 | wdcnt  98 | wdcnt  7 | wdcnt  6 | wdcnt  5 | wdcnt  4 | wdcnt  3 | wdcnt  2 | wdcnt  1 | wdcnt  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [15:00] | R | jsm\_wdcnt[15:0]; | - | JTAG PROM word-count bits [15:0] |

Adr D8 ADR\_JTAGSM2 JTAG State Machine Checksum

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| chain  ok | header  ok | end  ok | tck  cnt  OK | tck  cnt  3 | tck  cnt  2 | tck  cnt  1 | tck  cnt  0 | cksum  7 | cksum  6 | cksum  5 | cksum  4 | cksum  3 | cksum  2 | cksum  1 | cksum  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [07:00] | R | jsm\_cksum[7:0]; | - | jtag state machine checksum |
| [11:08] | R | tck\_fpga\_cnt[3:0] | - | fpga jtag chain tck counter |
| [12] | R | jsm\_tckcnt\_ok | 1 | Total TCKs sent maches PROM trailer tck\_cnt |
| [13] | R | jsm\_end\_ok | 1 | jtag PROM end marker detected |
| [14] | R | jsm\_header\_ok | 1 | jtag PROM header marker detected |
| [15] | R | jsm\_chain\_ok | 1 | jtag PROM chain marker detected |

Adr DA ADR\_VMESM0 VME State Machine Control (reads VME PROM)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| throt  3 | throt  2 | throt  1 | throt  0 | vsm  phaser  auto | vsm  path  ok | vsm  ok | vme  ready | vsm jtag  auto | vsm  wdcnt  ok | vsm  cksum  ok | vsm  abort | vsm  busy | vsm  auto  start | vsm  sreset | vsm  start |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [00] | RW | vsm\_start | 0 | Manual cycle start command |
| [01] | RW | vsm\_sreset | 0 | Status signal reset |
| [02] | R | vsm\_autostart | 1 | Auto-start after hard-reset |
| [03] | R | vsm\_busy | 0 | State machine busy writing |
| [04] | R | vsm\_aborted | 0 | State machine aborted reading PROM |
| [05] | R | vsm\_cksum\_ok | 1 | Check-sum matches PROM contents |
| [06] | R | vsm\_wdcnt\_ok | 1 | Word count matches PROM contents |
| [07] | RW\* | vsm\_jtag\_auto | 1 | JTAG SM autostart after vmesm completes |
| [08] | R | vme\_ready | 1 | TMB VME registers done loading from PROM |
| [09] | R | vsm\_ok | 1 | State machine completed without errors |
| [10] | R | vsm\_path\_ok | 1 | State machine wrote 55AAh to ADR\_VMESM4 |
| [11] | RW | vsm\_phaser\_auto | 1 | Digital phase shifter autostart after vmesm done |
| [15:12] | RW | vsm\_throttle[3:0] | 0 | VME PROM-read speed control, 0=fastest |

\* vsm\_jtag\_auto should be set to 0 to enable U76 testing, otherwise jtagsm will run, and erase U76 data.

Adr DC ADR\_VMESM1 VME State Machine Word Count

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| wdcnt  15 | wdcnt  14 | wdcnt  13 | wdcnt  12 | wdcnt  11 | wdcnt  10 | wdcnt  9 | wdcnt  98 | wdcnt  7 | wdcnt  6 | wdcnt  5 | wdcnt  4 | wdcnt  3 | wdcnt  2 | wdcnt  1 | wdcnt  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [15:00] | R | vsm\_wdcnt[15:0]; | - | VME PROM word-count bits [15:0] |

Adr DE ADR\_VMESM2 VME State Machine Checksum

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | jtag  vec  1 | jtag  vec  0 | fmt err  4 | fmt err  3 | fmt err  2 | fmt err  1 | fmt  err  0 | cksum  7 | cksum  6 | cksum  5 | cksum  4 | cksum  3 | cksum  2 | cksum  1 | cksum  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [07:00] | R | vsm\_cksum[7:0]; | - | VME state machine checksum |
| [08] | R | vsm\_fmt\_err[0] | 0 | Missing BC header-begin marker |
| [09] | R | vsm\_fmt\_err[1] | 0 | Missing EC header-end marker |
| [10] | R | vsm\_fmt\_err[2] | 0 | Missing FC data-end marker |
| [11] | R | vsm\_fmt\_err[3] | 0 | Missing FF prom-end marker |
| [12] | R | vsm\_fmt\_err[4] | 0 | Word counter overflow |
| [14:13] | R | jtag\_sm\_vec[1:0] | 0 | JSM JTAG signal State Machine vector |
| [15] | R | -- | - | unassigned |

Adr E0 ADR\_VMESM3 Number of VME Addresses Written by VMESM

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | format  sm  2 | format  sm  1 | format  sm  0 | prom  sm  3 | prom  sm  2 | prom  sm  1 | prom  sm  0 | nvme  writes  7 | nvme  writes  6 | nvme  writes  5 | nvme  writes  4 | nvme  writes  3 | nvme  writes  2 | nvme  writes  1 | nvme  writes  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [07:00] | R | vsm\_nvme\_writes[7:0] | - | Number of vme addresses written |
| [11:8] | R | jsm\_prom\_sm\_vec[3:0] | - | JSM PROM State Machine state vector |
| [14:12] | R | jsm\_format\_sm\_vec[2:0] | - | JSM Data Format Machine state vector |
| [15] | R | -- | 0 | unassigned |

Adr E2 ADR\_VMESM4 VME State Machine Write-Data Check

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| data  15 | data  14 | data  13 | data  12 | data  11 | data  10 | data  9 | data  8 | data  7 | data  6 | data  5 | data  4 | data  3 | data  2 | data  1 | data  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [15:00] | R | vmesm4\_rd[15:0] | 55AAh | vsm\_path\_ok=1 if vsm writes 55aa to this adr |

Adr E4 ADR\_DDDSM RAT 3D3444 State Machine Control

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| verify  dly1 | verify  dly0 | rx  phase | link  tmb | oe  3 | oe  2 | oe  1 | oe  o | verify  ok | sm  busy | auto  start | serial  from | serial  to | adr  latch | dddr  clock | dddr  start |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [00] | RW | dddr\_start\_vme | 0 | Start DDDR State Machine |
| [01] | RW | dddr\_clock | 0 | DDDR manual-mode clock |
| [02] | RW | dddr\_adr\_latch | 1 | DDDR manual-mode address latch, active low |
| [03] | RW | dddr\_serial\_in | 0 | Serial data to DDDR chip |
| [04] | R | dddr\_serial\_out | 0 | Serial data from DDDR chip |
| [05] | RW | dddr\_auto\_start | 1 | DDDR State Machine autostart state |
| [06] | R | dddr\_busy | 0 | DDDR State Machine busy |
| [07] | R | dddr\_verify\_ok | 1 | DDDR data read back verified OK |
| [11:08] | RW | dddr\_oe[3:0] | 00112 | 3D3444 output enables, 1=enable |
| [12] | RW | dddr\_linktmb | 1 | 1=start RAT machine when starting TMB machine |
| [13] | RW | dddr\_rxphase | 1 | 1=use negative clock edge to latch verify data, 0=posedge |
| [15:14] | RW | dddr\_verify\_dly[1:0] | 3 | Delay before latching verify data |

Adr E6 ADR\_DDDR0 RAT 3D3444 RPC Delays, 1 step = 2ns

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [03:00] | RW | delay\_ch0[3:0] | 3 | RPC0 rx clock |
| [07:04] | RW | delay\_ch1[3:0] | 3 | RPC1 rx clock |
| [11:08] | RW | delay\_ch2[3:0] | 0 | RAT2 rx clock, not used |
| [15:12] | RW | delay\_ch3[3:0] | 0 | RAT2 rx clock, not used |

Adr E8 ADR\_UPTIME Uptime Counter

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | up  time  14 | up  time  13 | up  time  12 | up  time  11 | up  time  10 | up  time  9 | up  time  8 | up  time  7 | up  time  6 | up  time  5 | up  time  4 | up  time  3 | up  time  2 | up  time  1 | up  time  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [04:00] | R | uptime[14:0] | - | Seconds since last hard-reset |
| [15] | R | -- | 0 | unassigned |

Adr EA ADR\_BDSTATUS Board Status Summary (copy of raw-hits header)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| status  15 | status  14 | status  13 | status  12 | status  11 | status  10 | status  9 | status  8 | status  7 | status  6 | status  5 | status  4 | status  3 | status  2 | status  1 | status  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [00] | R | bdstatus\_ok | 1 | Voltages OK, temperature OK, prom-load OK |
| [01] | R | vstat\_5p0V | 1 | Voltage Comparator +5.0V, 1=OK |
| [02] | R | vstat\_3p3v | 1 | Voltage Comparator +3.3V, 1=OK |
| [03] | R | vstat\_1p8v | 1 | Voltage Comparator +1.8V, 1=OK |
| [04] | R | vstat\_1p5v | 1 | Voltage Comparator +1.5V, 1=OK |
| [05] | R | /t\_crit | 1 | Temperature ADC Tcritical, 1=OK |
| [06] | R | vsm\_ok | 1 | VME Machine ran without errors |
| [07] | R | vsm\_aborted | 0 | VME State machine aborted reading PROM |
| [08] | R | vsm\_cksum\_ok | 1 | VME Check-sum matches PROM contents |
| [09] | R | vsm\_wdcnt\_ok | 1 | VME Word count matches PROM contents |
| [10] | R | jsm\_ok | 1 | JTAG State machine completed without errors |
| [11] | R | jsm\_aborted | 0 | JTAG State machine aborted reading PROM |
| [12] | R | jsm\_cksum\_ok | 1 | JTAG Check-sum matches PROM contents |
| [13] | R | jsm\_wdcnt\_ok | 1 | JTAG Word count matches PROM contents |
| [14] | R | jsm\_tck\_fpga\_ok | 1 | JTAG tck loopback detected on chain adr C |
| [15] | R | jsm\_tckcnt\_ok | 1 | JTAG state machine TCK count matches PROM |

Adr EC ADR\_BXN\_CLCT CLCT BXN At CLCT-Pretrigger

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | clct  bxn  11 | clct  bxn  10 | clct  bxn  9 | clct  bxn  8 | clct  bxn  7 | clct  bxn  6 | clct  bxn  5 | clct  bxn  4 | clct  bxn  3 | clct  bxn  2 | clct  bxn  1 | clct  bxn  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [11:00] | R | bxn\_clct\_vme[11:0] | - | CLCT BXN latched at last CLCT pretrigger |
| [15:12] | R | -- | 0 | unassigned |

Adr EE ADR\_BXN\_ALCT ALCT BXN At ALCT-Valid-Pattern-Flag

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | alct  bxn  4 | alct  bxn  3 | alct  bxn  2 | alct  bxn  1 | alct  bxn  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [4:00] | R | bxn\_alct\_vme[4:0] | - | ALCT BXN latched at last ALCT vpf |
| [15:5] | R | -- | 0 | unassigned |

Adr F0 ADR\_LAYER\_TRIG Layer-Trigger Mode

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| clct  throt  7 | clct  throt  6 | clct  throt  5 | clct  throt  4 | clct  throt  3 | clct  throt  2 | clct  throt  1 | clct  throt  0 | 0 | nlayrs  hit  2 | nlayrs  hit  1 | nlayrs  hit  0 | layer  thresh  2 | layer  thresh  1 | layer  thresh  0 | layer  trig  en |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [00] | RW | layer\_trigger\_en | 0 | 1=Enable layer trigger mode(see adr 68 p43) |
| [03:01] | RW | lyr\_thresh\_pretrig[2:0] | 4 | layer-trigger threshold |
| [06:04] | R | nlayers\_hit\_vme[2:0] | -- | number layers hit on last layer-trigger |
| [07] | RW | -- | -- | Unassigned |
| [15:08] | RW | clct\_throttle[7:0] | 0 | CLCT Pre-trigger rate throttle |

Adr F2 ADR\_ISE\_VERSION ISE Version

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ver  7 | ver  6 | ver  5 | ver  4 | ver  3 | ver  2 | ver  1 | ver  0 | minor  3 | minor  2 | minor  1 | minor  0 | spack  3 | spack  2 | spack  1 | spack  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [03:00] | R | ise\_version[3:0] | 03h | ISE Service Pack |
| [07:04] | R | ise\_version[7:4] | 01h | ISE Minor Version |
| [15:08] | R | ise\_version[15:8] | 10h | ISE Major Version |

Adr F4 ADR\_TEMP0 Pattern Finder Pre-Trigger

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| adj  cfeb  dist  5 | adj  cfeb  dist  4 | adj  cfeb  dist  3 | adj  cfeb  dist  2 | adj  cfeb  dist  1 | adj  cfeb  dist  0 | pid  thresh  post  3 | pid  thresh  post  2 | pid  thresh  post  1 | pid  thresh  post  0 | pid  thresh  pretrig  3 | pid  thresh  pretrig  2 | pid  thresh  pretrig  1 | pid  thresh  pretrig  0 | 0 | clct  blank |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [00] | RW | clct\_blanking | 1 | 1=blank non-vpf clct output  [requires alct-only or l1a-notmb mode enabled to change this to 0] |
| [01] | RW | -- | 0 | Unassigned |
| [05:02] | RW | pid\_thresh\_pretrig[3:0] | 0 | Minimum pattern ID 0x0-0xA for pre-trigger |
| [09:06] | RW | pid\_thresh\_postdrift[3:0] | 0 | Minimum pattern ID 0x0-0xA after drift delay |
| [15:10] | RW | adjcfeb\_dist[5:0] | 5 | Distance from key on CFEBn to CFEBn+1  to set active feb flag on CFEBn+1 for DMB  Setting to 5 enables hs0,1,2,3,4 and hs31,30,29,29,28,27. |

Adr F6 ADR\_TEMP1 CLCT Separation

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| clct  sep  7 | clct  sep  6 | clct  sep  5 | clct  sep  4 | clct  sep  3 | clct  sep  2 | clct  sep  1 | clct  sep  0 | 0 | clct  sep  ram  sel\_ab | clct  sep  ram  adr  3 | clct  sep  ram  adr  2 | clct  sep  ram  adr  1 | clct  sep  ram  adr  0 | clct  sep ram  we | clct  sep  src |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [00] | RW | clct\_sep\_src | 1 | CLCT separation source 1=vme, 0=ram |
| [01] | RW | clct\_sep\_ram\_we | 0 | 1=enable CLCT separation ram for writing |
| [05:02] | RW | clct\_sep\_ram\_adr[3:0] | 0 | CLCT separation RAM rw address 0-F |
| [06] | RW | clct\_sep\_ram\_sel\_ab | 0 | 1=read me1a RAM, 0=me1b RAM or std RAM |
| [07] | RW | -- | -- | Unassigned |
| [15:08] | RW | clct\_sep\_vme[7:0] | 10 | Minimum CLCT separation in key ½-strips |

Adr F8 ADR\_TEMP2 CLCT Separation RAM Data

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| pspan  7 | pspan  6 | pspan  5 | pspan  4 | pspan  3 | pspan  2 | pspan  1 | pspan  0 | nspan  7 | nspan  6 | nspan  5 | nspan  4 | nspan  3 | nspan  2 | nspan  1 | nspan  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [07:00] | RW/R | clct\_sep\_ram\_wr[7:0] | 10 | nspan CLCT separation RAM data,  blanks keys from 1st key to keys>=key-nspan |
| [15:08] | RW/R | clct\_sep\_ram\_wr[15:8] | 10 | pspan CLCT separation RAM data,  blanks keys from 1st key to keys<=key+pspan |

Adr FA ADR\_PARITY SEU Parity Errors

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| perr  mux  5 | perr  mux  4 | perr  mux  3 | perr  mux  2 | perr  mux  1 | perr  mux  0 | 0 | 0 | perr  reset | perr  ff | perr | perr  en | perr  adr  3 | perr  adr  2 | perr  adr  1 | perr  adr  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [03:00] | RW | perr\_adr[3:0] | 0 | Parity data bank select address |
| [4] | R | perr\_en | 1 | Parity error latch enabled |
| [5] | R | perr | 0 | Parity error summary |
| [6] | R | perr\_ff | 0 | Parity error summary, latched |
| [7] | RW | perr\_reset | 0 | Parity error reset |
| [9:8] | RW | -- | 0 | Unassigned |
| [15;10] | R | parity\_rd\_mux[5:0] | 0 | Parity data multiplexer, selected by perr\_adr[] |

adr 0: parity\_rd\_mux <= perr\_ram\_ff[ 5: 0]; // R cfeb0 rams

adr 1: parity\_rd\_mux <= perr\_ram\_ff[11: 6]; // R cfeb1 rams

adr 2: parity\_rd\_mux <= perr\_ram\_ff[17:12]; // R cfeb2 rams

adr 3: parity\_rd\_mux <= perr\_ram\_ff[23:18]; // R cfeb3 rams

adr 4: parity\_rd\_mux <= perr\_ram\_ff[29:24]; // R cfeb4 rams

adr 5: parity\_rd\_mux <= perr\_ram\_ff[35:30]; // R cfeb5 rams

adr 6: parity\_rd\_mux <= perr\_ram\_ff[41:36]; // R cfeb6 rams

adr 7: parity\_rd\_mux <= {1’b0,perr\_ram\_ff[46:42]}; // R rpc rams

adr 8: parity\_rd\_mux <= {4’h0,perr\_ram\_ff[48:47]}; // R mini rams

adr 9: parity\_rd\_mux <= {1’b0,perr\_cfeb[6:0]}; // R cfeb parity errors

adr 10: parity\_rd\_mux <= {1’b0,perr\_cfeb\_ff[6:0]}; // R cfeb parity errors,latched

adr 11: parity\_rd\_mux <= {4’h0,perr\_rpc\_ff,perr\_rpc}; // R rpc parity errors,latched

adr12: parity\_rd\_mux <= {4’h0,perr\_mini\_ff, perr\_mini}; // R mini parity errors,latched

Adr FC ADR\_CCB\_STAT1 CCB Status Register Continued from Adr 2E

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [00] | R | ccb\_ttcrx\_lock\_never | 0 | TTCrx lock never achieved |
| [01] | R | ccb\_ttcrx\_lost\_ever | 0 | TTCrx lock was lost at least once |
| [02] | R | ccb\_qpll\_lock\_never | 0 | QPLL lock never achieved |
| [03] | R | ccb\_qpll\_lost\_ever | 0 | QPLL lock was lost at least once |
| [15:04] | R | -- | 0 | Unassigned |

Adr FE ADR\_BXN\_L1A CLCT BXN at L1A Arrival

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | l1a  bxn  11 | l1a  bxn  10 | l1a  bxn  9 | l1a  bxn  8 | l1a  bxn  7 | l1a  bxn  6 | l1a  bxn  5 | l1a  bxn  4 | l1a  bxn  3 | l1a  bxn  2 | l1a  bxn  1 | l1a  bxn  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [11:00] | R | bxn\_l1a\_vme[11:0] | - | CLCT BXN latched at last L1A arrival |
| [15:12] | R | -- | 0 | unassigned |

Adr 100 ADR\_L1A\_LOOKBACK L1A Lookback Distance

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| l1a  win  pri  en | inj  rdata  17 | inj  rdata  16 | inj  wdata  17 | inj  wdata  16 | l1a  look back  10 | l1a  look back  9 | l1a  look back  8 | l1a  look back  7 | l1a  look back  6 | l1a  look back  5 | l1a  look back  4 | l1a  look back  3 | l1a  look back  2 | l1a  look back  1 | l1a  look  back  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [10:00] | RW | l1a\_lookback[10:0] | 128 | bx to look back from L1As wr\_buf\_adr  for L1A-only readouts |
| [12:11] | RW | inj\_wdata[17:16] | 0 | Injector RAM write data MSBs |
| [14:13] | R | inj\_rdata[17:16] | 0 | Injector RAM read data MSBs |
| [15] | RW | l1a\_win\_pri\_en | 1 | 1=Limit TMB to 1 event readout per L1A |

Adr 102 ADR\_SEQ\_DEBUG Sequencer Debug Signals

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | l1a  bxn  11 | l1a  bxn  10 | l1a  bxn  9 | l1a  bxn  8 | l1a  bxn  7 | l1a  bxn  6 | l1a  bxn  5 | l1a  bxn  4 | l1a  bxn  3 | l1a  bxn  2 | l1a  bxn  1 | l1a  bxn  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [03:00] | RW | seqdeb\_adr[3:0] | - | Sequencer signal address 0-15 |
| [15:04] | R | seqdeb\_rd\_mux[11:0] | - | Multiplexed sequencer data for debugging |

adr 0: deb\_wr\_buf\_adr[10:0] Buffer write address at last pretrig

adr 1: deb\_buf\_push\_adr[10:0] Queue push address at last push

adr 2: deb\_buf\_pop\_adr[10:0] Queue pop address at last pop

adr 3: deb\_buf\_push\_data[11:0] Queue push data at last push

adr 4: deb\_buf\_push\_data[23:12] +Queue push data at last push

adr 5: deb\_buf\_push\_data[31:24] +Queue push data at last push

adr 6: deb\_buf\_pop\_data[11:0] Queue pop data at last pop

adr 7: deb\_buf\_pop\_data[23:12] +Queue pop data at last pop

adr 8: deb\_buf\_pop\_data[31:24] +Queue pop data at last pop

Adr 104 ADR\_ALCT\_SYNC\_CTRL ALCT Sync Mode Control

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| sync  pre  3 | sync  pre  2 | sync  pre  1 | sync  pre  0 | 0 | 0 | sync  2nd  err ff | sync  1st  err ff | sync  2nd  err | sync  1st  err | sync  clr | sync  rand | sync  dly  3 | sync  dly  2 | sync  dly  1 | sync  dly  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [03:00] | RW | alct\_sync\_rxdata\_dly [3:0] | 0 | Sync mode delay pointer to valid data |
| [04] | RW | alct\_sync\_tx\_random | 0 | Sync mode tmb transmits random data to alct |
| [05] | RW | alct\_sync\_clr\_err | 0 | ALCT sync mode clear rng error FFs |
| [06] | R | alct\_sync\_1st\_err | 0 | 1st-in-time match ok, alct-to-tmb |
| [07] | R | alct\_sync\_2nd\_err | 0 | 2nd-in-time match ok, alct-to-tmb |
| [08] | R | alct\_sync\_1st\_err\_ff | 0 | 1st-in-time match ok, alct-to-tmb, latched |
| [09] | R | alct\_sync\_2nd\_err\_ff | 0 | 2nd-in-time match ok, alct-to-tmb, latched |
| [11:10] | RW | -- | 0 | Unassigned |
| [15:12] | RW | alct\_sync\_rxdata\_pre[3:0] | 9 | Sync mode pre-delay pointer to valid data |

Adr 106 ADR\_ALCT\_SYNC\_TXDATA\_1ST ALCT Sync Mode Transmit Data 1st

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | sync  1st  9 | sync  1st  8 | sync  1st  7 | sync  1st  6 | sync  1st  5 | sync  1st  4 | sync  1st  3 | sync  1st  2 | sync  1st  1 | sync  1st  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [09:00] | RW | alct\_sync\_txdata\_1st[9:0] | - | Sync mode data to send for loopback 1st in time |
| [15:10] | RW | -- | 0 | Unassigned |

Adr 108 ADR\_ALCT\_SYNC\_TXDATA\_2ND ALCT Sync Mode Transmit Data 2nd

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | sync  2nd  9 | sync  2nd  8 | sync  2nd  7 | sync  2nd  6 | sync  2nd  5 | sync  2nd  4 | sync  2nd  3 | sync  2nd  2 | sync  2nd  1 | sync  2nd  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [09:00] | RW | alct\_sync\_txdata\_1st[9:0] | - | Sync mode data to send for loopback 1st in time |
| [15:10] | RW | -- | 0 | Unassigned |

Adr 10A ADR\_SEQ\_OFFSET1 Sequencer Counter Offsets Continued [from Adr076]

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | bxn  offset  11 | bxn  offset  10 | bxn  offset  9 | bxn  offset  8 | bxn  offset  7 | bxn  offset  6 | bxn  offset  5 | bxn  offset  4 | bxn  offset  3 | bxn  offset  2 | bxn  offset  1 | bxn  offset  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [11:00] | RW | bxn\_offset\_l1a[11:0] | - | L1A bxn offset preset value |
| [15:12] | RW | -- | 0 | Unassigned |

Adr 10C ADR\_MINISCOPE Internal 16 Channel Digital Miniscope

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | tbins  pretrig  4 | tbins  pretrig  3 | tbins  pretrig  2 | tbins  pretrig  1 | tbins  pretrig  0 | tbins  4 | tbins  3 | tbins  2 | tbins  1 | tbins  0 | tbins  word  nsert | tbins  test  mode | read  enable |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [00] | RW | mini\_read\_enable | 1 | Enable Miniscope readout to DMB |
| [01] | RW | mini\_tbins\_test | 0 | Miniscope data=write\_address, for testing |
| [02] | RW | mini\_tbins\_word | 1 | Insert tbins and pretrig tbins in 1st word |
| [07:03] | RW | fifo\_tbins\_mini[4:0] | 22 | Number Mini FIFO time bins to read out,  must multiple of 2 but not of 4 |
| [12:08] | RW | fifo\_pretrig\_mini[4:0] | 4 | Number Mini FIFO time bins before pre-trigger |
| [15:13] | RW | -- | 0 | Unassigned |

Adr 10E ADR\_PHASER0 ALCT rxd Digital Phase Shifter

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| alct  rxd  delay  7 | alct  rxd  delay  6 | alct  rxd  delay  5 | alct  rxd  delay  4 | alct  rxd  delay  3 | alct  rxd  delay  2 | alct  rxd  delay  1 | alct  rxd  delay  0 | pos  neg | sm  2 | sm  1 | sm  0 | lock | busy | reset | fire |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [00] | RW | fire\_alct\_rxd | 0 | Set new phase, software sets then unsets |
| [01] | RW | reset\_alct\_rxd | 0 | Reset current phase to 32 |
| [02] | R | phaser\_busy\_alct\_rxd | 0 | Phase shifter busy |
| [03] | R | lock\_alct\_rxd | 1 | DCM lock status |
| [06:04] | R | phaser\_sm\_alct\_rxd[2:0] | 0 | Phase shifter machine state vector |
| [07] | RW | alct\_rxd\_posneg | 0 | 0=latch inter-stage on falling main clock edge  1=latch inter-stage on rising main clock edge |
| [15:08] | RW | alct\_rxd\_delay[7:0] | 32 | Phase delay to latch data received from ALCT  approximately 0.1ns steps (clock period/256) |

Adr 110 ADR\_PHASER1 ALCT txd Digital Phase Shifter

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| alct  txd  delay  7 | alct  txd  delay  6 | alct  txd  delay  5 | alct  txd  delay  4 | alct  txd  delay  3 | alct  txd  delay  2 | alct  txd  delay  1 | alct  txd  delay  0 | pos  neg | sm  2 | sm  1 | sm  0 | lock | busy | reset | fire |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [00] | RW | fire\_alct\_txd | 0 | Set new phase, software sets then unsets |
| [01] | RW | reset\_alct\_txd | 0 | Reset current phase to 32 |
| [02] | R | phaser\_busy\_alct\_txd | 0 | Phase shifter busy |
| [03] | R | lock\_alct\_txd | 1 | DCM lock status |
| [06:04] | R | phaser\_sm\_alct\_txd[2:0] | 0 | Phase shifter machine state vector |
| [07] | RW | alct\_txd\_posneg | 0 | 0=latch inter-stage on falling main clock edge  1=latch inter-stage on rising main clock edge |
| [15:08] | RW | alct\_txd\_delay[7:0] | 32 | Phase delay for data transmitted to ALCT  approximately 0.1ns steps (clock period/256) |

Adr 112 ADR\_PHASER2 CFEB0 rxd Digital Phase Shifter

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| cfeb  rxd  delay  7 | cfeb  rxd  delay  6 | cfeb  rxd  delay  5 | cfeb  rxd  delay  4 | cfeb  rxd  delay  3 | cfeb  rxd  delay  2 | cfeb  rxd  delay  1 | cfeb  rxd  delay  0 | pos  neg | sm  2 | sm  1 | sm  0 | lock | busy | reset | fire |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [00] | RW | fire\_cfeb0\_rxd | 0 | Set new phase, software sets then unsets |
| [01] | RW | reset\_cfeb0\_rxd | 0 | Reset current phase to 32 |
| [02] | R | phaser\_busy\_cfeb0\_rxd | 0 | Phase shifter busy |
| [03] | R | lock\_cfeb0\_rxd | 1 | DCM lock status |
| [06:04] | R | phaser\_sm\_cfeb0\_rxd[2:0] | 0 | Phase shifter machine state vector |
| [07] | RW | cfeb0\_rxd\_posneg | 0 | 0=latch inter-stage on falling main clock edge  1=latch inter-stage on rising main clock edge |
| [15:08] | RW | cfeb0\_rxd\_delay[7:0] | 32 | Phase delay to latch data received from CFEB  approximately 0.1ns steps (clock period/256) |

Adr 114 ADR\_PHASER3 CFEB1 rxd Digital Phase Shifter

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| cfeb  rxd  delay  7 | cfeb  rxd  delay  6 | cfeb  rxd  delay  5 | cfeb  rxd  delay  4 | cfeb  rxd  delay  3 | cfeb  rxd  delay  2 | cfeb  rxd  delay  1 | cfeb  rxd  delay  0 | pos  neg | sm  2 | sm  1 | sm  0 | lock | busy | reset | fire |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [00] | RW | fire\_cfeb1\_rxd | 0 | Set new phase, software sets then unsets |
| [01] | RW | reset\_cfeb1\_rxd | 0 | Reset current phase to 32 |
| [02] | R | phaser\_busy\_cfeb1\_rxd | 0 | Phase shifter busy |
| [03] | R | lock\_cfeb1\_rxd | 1 | DCM lock status |
| [06:04] | R | phaser\_sm\_cfeb1\_rxd[2:0] | 0 | Phase shifter machine state vector |
| [07] | RW | cfeb1\_rxd\_posneg | 0 | 0=latch inter-stage on falling main clock edge  1=latch inter-stage on rising main clock edge |
| [15:08] | RW | cfeb1\_rxd\_delay[7:0] | 32 | Phase delay to latch data received from CFEB  approximately 0.1ns steps (clock period/256) |

Adr 116 ADR\_PHASER4 CFEB2 rxd Digital Phase Shifter

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| cfeb  rxd  delay  7 | cfeb  rxd  delay  6 | cfeb  rxd  delay  5 | cfeb  rxd  delay  4 | cfeb  rxd  delay  3 | cfeb  rxd  delay  2 | cfeb  rxd  delay  1 | cfeb  rxd  delay  0 | pos  neg | sm  2 | sm  1 | sm  0 | lock | busy | reset | fire |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [00] | RW | fire\_cfeb2\_rxd | 0 | Set new phase, software sets then unsets |
| [01] | RW | reset\_cfeb2\_rxd | 0 | Reset current phase to 32 |
| [02] | R | phaser\_busy\_cfeb2\_rxd | 0 | Phase shifter busy |
| [03] | R | lock\_cfeb2\_rxd | 1 | DCM lock status |
| [06:04] | R | phaser\_sm\_cfeb2\_rxd[2:0] | 0 | Phase shifter machine state vector |
| [07] | RW | cfeb2\_rxd\_posneg | 0 | 0=latch inter-stage on falling main clock edge  1=latch inter-stage on rising main clock edge |
| [15:08] | RW | cfeb2\_rxd\_delay[7:0] | 32 | Phase delay to latch data received from CFEB  approximately 0.1ns steps (clock period/256) |

Adr 118 ADR\_PHASER5 CFEB3 rxd Digital Phase Shifter

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| cfeb  rxd  delay  7 | cfeb  rxd  delay  6 | cfeb  rxd  delay  5 | cfeb  rxd  delay  4 | cfeb  rxd  delay  3 | cfeb  rxd  delay  2 | cfeb  rxd  delay  1 | cfeb  rxd  delay  0 | pos  neg | sm  2 | sm  1 | sm  0 | lock | busy | reset | fire |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [00] | RW | fire\_cfeb3\_rxd | 0 | Set new phase, software sets then unsets |
| [01] | RW | reset\_cfeb3\_rxd | 0 | Reset current phase to 32 |
| [02] | R | phaser\_busy\_cfeb3\_rxd | 0 | Phase shifter busy |
| [03] | R | lock\_cfeb3\_rxd | 1 | DCM lock status |
| [06:04] | R | phaser\_sm\_cfeb3\_rxd[2:0] | 0 | Phase shifter machine state |
| [07] | RW | cfeb3\_rxd\_posneg | 0 | 0=latch inter-stage on falling main clock edge  1=latch inter-stage on rising main clock edge |
| [15:08] | RW | cfeb3\_rxd\_delay[7:0] | 32 | Phase delay to latch data received from CFEB  approximately 0.1ns steps (clock period/256) |

Adr 11A ADR\_PHASER6 CFEB4 rxd Digital Phase Shifter

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| cfeb  rxd  delay  7 | cfeb  rxd  delay  6 | cfeb  rxd  delay  5 | cfeb  rxd  delay  4 | cfeb  rxd  delay  3 | cfeb  rxd  delay  2 | cfeb  rxd  delay  1 | cfeb  rxd  delay  0 | pos  neg | sm  2 | sm  1 | sm  0 | lock | busy | reset | fire |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [00] | RW | fire\_cfeb4\_rxd | 0 | Set new phase, software sets then unsets |
| [01] | RW | reset\_cfeb4\_rxd | 0 | Reset current phase to 32 |
| [02] | R | phaser\_busy\_cfeb4\_rxd | 0 | Phase shifter busy |
| [03] | R | lock\_cfeb4\_rxd | 1 | DCM lock status |
| [06:04] | R | phaser\_sm\_cfeb4\_rxd[2:0] | 0 | Phase shifter machine state vector |
| [07] | RW | cfeb4\_rxd\_posneg | 0 | 0=latch inter-stage on falling main clock edge  1=latch inter-stage on rising main clock edge |
| [15:08] | RW | cfeb4\_rxd\_delay[7:0] | 32 | Phase delay to latch data received from CFEB  approximately 0.1ns steps (clock period/256) |

Adr 11C ADR\_DELAY0\_INT CFEB DDR RxD Interstage Delays

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| cfeb3  delay  3 | cfeb3  delay  2 | cfeb3  delay  1 | cfeb3  delay  0 | cfeb2  delay  3 | cfeb2  delay  2 | cfeb2  delay  1 | cfeb2  delay  0 | cfeb1  delay  3 | cfeb1  delay  2 | cfeb1  delay  1 | cfeb1  delay  0 | cfeb0  delay  3 | cfeb0  delay  2 | cfeb0  delay  1 | cfeb0  delay  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [03:00] | RW | cfeb0\_rxd\_int\_delay[3:0] | 0 | Delay data received from CFEB0 by integer bx |
| [07:04] | RW | cfeb1\_rxd\_int\_delay [3:0] | 0 | Delay data received from CFEB1 by integer bx |
| [11:08] | RW | cfeb2\_rxd\_int\_delay [3:0] | 0 | Delay data received from CFEB2 by integer bx |
| [15:12] | RW | cfeb3\_rxd\_int\_delay [3:0] | 0 | Delay data received from CFEB3 by integer bx |

Adr 11E ADR\_DELAY1\_INT CFEB DDR RxD Interstage Delays Continued

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | cfeb6  delay  3 | cfeb6  delay  2 | cfeb6  delay  1 | cfeb6  delay  0 | cfeb5  delay  3 | cfeb5  delay  2 | cfeb5  delay  1 | cfeb5  delay  0 | cfeb4  delay  3 | cfeb4  delay  2 | cfeb4  delay  1 | cfeb4  delay  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [03:00] | RW | cfeb4\_rxd\_int\_delay[3:0] | 0 | Delay data received from CFEB4 by integer bx |
| [07:04] | RW | cfeba\_rxd\_int\_delay[3:0] | 0 | Delay data received from A-side CFEBs by int bx |
| [11:08] | RW | cfebb\_rxd\_int\_delay[3:0] | 0 | Delay data received from B-side CFEBs by int bx |
| [15:12] | RW | -- | 0 | Unassigned |

Adr 120 ADR\_SYNC\_ERR\_CTRL Synchronization Error Control

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| sync  err  forced | clock  lock  err | bx0  match  err | alct  ecc tx  err | alct  ecc rx  err | clct  bx0  err | sync  err | err  stops  L1As | err  stops  pretrig | err  blanks  LCTs | clock  lock  lost en | bx0  match  en | alct  tx  ecc en | alct  rx  ecc en | clct  bx0  en | sync  err  reset |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [00] | RW | sync\_err\_reset | 0 | VME sync error reset |
| Sync error source enables: | | | | |
| [01] | RW | clct\_bx0\_sync\_err\_en | 1 | TMB clock pulse count err:  bxn!=0+offset at ttc\_bx0 arrival |
| [02] | RW | alct\_ecc\_rx\_err\_en | 0 | ALCT uncorrected ECC error in data  ALCT received from TMB |
| [03] | RW | alct\_ecc\_tx\_err\_en | 0 | ALCT uncorrected ECC error in data ALCT transmitted to TMB |
| [04] | RW | bx0\_match\_err\_en | 0 | ALCT alct\_bx0 != clct\_bx0 in LCT to MPC |
| [05] | RW | clock\_lock\_lost\_err\_en | 0 | 40MHz main clock lost lock |
| Sync error action enables: | | | | |
| [06] | RW | sync\_err\_blanks\_mpc\_en | 0 | Sync error blanks LCTs to MPC |
| [07] | RW | sync\_err\_stops\_pretrig\_en | 0 | Sync error stops CLCT pre-triggers |
| [08] | RW | sync\_err\_stops\_readout\_en | 0 | Sync error stops L1A readouts |
| Sync error types latched for VME readout: | | | | |
| [09] | R | sync\_err | 0 | Sync error OR of enabled types of error |
| [10] | R | clct\_bx0\_sync\_err\_ff | 0 | TMB clock pulse count err:  bxn!=0+offset at ttc\_bx0 arrival |
| [11] | R | alct\_ecc\_rx\_err\_ff | 0 | ALCT uncorrected ECC error in data  ALCT received from TMB |
| [12] | R | alct\_ecc\_tx\_err\_ff | 0 | ALCT uncorrected ECC error in data  ALCT transmitted to TMB |
| [13] | R | bx0\_match\_err\_ff | 0 | ALCT alct\_bx0 != clct\_bx0 in LCT to MPC |
| [14] |  | clock\_lock\_lost\_err\_ff | 0 | 40MHz main clock lost lock |
| [15] | RW | sync\_err\_forced | 0 | Force sync\_err=1 |

See p47 Adr86[1:0] for tmb\_sync\_err\_en[1:0] Allow sync\_err to MPC for either muon

See p38 Adr38[2] for alct\_ecc\_err\_blank Blank alct muons having uncorrected ecc errors

Adr 122 ADR\_CFEB\_BADBITS\_CTRL CFEB Bad Bits Control/Status

(see 0x15C for V6)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| cfeb  blocked | found  cfeb4 | found  cfeb3 | found  cfeb2 | found  cfeb1 | found  cfeb0 | block  cfeb4 | block  cfeb3 | block  cfeb2 | block  cfeb1 | block  cfeb0 | reset  cfeb4 | reset  cfeb3 | reset cfeb2 | reset  cfeb1 | reset  cfeb0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [04:00] | RW | cfeb\_badbits\_reset[4:0] | 0 | 0x1F=Reset bad cfeb bits FFs for cfeb[n] |
| [09:05] | RW | cfeb\_badbits\_block[4:0] | 0 | 0x1F=Block bad cfeb bits in cfeb[n] |
| [14:10] | R | cfeb\_badbits\_found[4:0] | 0 | CFEB[n] has at least 1 bad bit |
| [15] | R | cfeb\_badbits\_blocked | 0 | At least one CFEB has a bad bit that was blocked |

Adr 124 ADR\_CFEB\_BADBITS\_TIMER CFEB Bad Bits Check Interval

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| nbx  15 | nbx  14 | nbx  13 | nbx  12 | nbx  11 | nbx  10 | nbx  9 | nbx  8 | nbx  7 | nbx  6 | nbx  5 | nbx  4 | nbx  3 | nbx  2 | nbx  1 | nbx  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [15:00] | RW | cfeb\_badbits\_nbx [15:0] | 3564 | Check Interval for CFEB bad bits, bx units |

Adr 126 ADR\_CFEB0\_BADBITS\_LY01 CFEB0 Ly0,Ly1 Bad Bits List

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ly1  distrip  7 | ly1  distrip  6 | ly1  distrip  5 | ly1  distrip  4 | ly1  distrip  3 | ly1  distrip  2 | ly1  distrip  1 | ly1  distrip  0 | ly0  distrip  7 | ly0  distrip  6 | ly0  distrip  5 | ly0  distrip  4 | ly0  distrip  3 | ly0  distrip  2 | ly0  distrip  1 | ly0  distrip  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [07:00] | R | cfeb0\_ly0\_badbits [7:0] | 000000002 | 1=CFEB rx bit[n] went bad |
| [15:08] | R | cfeb0\_ly1\_badbits [7:0] | 000000002 | 1=CFEB rx bit[n] went bad |

Adr 128 ADR\_CFEB0\_BADBITS\_LY23 CFEB0 Ly2,Ly3 Bad Bits List

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| [07:00] | R | cfeb0\_ly2\_badbits [7:0] | 000000002 | 1=CFEB rx bit[n] went bad |
| [15:08] | R | cfeb0\_ly3\_badbits [7:0] | 000000002 | 1=CFEB rx bit[n] went bad |

Adr 12A ADR\_CFEB0\_BADBITS\_LY45 CFEB0 Ly4,Ly5 Bad Bits List

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| [07:00] | R | cfeb0\_ly4\_badbits [7:0] | 000000002 | 1=CFEB rx bit[n] went bad |
| [15:08] | R | cfeb0\_ly5\_badbits [7:0] | 000000002 | 1=CFEB rx bit[n] went bad |

Adr 12C ADR\_CFEB1\_BADBITS\_LY01 CFEB1 Ly0,Ly1 Bad Bits List

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| [07:00] | R | cfeb1\_ly0\_badbits [7:0] | 000000002 | 1=CFEB rx bit[n] went bad |
| [15:08] | R | cfeb1\_ly1\_badbits [7:0] | 000000002 | 1=CFEB rx bit[n] went bad |

Adr 12E ADR\_CFEB1\_BADBITS\_LY23 CFEB1 Ly2,Ly3 Bad Bits List

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| [07:00] | R | cfeb1\_ly2\_badbits [7:0] | 000000002 | 1=CFEB rx bit[n] went bad |
| [15:08] | R | cfeb1\_ly3\_badbits [7:0] | 000000002 | 1=CFEB rx bit[n] went bad |

Adr 130 ADR\_CFEB1\_BADBITS\_LY45 CFEB1 Ly4,Ly5 Bad Bits List

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ly1  distrip  7 | ly1  distrip  6 | ly1  distrip  5 | ly1  distrip  4 | ly1  distrip  3 | ly1  distrip  2 | ly1  distrip  1 | ly1  distrip  0 | ly0  distrip  7 | ly0  distrip  6 | ly0  distrip  5 | ly0  distrip  4 | ly0  distrip  3 | ly0  distrip  2 | ly0  distrip  1 | ly0  distrip  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [07:00] | R | cfeb1\_ly4\_badbits [7:0] | 000000002 | 1=CFEB rx bit[n] went bad |
| [15:08] | R | cfeb1\_ly5\_badbits [7:0] | 000000002 | 1=CFEB rx bit[n] went bad |

Adr 132 ADR\_CFEB2\_BADBITS\_LY01 CFEB2 Ly0,Ly1 Bad Bits List

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| [07:00] | R | cfeb2\_ly0\_badbits [7:0] | 000000002 | 1=CFEB rx bit[n] went bad |
| [15:08] | R | cfeb2\_ly1\_badbits [7:0] | 000000002 | 1=CFEB rx bit[n] went bad |

Adr 134 ADR\_CFEB2\_BADBITS\_LY23 CFEB2 Ly2,Ly3 Bad Bits List

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| [07:00] | R | cfeb2\_ly2\_badbits [7:0] | 000000002 | 1=CFEB rx bit[n] went bad |
| [15:08] | R | cfeb2\_ly3\_badbits [7:0] | 000000002 | 1=CFEB rx bit[n] went bad |

Adr 136 ADR\_CFEB2\_BADBITS\_LY45 CFEB2 Ly4,Ly5 Bad Bits List

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| [07:00] | R | cfeb2\_ly4\_badbits [7:0] | 000000002 | 1=CFEB rx bit[n] went bad |
| [15:08] | R | cfeb2\_ly5\_badbits [7:0] | 000000002 | 1=CFEB rx bit[n] went bad |

Adr 138 ADR\_CFEB3\_BADBITS\_LY01 CFEB3 Ly0,Ly1 Bad Bits List

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| [07:00] | R | cfeb3\_ly0\_badbits [7:0] | 000000002 | 1=CFEB rx bit[n] went bad |
| [15:08] | R | cfeb3\_ly1\_badbits [7:0] | 000000002 | 1=CFEB rx bit[n] went bad |

Adr 13A ADR\_CFEB3\_BADBITS\_LY23 CFEB3 Ly2,Ly3 Bad Bits List

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| [07:00] | R | cfeb3\_ly2\_badbits [7:0] | 000000002 | 1=CFEB rx bit[n] went bad |
| [15:08] | R | cfeb3\_ly3\_badbits [7:0] | 000000002 | 1=CFEB rx bit[n] went bad |

Adr 13C ADR\_CFEB3\_BADBITS\_LY45 CFEB3 Ly4,Ly5 Bad Bits List

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| [07:00] | R | cfeb3\_ly4\_badbits [7:0] | 000000002 | 1=CFEB rx bit[n] went bad |
| [15:08] | R | cfeb3\_ly5\_badbits [7:0] | 000000002 | 1=CFEB rx bit[n] went bad |

Adr 13E ADR\_CFEB4\_BADBITS\_LY01 CFEB4 Ly0,Ly1 Bad Bits List

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| [07:00] | R | cfeb4\_ly0\_badbits [7:0] | 000000002 | 1=CFEB rx bit[n] went bad |
| [15:08] | R | cfeb4\_ly1\_badbits [7:0] | 000000002 | 1=CFEB rx bit[n] went bad |

Adr 140 ADR\_CFEB4\_BADBITS\_LY23 CFEB4 Ly2,Ly3 Bad Bits List

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| [07:00] | R | cfeb4\_ly2\_badbits [7:0] | 000000002 | 1=CFEB rx bit[n] went bad |
| [15:08] | R | cfeb4\_ly3\_badbits [7:0] | 000000002 | 1=1=CFEB rx bit[n] went bad |

Adr 142 ADR\_CFEB4\_BADBITS\_LY45 CFEB4 Ly4,Ly5 Bad Bits List

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| [07:00] | R | cfeb4\_ly4\_badbits [7:0] | 000000002 | 1=CFEB rx bit[n] went bad |
| [15:08] | R | cfeb4\_ly5\_badbits [7:0] | 000000002 | 1=CFEB rx bit[n] went bad |

Adr 144 ADR\_ALCT\_STARTUP\_DELAY ALCT startup delay milliseconds for Spartan-6

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| d[15] | d[14] | d[13] | d[12] | d[11] | d[10] | d[9] | d[8] | d[7] | d[6] | d[5] | d[4] | d[3] | d[2] | d[1] | d[0] |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [15:00] | RW | alct\_startup\_delay [15:0] | 116 | Msec to wait after TMB powers up before  Initializing DDD delays and ALCT JTAG.  This setting is only used after TMB first powers up or has a hard reset, so changes need to be stored in VME PROM.  ALCT Spartan-6 takes 212msec to configure.  TMB Virtex-2 takes 100msec.  This register holds the number of msec to wait after TMB configures, so a value of 116 corresponds to 100ms + 116ms =216ms after a TMB hard reset. |

Adr 146 ADR\_ALCT\_STARTUP\_STATUS ALCT startup delay machine status

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| mmcm\_lostlock\_count | | | | | | | | alct  start  done | alct  wait  cfg | alct  wait  vme | alct  wait  dll | alct  start  msec | vsm  ready | power  up | global  reset |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [00] | R | global\_reset | 0 | Global reset |
| [01] | R | power\_up | 1 | DLL clock locked, we wait for it |
| [02] | R | vsm\_ready | 1 | Injector RAM read data MSBs |
| [03] | R | alct\_startup\_msec | 0 | Startup machine millisecond pulse, width=25ns |
| [04] | R | alct\_wait\_dll | 0 | Startup machine waiting for TMB DLL lock |
| [05] | R | alct\_wait\_vme | 0 | Startup machine waiting for TMB VME user PROM |
| [06] | R | alct\_wait\_cfg | 0 | Startup machine waiting for ALCT FPGA to config |
| [07] | R | alct\_startup\_done | 1 | Startup machine done ALCT FPGA assumed configured |
| [15:08] | R | mmcm\_lostlock\_count | 0 | FPGA MMCM lost-lock count (full scale is hex FC) |

Adr 148 ADR\_V6\_SNAP12\_QPLL Virtex-6 SNAP12 Serial interface + QPLL status

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| qpll\_lostlock\_count | | | | | | | | tmbmmcm\_locklost | r12  fok | r12  sdat | r12  sclk | 0 | qpll  err | qpll  lock | qpll  nrst |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [00] | RW | qpll\_nrst | 1 | nReset QPLL, 0=reset |
| [01] | R | qpll\_lock | 0 | QPLL locked status |
| [02] | R | qpll\_err | 0 | QPLL error status |
| [03] | R | qpll\_locklost | 0 | QPLL lost its lock at least once since the last reset |
| [04] | R | r12\_sclk | 1 | SNAP12 Serial interface clock, drive high |
| [05] | R | r12\_sdat | 0 | SNAP12 Serial interface data |
| [06] | R | r12\_fok | 0 | SNAP12 Serial interface status |
| [07] | R | tmbmmcm\_locklost | 0 | FPGA MMCM lost its lock since the last reset |
| [15:08] | R | qpll\_lostlock\_count | 0 | QPLL lost-lock count (full scale is hex FC) |

Adr 14A ADR\_V6\_GTX\_RX\_ALL Virtex-6 master GTX control and status

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| gtx err sum bit 7 | gtx err sum bit 6 | gtx err sum bit 5 | gtx err sum bit 4 | gtx err sum bit 3 | gtx err sum bit 2 | gtx err sum bit 1 | gtx err sum bit 0 | gtx  pol  swap | gtx  link bad | gtx linkhad err | gtx  link good | gtx  sync  done | gtx  en  prbs | gtx  reset | gtx  en |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [00] | RW | gtx\_rx\_enable\_all | 1 | Enable all GTX optical inputs (0 puts GTX in reset state) |
| [01] | RW | gtx\_rx\_reset\_all | 0 | Reset the sync stage of all GTX |
| [02] | RW | gtx\_rx\_en\_prbs\_test\_all | 0 | Select all GTX for PRBS test input mode |
| [03] | R | &gtx\_rx\_sync\_done[6:0] | 1 | All GTX are ready |
| [04] | R | &gtx\_link\_good[6:0] | 1 | All GTX links are locked (over 15 BX with clean structure) |
| [05] | R | |gtx\_link\_had\_err[6:0] | 0 | At least one GTX link had an error since last reset |
| [06] | R | |gtx\_link\_bad[6:0] | 0 | At least one GTX link had over 100 errors |
| [07] | R | |gtx\_rx\_pol\_swap[6:0] | 0 | GTX 5,6 [ie dcfeb 4,5] have swapped rx board routes |
| [15:8] | R | gtx\_rx\_err\_count\_sum\_all | 0 | Sum of GTX link error counts (full scale count is hex FE) |

Adr 14C-158 ADR\_V6\_GTX\_RX0-6 Virtex-6 individual GTX (idcfeb[6:0]) control and status

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| gtx err countbit 7 | gtx err countbit 6 | gtx err countbit 5 | gtx err countbit 4 | gtx err countbit 3 | gtx err countbit 2 | gtx err countbit 1 | gtx err countbit 0 | gtx  pol  swap | gtx  link bad | gtx linkhad err | gtx  link good | gtx  sync  done | gtx  en  prbs | gtx  reset | gtx  en |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [00] | RW | gtx\_rx\_enable[idcfeb] | 1 | Enable this GTX optical input (0 puts GTX in reset state) |
| [01] | RW | gtx\_rx\_reset[idcfeb] | 0 | Reset the sync stage of this GTX |
| [02] | RW | gtx\_rx\_en\_prbs\_test[idcfeb] | 0 | Select this GTX for PRBS test input mode |
| [03] | R | gtx\_rx\_sync\_done[idcfeb] | 1 | GTX ready |
| [04] | R | gtx\_link\_good | 1 | GTX link is locked (over 15 BX with clean data frames) |
| [05] | R | gtx\_link\_had\_err | 0 | GTX link had an error (bad data frame) since last reset |
| [06] | R | gtx\_link\_bad | 0 | GTX link had over 100 errors since last reset |
| [07] | R | gtx\_rx\_pol\_swap[idcfeb] | 0 | GTX 5,6 [ie dcfeb 4,5] have swapped rx board routes |
| [15:8] | R | gtx\_rx\_err\_count[idcfeb] | 0 | GTX link error count (full scale count is hex E0) |

Adr 15A ADR\_V6\_SYSMON Virtex-6 Sysmon ADC

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| adc\_data  bit 9 | adc\_data  bit 8 | adc\_data  bit 7 | adc\_data  bit 6 | adc\_data  bit 5 | adc\_data  bit 4 | adc\_data  bit 3 | adc\_data  bit 2 | adc\_data  bit 1 | adc\_data  bit 0 | adc\_valid  or  adc\_reset | adc\_adr  bit 4 | adc\_adr  bit 3 | adc\_adr  bit 2 | adc\_adr  bit 1 | adc\_adr  bit 0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [04:00] | RW | adc\_adr[4:0] | 0 | ADC channel |
| [05] | R | adc\_valid | 0 | ADC RAM has valid data for this adc\_adr, readonly |
| [05] | W | adc\_reset | 0 | Reset Sysmon module, writeonly |
| [15:6] | R | adc\_data[15:6] | 0 | ADC counts for this adc\_adr |

Virtex-6 Sysmon ADC Channel Assignments:

adr Source Units Conversion Factor

0 Temperature Degrees C = (ADC code × 503.975)/1024 – 273.15

1 VccINT Volts = (ADC Code / 1024) x 3V

2 VccAUX Volts = (ADC Code / 1024) x 3V

4 Vref 1.25V Volts = (ADC Code / 1024) x 3V

5 Vzero 0.00V Volts = (ADC Code / 1024) x 3V

Adr 15C ADR\_V6\_CFEB\_BADBITS\_CTRL CFEB Bad Bits Control/Status (See Adr 0x122)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | found  cfeb6 | found  cfeb5 | block  cfeb6 | block  cfeb5 | reset  cfeb6 | reset  cfeb5 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [01:00] | RW | cfeb\_badbits\_reset[6:5] | 0 | 0x1F=Reset bad cfeb bits FFs for cfeb[n] |
| [03:02] | RW | cfeb\_badbits\_block[6:5] | 0 | 0x1F=Block bad cfeb bits in cfeb[n] |
| [05:04] | R | cfeb\_badbits\_found[6:5] | 0 | CFEB[n] has at least 1 bad bit |
| [15:06] | RW | -- | 0 | Unassigned |

Adr 15E ADR\_ V6\_CFEB5\_BADBITS\_LY01 CFEB5 Ly0,Ly1 Bad Bits List

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ly1  distrip  7 | ly1  distrip  6 | ly1  distrip  5 | ly1  distrip  4 | ly1  distrip  3 | ly1  distrip  2 | ly1  distrip  1 | ly1  distrip  0 | ly0  distrip  7 | ly0  distrip  6 | ly0  distrip  5 | ly0  distrip  4 | ly0  distrip  3 | ly0  distrip  2 | ly0  distrip  1 | ly0  distrip  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [07:00] | R | cfeb5\_ly0\_badbits [7:0] | 000000002 | 1=CFEB rx bit[n] went bad |
| [15:08] | R | cfeb5\_ly1\_badbits [7:0] | 000000002 | 1=CFEB rx bit[n] went bad |

Adr 160 ADR\_ V6\_CFEB5\_BADBITS\_LY23 CFEB5 Ly2,Ly3 Bad Bits List

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| [07:00] | R | cfeb5\_ly2\_badbits [7:0] | 000000002 | 1=CFEB rx bit[n] went bad |
| [15:08] | R | cfeb5\_ly3\_badbits [7:0] | 000000002 | 1=CFEB rx bit[n] went bad |

Adr 162 ADR\_ V6\_CFEB5\_BADBITS\_LY45 CFEB5 Ly4,Ly5 Bad Bits List

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| [07:00] | R | cfeb5\_ly4\_badbits [7:0] | 000000002 | 1=CFEB rx bit[n] went bad |
| [15:08] | R | cfeb5\_ly5\_badbits [7:0] | 000000002 | 1=CFEB rx bit[n] went bad |

Adr 164 ADR\_ V6\_CFEB6\_BADBITS\_LY01 CFEB6 Ly0,Ly1 Bad Bits List

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| [07:00] | R | cfeb6\_ly0\_badbits [7:0] | 000000002 | 1=CFEB rx bit[n] went bad |
| [15:08] | R | cfeb6\_ly1\_badbits [7:0] | 000000002 | 1=CFEB rx bit[n] went bad |

Adr 166 ADR\_ V6\_CFEB6\_BADBITS\_LY23 CFEB6 Ly2,Ly3 Bad Bits List

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| [07:00] | R | cfeb6\_ly2\_badbits [7:0] | 000000002 | 1=CFEB rx bit[n] went bad |
| [15:08] | R | cfeb6\_ly3\_badbits [7:0] | 000000002 | 1=CFEB rx bit[n] went bad |

Adr 168 ADR\_ V6\_CFEB6\_BADBITS\_LY45 CFEB6 Ly4,Ly5 Bad Bits List

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| [07:00] | R | cfeb6\_ly4\_badbits [7:0] | 000000002 | 1=CFEB rx bit[n] went bad |
| [15:08] | R | cfeb6\_ly5\_badbits [7:0] | 000000002 | 1=CFEB rx bit[n] went bad |

Adr 16A ADR\_V6\_PHASER7 ME1/1 A-Side CFEBs rxd Digital Phase Shifter

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| cfeb  rxd  delay  7 | cfeb  rxd  delay  6 | cfeb  rxd  delay  5 | cfeb  rxd  delay  4 | cfeb  rxd  delay  3 | cfeb  rxd  delay  2 | cfeb  rxd  delay  1 | cfeb  rxd  delay  0 | pos  neg | sm  2 | sm  1 | sm  0 | lock | busy | reset | fire |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [00] | RW | fire\_cfeba\_rxd | 0 | Set new phase, software sets then unsets |
| [01] | RW | reset\_cfeba\_rxd | 0 | Reset current phase to 32 |
| [02] | R | phaser\_busy\_cfeba\_rxd | 0 | Phase shifter busy |
| [03] | R | lock\_cfeba\_rxd | 1 | DCM lock status |
| [06:04] | R | phaser\_sm\_cfeba\_rxd[2:0] | 0 | Phase shifter machine state vector |
| [07] | RW | cfeba\_rxd\_posneg | 0 | 0=latch inter-stage on falling main clock edge  1=latch inter-stage on rising main clock edge |
| [15:08] | RW | cfeba\_rxd\_delay[7:0] | 32 | Phase delay to latch data received from CFEB  approximately 0.1ns steps (clock period/256) |

Adr 16C ADR\_V6\_PHASER8 ME1/1 B-Side CFEBs rxd Digital Phase Shifter

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| cfeb  rxd  delay  7 | cfeb  rxd  delay  6 | cfeb  rxd  delay  5 | cfeb  rxd  delay  4 | cfeb  rxd  delay  3 | cfeb  rxd  delay  2 | cfeb  rxd  delay  1 | cfeb  rxd  delay  0 | pos  neg | sm  2 | sm  1 | sm  0 | lock | busy | reset | fire |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [00] | RW | fire\_cfebb\_rxd | 0 | Set new phase, software sets then unsets |
| [01] | RW | reset\_cfebb\_rxd | 0 | Reset current phase to 32 |
| [02] | R | phaser\_busy\_cfebb\_rxd | 0 | Phase shifter busy |
| [03] | R | lock\_cfebb\_rxd | 1 | DCM lock status |
| [06:04] | R | phaser\_sm\_cfebb\_rxd[2:0] | 0 | Phase shifter machine state vector |
| [07] | RW | cfebb\_rxd\_posneg | 0 | 0=latch inter-stage on falling main clock edge  1=latch inter-stage on rising main clock edge |
| [15:08] | RW | cfebb\_rxd\_delay[7:0] | 32 | Phase delay to latch data received from CFEB  approximately 0.1ns steps (clock period/256) |

Adr 16E ADR\_V6\_HCM501 CFEB5 Ly0,Ly1 Hot Channel Mask

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ly1  distrip  7 | ly1  distrip  6 | ly1  distrip  5 | ly1  distrip  4 | ly1  distrip  3 | ly1  distrip  2 | ly1  distrip  1 | ly1  distrip  0 | ly0  distrip  7 | ly0  distrip  6 | ly0  distrip  5 | ly0  distrip  4 | ly0  distrip  3 | ly0  distrip  2 | ly0  distrip  1 | ly0  distrip  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [07:00] | RW | cfeb5\_ly0\_hcm[7:0] | 111111112 | 1=Enable DiStrip[7:0] Layer 0 |
| [15:08] | RW | cfeb5\_ly1\_hcm[7:0] | 111111112 | 1=Enable DiStrip[7:0] Layer 1 |

Adr 170 ADR\_V6\_HCM523 CFEB5 Ly2,Ly3 Hot Channel Mask

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| [07:00] | RW | cfeb5\_ly2\_hcm[7:0] | 111111112 | 1=Enable DiStrip[7:0] Layer 2 |
| [15:08] | RW | cfeb5\_ly3\_hcm[7:0] | 111111112 | 1=Enable DiStrip[7:0] Layer 3 |

Adr 172 ADR\_V6\_HCM545 CFEB5 Ly4,Ly5 Hot Channel Mask

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| [07:00] | RW | cfeb5\_ly4\_hcm[7:0] | 111111112 | 1=Enable DiStrip[7:0] Layer 4 |
| [15:08] | RW | cfeb5\_ly5\_hcm[7:0] | 111111112 | 1=Enable DiStrip[7:0] Layer 5 |

Adr 174 ADR\_V6\_HCM601 CFEB6 Ly0,Ly1 Hot Channel Mask

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| [07:00] | RW | cfeb6\_ly0\_hcm[7:0] | 111111112 | 1=Enable DiStrip[7:0] Layer 0 |
| [15:08] | RW | cfeb6\_ly1\_hcm[7:0] | 111111112 | 1=Enable DiStrip[7:0] Layer 1 |

Adr 176 ADR\_V6\_HCM623 CFEB6 Ly2,Ly3 Hot Channel Mask

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| [07:00] | RW | cfeb6\_ly2\_hcm[7:0] | 111111112 | 1=Enable DiStrip[7:0] Layer 2 |
| [15:08] | RW | cfeb6\_ly3\_hcm[7:0] | 111111112 | 1=Enable DiStrip[7:0] Layer 3 |

Adr 178 ADR\_V6\_HCM645 CFEB6 Ly4,Ly5 Hot Channel Mask

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| [07:00] | RW | cfeb6\_ly4\_hcm[7:0] | 111111112 | 1=Enable DiStrip[7:0] Layer 4 |
| [15:08] | RW | cfeb6\_ly5\_hcm[7:0] | 111111112 | 1=Enable DiStrip[7:0] Layer 5 |

Adr 17A ADR\_V6\_EXTEND DCFEB 7-bit extensions to 5 bit fields in 0x42, 0x68

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | cfeben  6  read | cfeben  5  read | cfeben  6  vme | cfeben  5  vme | inj  mask  6 | inj  mask  5 | inj  febsel  6 | inj  febsel  5 | mask  all  cfeb6 | mask  all  cfeb5 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [01:00] | RW | mask\_all[6:5] | 112 | Extend 0x42[4:0] = mask\_all[4:0] |
| [03:02] | RW | inj\_febsel[6:5] | 0 | Extend 0x42[9:5] = inj\_febsel[4:0] |
| [05:04] | RW | injector\_mask[6:5] | 112 | Extend 0x42[14:10] = injector\_mask\_cfeb[4:0] |
| [07:06] | RW | cfeb\_en\_vme[6:5] | 112 | Extend 0x68[14:10] = cfeb\_en\_vme[4:0] |
| [09:08] | R | cfeb\_en[6:5] | 112 | Extend 0x68[14:10] = cfeb\_en[4:0] readback |
| [15:10] | RW | -- | 0 | Unassigned |

Adr 17C ADR\_MPC0\_FRAME0\_FIFO MPC0 Frame0 Data Sent to MPC stored in FIFO

(see also Adr 88)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 1st  vpf | lct  1st q  3 | lct  1st q  2 | lct  1st q  1 | lct  1st q  0 | clct  1st pat  3 | clct  1st pat  2 | clct  1st pat  1 | clct  1st pat  0 | alct  1st wg  6 | alct  1st wg  5 | alct  1st wg  4 | alct  1st wg  3 | alct  1st wg  2 | alct  1st wg  1 | alct  1st wg  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [06:00] | R | alct\_first\_key[6:0] | 0-11110 | ALCT first key wire-group |
| [10:07] | R | clct\_first\_pat[3:0] | 0-10 | CLCT first pattern number |
| [14:11] | R | lct\_first\_quality[3:0] | 8 | LCT first muon quality |
| [15] | R | first\_vpf | 1 | First valid pattern flag |

Adr 17E ADR\_MPC0\_FRAME1\_FIFO MPC0 Frame1 Data Sent to MPC stored in FIFO

(see also Adr 8A)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| csc  id  3 | csc  id  2 | csc  id  1 | csc  id  0 | tmb  bx0  local | alct  1st  bxn  0 | sync  err | clct  1st  bend | clct  1st  key  7 | clct  1st  key  6 | clct  1st  key  5 | clct  1st  key  4 | clct  1st  key  3 | clct  1st  key  2 | clct  1st  key  1 | clct  1st  key  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [07:00] | R | clct\_first\_key[7:0] | 0-15910 | CLCT first muon key ½-strip |
| [08] | R | clct\_first\_bend | 0 | CLCT first muon bend direction |
| [09] | R | sync\_err | 0 | BXN does not match at BX0 |
| [10] | R | alct\_first\_bxn[0] | 0-1 | ALCT first muon bunch crossing number |
| [11] | R | clct\_first\_bx0\_local | 0-1 | 1=TMBs bxn[11:0]==0 |
| [15:12] | R | csc\_id[3:0] | 1-9 | CSC chamber ID |

Adr 180 ADR\_MPC1\_FRAME0\_FIFO MPC1 Frame0 Data Sent to MPC stored in FIFO

(see also Adr 8C)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 2nd  vpf | lct  2nd q  3 | lct  2nd q  2 | lct  2nd q  1 | lct  2nd q  0 | clct  2nd pat  3 | clct  2nd pat  2 | clct  2nd pat  1 | clct  2nd pat  0 | alct  2nd wg  6 | alct  2nd wg  5 | alct  2nd wg  4 | alct  2nd wg  3 | alct  2nd wg  2 | alct  2nd wg  1 | alct  2nd wg  0 |

5

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [06:00] | R | alct\_second\_key[6:0] | 0-11110 | ALCT second key wire-group |
| [10:07] | R | clct\_second\_pat[3:0] | 0-10 | CLCT second pattern number |
| [14:11] | R | lct\_second\_quality[3:0] | 8 | LCT second muon quality |
| [15] | R | second\_vpf | 1 | Second valid pattern flag |

Adr 182 ADR\_MPC1\_FRAME1\_FIFO MPC1 Frame1 Data Sent to MPC stored in FIFO

(see also Adr 8E)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| csc  id  3 | csc  id  2 | csc  id  1 | csc  id  0 | tmb  bx0  local | alct  2nd  bxn  0 | sync  err | clct  2nd  bend | clct  2nd  key  7 | clct  2nd  key  6 | clct  2nd  key  5 | clct  2nd  key  4 | clct  2nd  key  3 | clct  2nd  key  2 | clct  2nd  key  1 | clct  2nd  key  0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [07:00] | R | clct\_second\_key[7:0] | 0-15910 | CLCT second muon key ½-strip |
| [08] | R | clct\_second\_bend | 0 | CLCT second muon bend direction |
| [09] | R | sync\_err | 0 | BXN does not match at BX0 |
| [10] | R | alct\_second\_bxn[0] | 0-1 | ALCT second muon bunch crossing number |
| [11] | R | clct\_second\_bx0\_local | 0-1 | 1=TMBs bxn[11:0]==0 |
| [15:12] | R | csc\_id[3:0] | 1-9 | CSC chamber ID |

Adr 184 ADR\_MPC\_FRAMES\_FIFO\_CTRL Control of FIFO Storage for Data Sent to MPC

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| not used | not used | not used | not used | not used | not used | not used | dbiterr | sbiterr | prog full | empty | overflow | write ack | full | read enable | write enable |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Typical | Description |
| [00] | RW | mpc\_frames\_fifo\_ctrl\_wr[0] | 0 | FIFO write enable |
| [01] | RW | mpc\_frames\_fifo\_ctrl\_wr[1] | 0 | FIFO read enable |
| [02] | R | mpc\_frames\_fifo\_ctrl\_full | 0 | FIFO full flag |
| [03] | R | mpc\_frames\_fifo\_ctrl\_wr\_ack | 0 | FIFO write acknowledge |
| [04] | R | mpc\_frames\_fifo\_ctrl\_overflow | 0 | FIFO overflow |
| [05] | R | mpc\_frames\_fifo\_ctrl\_empty | 0 | FIFO empty flag |
| [06] | R | mpc\_frames\_fifo\_ctrl\_prog\_full | 0 | FIFO programmable full |
| [07] | R | mpc\_frames\_fifo\_ctrl\_sbiterr | 0 | FIFO Single Bit Error |
| [08] | R | mpc\_frames\_fifo\_ctrl\_dbiterr | 0 | FIFO Double Bit Error |

Adr 186 ADR\_TMB\_MMCM\_LOCK\_TIME TMB Clock Startup Timer

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| mmcm\_lock\_time | | | | | | | | | | | | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [15:00] | R | mmcm\_lock\_time[15:0] | 0 | Time to lock MMCM, with special test counter |

Adr 188 ADR\_TMB\_POWER\_UP\_TIME TMB Power-up Timer

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [15:00] | R | power\_up\_time[15:0] | 0 | Time to lock MMCM after Hard Reset, in 100 ns units |

Adr 18A ADR\_TMB\_LOAD\_CFG\_TIME TMB Load Config Timer

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [15:00] | R | tmb\_load\_cfg\_time[15:0] | 0 | Time to read config from flash after Hard Reset, in 100 ns units |

Adr 18C ADR\_ALCT\_PHASER\_LOCK\_TIME ALCT Phaser MMCM Lock Timer

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [15:00] | R | phaser\_lock\_time[15:0] | 0 | Time to lock Phaser after Hard Reset, in 100 ns units |

Adr 18E ADR\_ALCT\_LOAD\_CFG\_TIME ALCT Load Config Timer

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [15:00] | R | alct\_load\_cfg\_time[15:0] | 0 | Time to complete ALCT config after alct wait period, in 100 ns units |

Adr 190 ADR\_GTX\_RST\_DONE\_TIME GTX Reset Done Timer

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [15:00] | R | gtx\_rst\_done\_time[15:0] | 0 | Time to finish GTX reset after Hard Reset, in 100 ns units |

Adr 192 ADR\_GTX\_SYNC\_DONE\_TIME GTX Sync Done Timer

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Dir | Signal | Default | Description |
| [15:00] | R | gtx\_sync\_done\_time[15:0] | 0 | Time to finish GTX sync after Hard Reset, in 100 ns units |

TTC Commands

Table 2: Fast Control Bus ccb\_cmd[5..0] Decoding Scheme

|  |  |  |  |
| --- | --- | --- | --- |
| Signal | Code (hex) | Decoded by TMB | Description |
| BX0 (\*) | 01 | Y | Bunch Crossing Zero |
| L1 Reset (\*) | 03 | Y | Reset L1 readout buffers and resynchronize optical links |
| Hard\_reset (\*) | 04 |  | Reload all FPGAs from EPROMs |
| Start Trigger | 06 | Y | Go to trigger run , wait for bx0, may be disabled by Adr 2C[7] |
| Stop Trigger | 07 | Y | Go to stop state, wait for bx0, may be disabled by Adr 2C[7] |
| Test Enable | 08 |  |  |
| Private Gap | 09 |  |  |
| Private Orbit | 0A |  |  |
| Tmb\_hard\_reset (\*) | 10 |  | Reload TMB FPGAs from EPROM |
| Alct\_hard\_reset (\*) | 11 |  | Reload ALCT FPGAs from EPROM |
| Dmb\_hard\_reset (\*) | 12 |  | Reload DMB FPGAs from EPROM |
| Mpc\_hard\_reset (\*) | 13 |  | Reload MPC FPGAs from EPROM |
| Dmb\_cfeb\_calibrate0 (\*) | 14 |  | CFEB Calibrate Pre-Amp Gain |
| Dmb\_cfeb\_calibrate1 (\*) | 15 |  | CFEB Trigger Pattern Calibration |
| Dmb\_cfeb\_calibrate2 (\*) | 16 |  | CFEB Pedestal Calibration |
| Dmb\_cfeb\_initiate (\*) | 17 |  | Initiate CFEB calibration (Hold next L1ACC and Pretriggers) |
| Alct\_adb\_pulse\_sync (\*) | 18 |  | Pulse Anode Discriminator, synchronous |
| Alct\_adb\_pulse\_async (\*) | 19 |  | Pulse Anode Discriminator, asynchronous |
| Clct\_external\_trigger (\*) | 1A |  | External Trigger All CLCTs |
| Alct\_external\_trigger (\*) | 1B |  | External Trigger All ALCTs |
| Soft\_reset (\*) | 1C |  | Initializes the FPGA on DMB, TMB and MPC boards |
| DMB\_soft\_reset (\*) | 1D |  | Initializes the FPGA on a DMB |
| TMB\_soft\_reset (\*) | 1E |  | Initializes the FPGA on a TMB |
| MPC\_soft\_reset (\*) | 1F |  | Initializes the FPGA on a MPC |
| Send\_bcnt[7..0] (\*) | 20 |  | Send Bunch\_Counter[7..0] to ccb\_data[7..0] bus |
| Send\_evcnt[7..0] (\*) | 21 |  | Send Event\_Counter[7..0] to ccb\_data[7..0] bus |
| Send\_evcnt[15..8] (\*) | 22 |  | Send Event\_Counter[15..8] to ccb\_data[7..0] bus |
| Send\_evcnt[23..16] (\*) | 23 |  | Send Event\_Counter[23..16] to ccb\_data[7..0] bus |
| Inject patterns from TMBs | 24 | Y | Injects patterns from TMB’s internal RAM to MPC |
| Alct\_adb\_pulse (\*) | 25 |  | Generate sync and async anode discriminator pulses |
| Inject patterns from MPCs | 30 |  | Injects patterns from MPC’s input FIFO to SP |
| Inject patterns from MS | 31 |  | Injects patterns from MS input FIFO to Global Muon Trigger |
| tmb\_bxreset | 32 | Y | Reset TMB/ALCT BXN, do not reset L1A counters |

(\*) – decoded by CCB

TMB Board Status Operations

ID Registers

id\_slot=15 VME Slot

id\_rev =D Firmware version

id\_type=C Firmware Type

id\_date=06/08/2004 Firmware Compile Date

id\_rev =38CA=06/10/04 xc2v3000 Firmware Revcode

Digital Serial Numbers

Digital Serial for TMB CRC=DC DSN=00000A237E7F MFG=01 OK

Digital Serial for Mez CRC=BF DSN=000007E06194 MFG=01 OK

Digital Serial for RAT CRC=52 DSN=00000AB39AAD MFG=01 OK

Power Supply ADC

TMB2005E Comparators

5.0V status=OK

3.3V status=OK

1.8V status=OK

1.5V status=OK

Tcrit status=OK

TMB2005E ADC

+5.0 TMB 5.004 V 0.305 A

+3.3 TMB 3.221 V 1.160 A

+1.5 TMBcore 1.488 V 0.795 A

+1.5 GTLtt 1.492 V 0.230 A

+1.0 GTLref 1.004 V 0.000 A

+3.3 RAT 3.221 V 0.250 A

+1.8 RATcore 1.797 V 8.985 A

+vref/2 2.047 V 0.000 A

+vzero 0.000 V 0.000 A

+vref 4.095 V 0.000 A

TMB2005E Temperature IC

T tmb pcb 73.4 F 23. C Tcrit=261./127.

T tmb fpga 95.0 F 35. C Tcrit=261./127.

RAT2005E Temperature IC

T rat pcb 68.0 F 20. C Tcrit=261./127.

T rat xstr 69.8 F 21. C Tcrit=261./127.

Clock Delays

Current 3D3444 Delay Settings 02/27/2006

Ch0 8steps 16ns ALCT tx clock alct\_tof\_delay in muonic firmware versions

Ch1 1steps 2ns ALCT rx clock not used in muonic firmware versions

Ch2 2steps 4ns DMB tx clock

Ch3 9steps 20ns RPC tx clock

Ch4 0steps 0ns TMB1 rx clock not used in muonic firmware versions

Ch5 0steps 0ns MPC rx clock

Ch6 0steps 0ns DCC tx clock cfeb\_tof\_delay in muonic firmware versions

Ch7 7steps 14ns CFEB0 tx clock

Ch8 7steps 14ns CFEB1 tx clock

Ch9 7steps 14ns CFEB2 tx clock

ChA 7steps 14ns CFEB3 tx clock

ChB 7steps 14ns CFEB4 tx clock

JTAG Chains

Chain Select Address (X=don’t care)

3210 Base Function

00SS 0 ALCT: SS=00(Slow user) SS=01(Slow prom) SS=10(Mez user) SS=11(Mez prom)

01XX 4 TMB Mezzanine FPGA+PROMs

10XX 8 TMB User PROMs

1100 C FPGA Monitor (for TMB self-test)

1101 D RAT Module FPGA+PROM

RAT Module Status Register USER1

RAT FPGA device 0 Idcode= 20A10093

RAT PROM device 1 Idcode= 05024093

RAT FPGA device 0 USERcode=02232006

RAT PROM device 1 USERcode=02232006

RAT USER1=E00000007FFFFFFFFE02300336205650565E400CCC989C20060223EB

rs\_begin B

rs\_version E

rs\_monthday 0223

rs\_year 2006

rs\_syncmode 0

rs\_posneg 0

rs\_loop 1

rs\_rpc\_en 3

rs\_clk\_active 0

rs\_locked\_tmb 1

rs\_locked\_rpc0 0

rs\_locked\_rpc1 0

rs\_locklost\_tmb 0

rs\_locklost\_rpc0 1

rs\_locklost\_rpc1 1

rs\_txok 0

rs\_rxok 0

rs\_ntcrit 1

rs\_rpc\_free 0

rs\_dsn 0

rs\_dddoe\_wr 3

rs\_ddd\_wr 0033

rs\_ddd\_auto 1

rs\_ddd\_start 0

rs\_ddd\_busy 0

rs\_ddd\_verify\_ok 1

rs\_rpc0\_parity\_ok 1

rs\_rpc1\_parity\_ok 1

rs\_rpc0\_cnt\_perr 0565

rs\_rpc1\_cnt\_perr 0565

rs\_last\_opcode 02

rw\_rpc\_en 3

rw\_ddd\_start 0

rw\_ddd\_wr 0033

rw\_dddoe\_wr 3

rw\_perr\_reset 0

rw\_parity\_odd 1

rw\_perr\_ignore 0

rw\_rpc\_future 00

rs\_rpc0\_pdata 7FFFF

rs\_rpc1\_pdata 7FFFF

rs\_unused 0000000

rs\_end E

RAT Module Control Register USER2

RAT USER2=0118019B

ws\_rpc\_en 3

ws\_ddd\_start 0

ws\_ddd\_wr 0033

ws\_dddoe\_wr 3

ws\_perr\_reset 0

ws\_parity\_odd 1

ws\_perr\_ignore 0

ws\_rpc\_future 00

User PROM Programming

Introduction

TMB has two on-board erasable PROMs that contain non-volatile data for modifying VME registers and for initializing JTAG chains. The PROMs are read automatically by firmware state machines after power-up or hard-reset.

Both PROMs are Xilinx XC18V256 devices, which have a capacity of 256K bits stored 1-byte wide in 32K addresses. Some late-production TMBs may have one or two XC18V512 devices, because the 256K product was discontinued by the manufacturer.

PROM contents are programmed and verified either via the front-panel JTAG connector or from the VME backplane using TMBs boot register. The data may be read out 8-wide though TMBs PROM-port register ADR\_PROM (12h) or it may be read 1-bit serial via JTAG.

Register Initialization

TDI TDO

PROM 0

VME

Data

TDI

TDI TDO

PROM 1

JTAG

Data

TDO

JTAG Chain

ID=8h

Mezzanine

FPGA

Shared 8-bit bus

Increment Address

Initialization after power-up or hard reset proceeds as follows:

1. FPGA loads its firmware from mezzanine PROMs (100msec)
2. Delay Locked Loops (DLLs) acquire lock on the 40MHz TTC clock (lock time not yet tested)
3. VME registers load their default values (100ns)
4. The VMEsm state machine reads PROM 0 and writes any new data to the specified VME registers.
5. JTAGsm state machine reads PROM 1 and write JTAG data to the specified chains.

VME PROM-0

After TMB loads default values into its VME registers, the VMEsm state machine reads PROM 0 and updates the specified VME registers with PROM data. The PROM contains a 16-word header, followed by an arbitrary number of 24-bit VME-addresses and their associated 16-bit data word, then followed by a 3-byte trailer sequence that contains the checksum and end-of-PROM marker.

The VMEsm state machine expects PROM-0 data to be organized in a specific format and it may either terminate the read-process or indicate an error condition if the format is incorrect. If the BCh header-begin marker is missing, the state machine terminates reading immediately.

The 16-byte header consists of the BC “begin CLCT data” marker, a 2-byte word count, and the EC end marker. There are no restrictions on the values of the other 12 header bytes. VMEsm assembles the two word-count bytes into a 16-bit number that it uses to recognize when to stop reading the PROM.

The word-count includes every PROM address between the BC and FF markers, inclusive. If there are n VME addresses to be written, the word count would be 16 header + 5n vme data + 3 trailer =1910 +5n. A counter in ADR\_VMESM3 records the number of VME addresses what were actually written. A value of 55Aah should be written to VME address ADR\_VMESM4 to test the PROM-to-FPGA data path.

VME PROM-0 data format:

Adr 7654 3210 Hex Description

--- ---- ---- -- -----------

0 1011 1100 BC Begin CLCT Header Marker, if missing state machine stops

1 tttt oooo LL Word count [7:0] kkkk hhhh tttt oooo from BC to FF

2 kkkk hhhh HH Word count [15:8]

3 tttt oooo 12 Month (month/day in “hex-ascii” December 31, 2006)

4 tttt oooo 31 Day

5 tttt oooo 06 Year 2006 = kkkk hhhh tttt oooo

6 kkkk hhhh 20 Year

7 vvvv vvvv XX Version number = vvvv vvvv

8 xxxx xxxx AA Option (suggest AA to test even bits)

9 xxxx xxxx 55 Option (suggest 55 to test odd bits)

A xxxx xxxx XX Option

B xxxx xxxx XX Option

C xxxx xxxx XX Option

D xxxx xxxx XX Option

E xxxx xxxx XX Option

F 1110 1100 EC End Header Marker

10 aaaa aaaa LL VME adr[7:0] This 5-byte structure is repeated

11 aaaa aaaa MM VME adr[15:8] for every VME address that is

12 aaaa aaaa HH VME adr[23:16] to be modified

13 dddd dddd LL VME data[7:0]

14 dddd dddd HH VME data[15:8]

L-2 1111 1100 FC End of CLCT VME data Marker

L-1 cccc cccc cc Check sum [7:0] includes addresses 0 to L-2

L 1111 1111 FF End of PROM data Marker

If VMEsm detects an error condition, status information can be read from VME address

ADR\_VMESM2 (0xDE):

fmt\_err[0] = Missing BC header-begin marker

fmt\_err[1] = Missing EC header-end marker

fmt\_err[2] = Missing FC data-end marker

fmt\_err[3] = Missing FF prom-end marker

fmt\_err[4] = Word counter overflow

JTAG PROM-1

After the VMEsm state machine completes successful, the JTAGsm machine is started. It reads PROM-1 and writes to the JTAG chains specified by the PROM data. The PROM contains a 16-word header, followed by an arbitrary number of 3-byte Chain Blocks, then followed by a 8-byte trailer sequence that contains the tck-count, word-count, checksum and end-of-PROM marker.

Header

The JTAGsm state machine expects PROM-1 data to be organized in a specific format and it may either terminate the read-process or indicate an error condition if the format is incorrect. If the Bah header-begin marker is missing, the state machine terminates reading immediately.

The 16-byte header consists of the BA “begin ALCT data” marker and the EA end marker. The state machine skips over the next 15 bytes, so are no restrictions on the header contents.

Adr 7654 3210 Hex Description

--- ---- ---- -- -----------

0 10111010 BA Begin ALCT Marker, if “BA” missing state machine stops

1 0000aaaa 03 ALCT MSD 3 Type (288,384,672)

2 0000aaaa 08 ALCT 8

3 0000aaaa 04 ALCT LSD 4

4 0000mmmm 00 Month MSD 0 in “hex-ascii” June 9, 2008

5 0000mmmm 06 Month LSD 6

6 0000dddd 00 Day MSD 0

7 0000dddd 09 Day LSD 9

8 0000yyyy 02 Year MSD 2

9 0000yyyy 00 Year 0

A 0000yyyy 00 Year 0

B 0000yyyy 08 Year LSD 8

C 0000vvvv 01 Version number [3:0]

D 0000xxxx 00 Future use

E 0000xxxx 00 Future use

F 00101010 EA End ALCT Header Marker

Chain Block

A Chain Block marker “Cs” signals the start of a new sequence to generate TCK,TMS, and TDI for a JTAG chain. The “s” in the “Cs” marker is the chain address SEL[3:0]. Normally, TCK will be held high after the last TMS/TDI pair is sent, unless the “C” marker is replaced by a “D” maker. After Cs, there are two more bytes specifying the number of TCK clock pulses to send to the chain.

Following the TCK count are JTAG data bytes that contain packed TMS and TDI bits for up to 4 TCKs. The number of data bytes is tck\_count/4+1.

Chain Block Format [7:0]:

76543210

1100ssss Cs Chain Block begin marker chain address ssss =SEL[3:0]. Cs=hold tck high, Ds= do not

tttttttt ww TCK count [15:8]

tttttttt ww TCK count [7:0]

1sisisisi si JTAG data [7:0], I=TDI bit, s=TMS bit, defined below

4 TCKs packed per byte format, data[7:0]:

Bit Signal

[0] TDI[0]

[1] TMS[0]

[2] TDI[1]

[3] TMS[1]

[4] TDI[2]

[5] TMS[2]

[6] TDI[3]

[7] TMS[3]

SEL[3:0] Selects the active JTAG chain:

SEL[3:0]

Hex 3210 Function

0 0000 ALCT Slow Control FPGA user registers

1 0001 ALCT Slow Control FPGA PROM)

2 0010 ALCT Mezzanine FPGA user registers

3 0011 ALCT Mezzanine FPGA PROMs

4 01XX TMB Mezzanine FPGA+PROMs

8 10XX TMB User PROMs

C 1100 TMB FPGA Monitor (for TMB self-test)

D 1101 RAT Module FPGA+PROM

Chain Block, Continued

The state machine copies the signals TMS, and TDI to the JTAG chain selected by SEL[3:0]. It automatically generates the JTAG clock TCK and also arranges for asserting the next TMS and TDI values while TCK is low.

TMB hardware pulls TCK, TMS, and TDI high for chains that are not currently selected. When changing to a new chain ID, it is recommend that the last PROM word for that chain sets the signals to a logic high.

The number of Chain Blocks is limited only by the memory capacity of the PROM. Each block begins with a Cs marker, and the last block is indicated by an “FA” marker.

Trailer

An 8-byte trailer sequence contains the total-tck-count, PROM word count, data checksum and end-of-PROM marker. The tck-count is the number of TCKs the state machine sent to all chains. The word-count includes every PROM address between the BA and FA markers, inclusive, as well as the 3 TCK-count bytes. Checksum includes every PROM address from the BA marker to the last word-count byte.

Adr 7654 3210 Hex Description

--- ---- ---- -- -----------

T-1 11111010 FC End of JTAG data Marker Also set chain address to C

T+0 tttttttt tt TCK Count Total [17:16] Includes tcks sent for all chain blocks

T+1 tttttttt tt TCK Count Total [15:8]

T+2 tttttttt tt TCK Count Total [7:0]

T+3 wwwwwwww ww Word Count [15:8] Includes Adr 0 and end JTAG marker at T+2

T+4 wwwwwwww ww Word Count [7:0]

T+5 cccccccc cc Check sum [7:0] Includes addresses 0 and T+5

T+6 11111111 FF End of PROM data Marker

If the tck-count, word-count or checksum are incorrect, or if the last-word marker is missing, the state machine indicates the an error by setting jsm\_tck\_fpga\_ok=0.

TCK Throttle

The JTAGsm state machine reads header and trailer bytes from the PROM at 20MHz, then slows to 2.5MHz for processing JTAG data bytes. This results in TCK being pulsed at 10MHz (because there are 4 TCKs per byte, each 50ns high + 50ns low).

If this rate is too high for ALCT JTAG chains, the state machine can be throttled to a lower speed by setting jsm\_throttle[3:0] in ADR\_VMESM0 (D4h). A jsm\_throttle value of 0 corresponds firing TCK at 10MHz full speed. Increasing jsm\_throttle by ‘n’ increases the TCK period by 25ns\*n, and maintains a 50% duty cycle.

State Machine Status

Automatic operation of the state machine can be verified by including TCK writes to chain address C. That chain effectively loops-back TCK, TMS and TDI to the FPGA. If at least 1 TCK transition is seen on chain C, then signal jsm\_tck\_fpga\_ok will be a logic 1 in VME register ADR\_JTAGSM0, and tck\_fpga\_cnt[3:0] in ADR\_JTAGSM2 counts the number of TCKs. Demo software exists that converts old PROM data files to this new format and automatically inserts a C-chain Block if there is not one already.

JTAG PROM-1 data format Example:

Adr 7654 3210 Hex Description

--- ---- ---- -- -----------

0 10111010 BA Begin ALCT Marker, if “BA” missing state machine stops

1 0000aaaa 03 ALCT MSD 3 Type (288,384,672)

2 0000aaaa 08 ALCT 8

3 0000aaaa 04 ALCT LSD 4

4 0000mmmm 00 Month MSD 0 in “hex-ascii” June 9, 2008

5 0000mmmm 06 Month LSD 6

6 0000dddd 00 Day MSD 0

7 0000dddd 09 Day LSD 9

8 0000yyyy 02 Year MSD 2

9 0000yyyy 00 Year 0

A 0000yyyy 00 Year 0

B 0000yyyy 08 Year LSD 8

C 0000vvvv 01 Version number [3:0]

D 0000xxxx 00 Future use

E 0000xxxx 00 Future use

F 00101010 EA End ALCT Header Marker

10 1100ssss C3 Chain Block Markder for chain adr 3 (or Ds to set TCK low)

11 tttttttt ww TCK count [15:8]

12 tttttttt ww TCK count [7:0]

13 sisisisi si JTAG data

14 sisisisi si JTAG data

15 sisisisi si JTAG data

T-1 11111010 FC End of JTAG data Marker

T+0 tttttttt tt TCK Count Total [17:16] Includes tcks sent for all chain blocks

T+1 tttttttt tt TCK Count Total [15:8]

T+2 tttttttt tt TCK Count Total [7:0]

T+3 wwwwwwww ww Word Count [15:8] Includes Adr 0 and end JTAG marker at T+2

T+4 wwwwwwww ww Word Count [7:0]

T+5 cccccccc cc Check sum [7:0] Includes addresses 0 and T+5

T+6 11111111 FF End of PROM data Marker

DMB Readout

Full-Readout and Local-Readout Format (Long Header)

1 DB0C header Beginning Of Cathode Data

7 event header Non-buffered event data

e clct header Cathode LCTs

e tmb header TMB match result

e mpc header MPC frames

e rpc header RPC status

e buf header Buffer status

e 6E0B header End of header block

n hits CFEB0 raw hits

n hits CFEB1 raw hits

n hits CFEB2 raw hits

n hits CFEB3 raw hits

n hits CFEB4 raw hits

1 6B04 Start of RPC raw hits marker (optional)

m hits RPC0 raw hits (optional)

m hits RPC1 raw hits (optional)

1 6E04 End of RPC raw hits marker (optional)

1 6B05 Beginning scope data (optional)

s scope data Scope data (optional)

1 6E05 End of scope data (optional)

1 6B07 Beginning miniscope data (optional)

22 miniscope data Miniscope data 22 words (optional)

1 6E07 End of miniscope data (optional)

1 6BCB Beginning blocked CFEB list (optional)

20 blocked cfebs list Blocked CFEBs list 20 words (optional)

1 6ECB End blocked CFEB list (optional)

1 6E0C End of raw hits

1 2AAA Make word count x4 (inserted only if needed)

1 5555 Make word count x4 (inserted only if needed)

1 DE0F End of Frame

1 Dcrc0 CRC22[10:0]

1 Dcrc1 CRC22[21:11]

1 Dwordcount Total words in transmission (inclusive)

------

Word Count = 42(nheaders)

+ 1(E0B)

+ ncfebs\*(6\*ntbins)

+1(B04) (if RPC readout enabled)

+ nrpcs\*(2\*ntbins) (if RPC readout enabled)

+1(E04) (if RPC readout enabled)

+1(B05) (if Scope readout enabled)

+nch(128)/16\*256 (if Scope readout enabled)

+1(E05) (if Scope readout enabled)

+1(B07) (if miniscope readout enabled)

+22 (if miniscope readout enabled)

+1(E07) (if miniscope readout enabled)

+1(BCB) (if blocked cfebs list readout enabled)

+ncfebs\*4 (if blocked cfebs list readout enabled)

+1(ECB) (if blocked cfebs list readout enabled)

+1(EOC)

+2(2AAA 5555) (if needed to make word count multiple of 4)

+1(E0F)

+2(crc)

+1(wordcount)

Long Header-only Format

1 DB0C header Beginning of Cathode Data

7 event header Non-buffered event data

e clct header Cathode LCTs

e tmb header TMB match result

e mpc header MPC frames

e buf header Buffer status

e rpc header RPC status

1 6E0B End of header block

1 6E0C End of raw hits

1 DE0F End of Frame

1 Dcrc0 CRC22

1 Dcrc1 CRC22

1 Dwordcount Total words in transmission (inclusive)

------

40 words = nheaders(34)+E0B+E0C+2crc+E0F+wdcnt

Short Header-only Format

1 DB0C header Beginning of Cathode Data

7 event header Non-buffered event data

1 DEEF End of Frame

1 Dcrc0 CRC22

1 Dcrc1 CRC22

1 Dframe wordcount Total words in transmission (inclusive)

------

12 words = 8headers+2crc+EEF+wdcnt

Miniscope

TMB contains a smaller version of the main digital scope that is intended to be included in the DMB readout stream by default. The minscope displays a time history of ALCTs, CLCTs, and L1As that helps reproduce TMB behavior offline.

Miniscope data is written continuously to Block RAM, in the same fashion as CFEB raw hits are stored.

When there is a CLCT pre-trigger, miniscope data starts at fifo\_pretrig\_mini time bins before the pre-trigger occurred. If there is no CLCT pre-trigger, mininscope data can still be read out in an L1A-only event, using the L1A look-back mode.

The miniscope is enabled by setting:

0x10C [00] mini\_read\_enable = 1 Turn miniscope on

0x10C [01] mini\_tbins\_test = 1 Turn debug mode off

0x10C [02] mini\_tbins\_word = 1 Insert tbins and pre-trig tbins settings in 1st word

0x10C [07:03] fifo\_tbins\_mini = 22 Number of time bins to read out, must be a multiple of 2, but not of 4

0x10C [12:08] fifo\_pretrig\_mini = 4 Number of time bins before pre-trigger

Once enabled, miniscope data is included in every event readout that contains a full header.

Events the contain miniscope data will have

1. header19[14] mini\_read\_enable = 1 to indicate the event includes miniscope data.
2. 06B07 begin minscope marker in the data stream, located after RPC and main-scope data
3. Typically 22 miniscope time-bin data words
4. 06E07 end miniscope marker

The number of minscope time-bin data words depends on the VME register 0x10C[7:3].

Because the total number of words in the DMB readout is required to be a multiple of 4, and 2 words are used for 06E07|06E07 markers, the number of miniscope time-bin words must be a multiple of 2, but not a multiple of 4.

The first word after the 06B07 marker contains the number of minscope time-bins, which along with the mini\_read\_enable bit in header19[14] allows event-unpacking software to locate the miniscope data markers and predict the total event word count.

Miniscope data is inserted between RPC and Blocked-bits list

Adr= 282 Data= 06E04

Adr= 283 Data= 06B07 🡨 begin miniscope marker

Adr= 284 Data= 00416 🡨 tbin count 0x16 and tbins before pre-trigger 0x04

Adr= 285 Data= 00002 🡨 14 minicope channels at tbin=1

Adr= 286 Data= 00002

Adr= 287 Data= 00002

Adr= 288 Data= 00403

Adr= 289 Data= 01805

Adr= 290 Data= 01009

Adr= 291 Data= 01009

Adr= 292 Data= 02009

Adr= 293 Data= 00009

Adr= 294 Data= 00158

Adr= 295 Data= 00302

Adr= 296 Data= 00102

Adr= 297 Data= 00002

Adr= 298 Data= 00002

Adr= 299 Data= 00002

Adr= 300 Data= 00002

Adr= 301 Data= 00002

Adr= 302 Data= 00002

Adr= 303 Data= 00002

Adr= 304 Data= 00002

Adr= 305 Data= 00002

Adr= 306 Data= 06E07 🡨 end miniscope marker

Adr= 307 Data= 06BCB 🡨 blocked bits marker, if blocked bits are in the readout

Miniscope Channel Assignments:

ch[00] any\_cfeb\_hit At least 1 CFEB meets pre-trigger layer-hit threshold

ch[03:01] clct\_sm\_vec[2:0] CLCT pre-trigger state machine vector

ch[04] clct0\_vpf Valid pattern flag for 1st best CLCT

ch[05] clct1\_vpf Valid pattern flag for 2nd best CLCT

ch[06] alct0\_vpf\_tprt Valid pattern flag for 1st best ALCT, after pipe delay

ch[07] alct1\_vpf\_tprt Valid pattern flag for 2nd best ALCT, after pipe delay

ch[08] clct\_window CLCT match window

ch[09] wr\_push\_rtmb ALCT\*CLCT match signal

ch[10] tmb\_push\_dly L1A signals are l1a\_delay+2bx later

ch[11] l1a\_pulse L1A from CCB

ch[12] l1a\_window\_open L1A window

ch[13] l1a\_push\_me L1A queued for readout signal

ch[14] tmb\_special Always 0 in DMB readout, required by unpacker

ch[15] ddu\_special Always 0 in DMB readout, required by DDU

CLCT Pre-trigger State Machine Vector:

0 s: Startup wait after hard-reset

1 I: Idle, waiting for pre-trigger

2 p: Pre-triggered

3 f: Flushing triad one-shots [checks any\_cfeb\_hit, waits n-bx, returns to idle, n may be 0, n=1 here]

4 t: Trigger-rate throttle [ optional fixed delay before returning to idle]

5 h: Halted

Decoded Readout Example:

000000000000000111111 🡨 Time bins

123456789ABCDEF012345

ch 00 any\_cfeb\_hit \_\_\_------\_\_\_\_\_\_\_\_\_\_\_\_ 🡨 CLCT signals are in pre-trigger time domain

ch 03 clct\_state\_machine 111124444411111111111

ch 03 clct\_state\_machine iiiipfffffiiiiiiiiiii 🡨 CLCT Pre-trigger machine state

ch 04 clct0\_vpf \_\_\_\_\_\_\_\_\_-\_\_\_\_\_\_\_\_\_\_\_

ch 05 clct1\_vpf \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

ch 06 alct0\_vpf \_\_\_\_\_\_\_\_\_-\_\_\_\_\_\_\_\_\_\_\_ 🡨 ALCT arrival is needed to check TMB offline

ch 07 alct1\_vpf \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

ch 08 clct\_window \_\_\_\_\_\_\_\_\_---\_\_\_\_\_\_\_\_\_

ch 09 wr\_push\_rtmb \_\_\_\_\_\_\_\_\_\_-\_\_\_\_\_\_\_\_\_\_ 🡨 ALCT\*CLCT match signal

ch 10 tmb\_push\_dly \_\_\_-\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ 🡨 L1A signals are l1a\_delay+2bx later

ch 11 l1a\_pulse \_\_\_\_-\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ 🡨 L1A from CCB merged with other L1A

ch 12 l1a\_window\_open \_\_\_\_---\_\_\_\_\_\_\_\_\_\_\_\_\_\_

ch 13 l1a\_push\_me \_\_\_\_\_\_\_-\_\_\_\_\_\_\_\_\_\_\_\_\_ 🡨 L1A queued for readout signal

ch 14 tmb\_special \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ 🡨 Unpacker prevents TMB from using 15th bit

ch 15 ddu\_special \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ 🡨 DDU prevents TMB from using 16th bit

Blocked CFEB DiStrips List Format

1 6BCB marker Beginning of blocked cfeb distrip list

1 CFEB0 word 0 [14:12]=cfebid[2:0]=0 [11:0]=cfeb0 distrips[11:0]

1 CFEB0 word 1 [14:12]=cfebid[2:0]=0 [11:0]=cfeb0 distrips[23:12]

1 CFEB0 word 2 [14:12]=cfebid[2:0]=0 [11:0]=cfeb0 distrips[35:24]

1 CFEB0 word 3 [14:12]=cfebid[2:0]=0 [11:0]=cfeb0 distrips[47:36]

1 CFEB1 word 0 [14:12]=cfebid[2:0]=1 [11:0]=cfeb1 distrips[11:0]

1 CFEB1 word 1 [14:12]=cfebid[2:0]=1 [11:0]=cfeb1 distrips[23:12]

1 CFEB1 word 2 [14:12]=cfebid[2:0]=1 [11:0]=cfeb1 distrips[35:24]

1 CFEB1 word 3 [14:12]=cfebid[2:0]=1 [11:0]=cfeb1 distrips[47:36]

1 CFEB2 word 0 [14:12]=cfebid[2:0]=2 [11:0]=cfeb2 distrips[11:0]

1 CFEB2 word 1 [14:12]=cfebid[2:0]=2 [11:0]=cfeb2 distrips[23:12]

1 CFEB2 word 2 [14:12]=cfebid[2:0]=2 [11:0]=cfeb2 distrips[35:24]

1 CFEB2 word 3 [14:12]=cfebid[2:0]=2 [11:0]=cfeb2 distrips[47:36]

1 CFEB3 word 0 [14:12]=cfebid[2:0]=3 [11:0]=cfeb3 distrips[11:0]

1 CFEB3 word 1 [14:12]=cfebid[2:0]=3 [11:0]=cfeb3 distrips[23:12]

1 CFEB3 word 2 [14:12]=cfebid[2:0]=3 [11:0]=cfeb3 distrips[35:24]

1 CFEB3 word 3 [14:12]=cfebid[2:0]=3 [11:0]=cfeb3 distrips[47:36]

1 CFEB4 word 0 [14:12]=cfebid[2:0]=4 [11:0]=cfeb4 distrips[11:0]

1 CFEB4 word 1 [14:12]=cfebid[2:0]=4 [11:0]=cfeb4 distrips[23:12]

1 CFEB4 word 2 [14:12]=cfebid[2:0]=4 [11:0]=cfeb4 distrips[35:24]

1 CFEB4 word 3 [14:12]=cfebid[2:0]=4 [11:0]=cfeb4 distrips[47:36]

1 6ECB marker End of blocked cfeb distrip list

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22 words

Blocked DiStrips list includes:

* DiStrips turned off via VME Hot Channel Mask
* DiStrips turned off via mask\_all applied to the entire CFEB
* DisStrips marked as bad by automatic bad-bits detection

CFEB DiStrip Bit Packing

Each CFEB has 6 layers of 8 DiStrips = 48 bits

block\_distrip\_list[ 7: 0] = Layer0 Ds[7:0]

block\_distrip\_list[15: 8] = Layer1 Ds[7:0]

block\_distrip\_list[23:16] = Layer2 Ds[7:0]

block\_distrip\_list[31:24] = Layer3 Ds[7:0]

block\_distrip\_list[39:32] = Layer4 Ds[7:0]

block\_distrip\_list[47:40] = Layer5 Ds[7:0]

Which are packed into 4 readout words, 12 bits per word = 48 bits

CFEBn word 0 = block\_distrip\_list[11: 0]

CFEBn word 1 = block\_distrip\_list[23:12]

CFEBn word 2 = block\_distrip\_list[35:24]

CFEBn word 3 = block\_distrip\_list[47:36]

Header Word Descriptions

First 4 header words must conform to DDU format specification:

header00\_[11:0] 12’hB0C Beginning of Cathode record marker

header00\_[14:12] 3’b101 DDU code for TMB/ALCT

header00\_[15] 1 DDU special-word flag

header01\_[11:0] pop\_bxn\_counter[11:0] BXN pushed into L1A queue at L1A arrival

header01\_[14:12] 3’b101 DDU code for TMB/ALCT

header01\_[15] 1 DDU special-word flag

header01 notes:

* bxn\_counter contains the value of the 12-bit BXN counter at the time
* L1A arrives, and is typically 128bx later than the pre-trigger BXN (see header08).
* Readouts will always have bxn\_counter, but may or may not have pre-trigger data.

header02\_[11:0] pop\_l1a\_rx\_counter[11:0] L1As received by TMB

header02\_[14:12] 3’b101 DDU code for TMB/ALCT

header02\_[15] 1 DDU special-word flag

header03\_[11:0] readout\_counter[11:0] Counts L1A readouts

header03\_[14:12] 3’b101 DDU code for TMB/ALCT

header03\_[15] 1 DDU special-word flag

Next 4 words for short-header mode or full-header:

header04\_[4:0] board\_id[4:0] TMB module ID number = VME slot number 1-20

header04\_[8:5] csc\_id[3:0] Chamber ID number, set by VME register

header04\_[12:9] run\_id[3:0] Run info, set by VME register

header04\_[13] = buf\_q\_ovf\_err Tried to push new event when queue full

header04\_[14] = r\_sync\_err BXN sync error

header04 notes:

* board\_id defaults to the VME crate slot number, unless overridden via VME
* csc\_id is a user-set value to identify the CSC connected to this TMB
* run\_id is a user-set value to identify the current data run
* buf\_q\_ovf indicates that more L1As arrived than TMB was able to push into its
* readout processing queue. In this case the average trigger rate is probably higher than the
* readout data path can tolerate
* sync\_err indicates that bx0 did not arrive when the BXN counter turned over to the bxn-preset value. Either bx0 is not functioning, or the 40 MHz clock gained or lost counts. A sync\_err is latched-on until ttc\_resync or ttc\_bxreset.

header05\_[5:0] r\_nheaders[5:0] Number of header words

header05\_[8:6] fifo\_mode[2:0] Raw hits fifo readout mode set via VME

header05\_[10:9] r\_type[1:0] Record type: dump, nodump, full header, short header

header05\_[12:11] l1a\_type[1:0] L1A Pop type code: buffers, no buffers, clct/alct\_only

header05\_[13] r\_has\_buf Event has clct and rpc buffer data

header05\_[14] r\_buf\_stalled Buffer write pointer hit a fence and stalled

header05 notes:

1. nheaders indicates the length of the current header block, including the BOC marker to 1 frame before the EOB marker. In current firmware it will be 8 for short headers and 42 for full.
2. FIFO Modes:

mode raw hits header

0 no full (if buffer was available at pre-trigger)

1 all 5 CFEBs full (if buffer was available at pre-trigger)

2 local full (if buffer was available at pre-trigger), local=sparsified cfebs

3 no short

4 no no

1. Record Type Codes:

r-type raw hits header

0 no full

1 full full

2 local full

3 no short (no buffer was available at pre-trigger)

1. L1A Type Codes:

l1a-type

0 Normal CLCT trigger with buffer data and L1A window match

1 ALCT-only trigger, no data buffers (not usually read out)

2 L1A-only, no matching TMB trigger, no buffer data (not usually read out)

3 TMB triggered, no L1A-window match, event has buffer data (not usually read out)

header06\_[14:0] bd\_status[14:0] Board status summary

header06 notes:

bd\_status[ 0] bd\_status\_ok Board all-OK: voltages OK, temperature OK, prom-load OK

bd\_status[ 1] vstat\_5p0v Voltage Comparator +5.0V, 1=OK

bd\_status[ 2] vstat\_3p3v Voltage Comparator +3.3V, 1=OK

bd\_status[ 3] vstat\_1p8v Voltage Comparator +1.8V, 1=OK

bd\_status[ 4] vstat\_1p5v Voltage Comparator +1.5V, 1=OK

bd\_status[ 5] \*t\_crit Temperature ADC Tcritical 1=OK

bd\_status[ 6] vsm\_ok VME Machine ran without errors

bd\_status[ 7] vsm\_aborted VME State machine aborted reading PROM

bd\_status[ 8] vsm\_cksum\_ok VME Check-sum matches PROM contents

bd\_status[ 9] vsm\_wdcnt\_ok VME Word count matches PROM contents

bd\_status[10] jsm\_ok JTAG state machine completed without errors

bd\_status[11] jsm\_aborted JTAG State machine aborted reading PROM

bd\_status[12] jsm\_cksum\_ok JTAG Check-sum matches PROM contents

bd\_status[13] jsm\_wdcnt\_ok JTAG Word count matches PROM contents

bd\_status[14] jsm\_tck\_fpga\_ok FPGA jtag tck detected correctly

header07\_[14:0] revcode[14:0] Firmware version date code

header07 notes:

revcode[04:00] day 1-31

revcode[08:05] month 1-12

revcode[12:09] years after 2000

revcode[14:13] fpga type, 1 for xc2v3000, 2 for xc2v4000

Full Header-mode words 8-EOB: Event Counters

header08\_[11:0] r\_bxn\_counter\_ff[11:0] CLCT Bunch Crossing number at pre-trigger, 0-3563

header08\_[12] r\_tmb\_clct0\_discard; TMB discarded clct0 from ME1A

header08\_[13] r\_tmb\_clct1\_discard; TMB discarded clct1 from ME1A

header08\_[14] clock\_lock\_lost Main DLL clock lost lock

header09\_[14:0] r\_pretrig\_counter[14:0] Counts CLCT pre-triggers [stops on ovf]

header10\_[14:0] r\_pretrig\_counter[29:15]

header11\_[14:0] r\_clct\_counter[14:0] Counts CLCTs post-drift [stops on ovf]

header12\_[14:0] r\_clct\_counter[29:15]

header13\_[14:0] r\_trig\_counter[14:0] Counts TMB triggers to MPC, L1A request to CCB,

header14\_[14:0] r\_trig\_counter[29:15] [stops on ovf]

header15\_[14:0] r\_alct\_counter[14:0] Counts ALCTs received from ALCT board [stops on ovf]

header16\_[14:0] r\_alct\_counter[29:15]

header17\_[14:0] r\_orbit\_counter[14:0] BX0s since last hard reset [stops on ovf]

header18\_[14:0] r\_orbit\_counter[29:15]

CLCT Raw Hits Size:

header19\_[2:0] r\_ncfebs[2:0] Number of CFEBs read out

header19\_[7:3] r\_fifo\_tbins[4:0] Number of time bins per CFEB in dump

header19\_[12:8] fifo\_pretrig[4:0] Number of time bins before pre-trigger

header19\_[13] scope\_data\_exists Readout includes logic analyzer scope data

header19\_[14] mini\_read\_enable Readout includes miniscope data, 22wds+2markers

CLCT Configuration:

header20\_[2:0] hit\_thresh\_pretrig[2:0] Hits on pattern template pre-trigger threshold

header20\_[6:3] pid\_thresh\_pretrig[3:0] Pattern shape ID pre-trigger threshold

header20\_[9:7] hit\_thresh\_postdrift[2:0] Hits on pattern post-drift threshold

header20\_[13:10] pid\_thresh\_postdrift[3:0] Pattern shape ID post-drift threshold

header20\_[14] stagger\_hs\_csc CSC Staggering ON

header21\_[3:0] triad\_persist[3:0] CLCT Triad persistence

header21\_[6:4] dmb\_thresh\_pretrig[2:0] DMB pre-trigger threshold for active-cfeb list

header21\_[10:7] alct\_delay[3:0] Delay ALCT for CLCT match window

header21\_[14:11] clct\_window[3:0] CLCT match window width

CLCT Trigger Status:

header22\_[8:0] r\_trig\_source\_vec[8:0] Pre-trigger source vector

header22\_[14:9] r\_layers\_hit\_vec[5:0] CSC layers hit on layer trigger

header22 notes:

trig\_source [ 0] CLCT pattern triggered sequencer

trig\_source [ 1] ALCT pattern triggered sequencer

trig\_source [ 2] ALCT\*CLCT pattern triggered sequencer

trig\_source [ 3] ADB external triggered sequencer

trig\_source [ 4] DMB external triggered sequencer

trig\_source [ 5] CLCT (CCB scintillator) external triggered sequencer

trig\_source [ 6] ALCT (CCB) external triggered sequencer

trig\_source [ 7] VME triggered sequencer

trig\_source [ 8] Layer-mode trigger

header23\_[4:0] r\_active\_feb\_mux[4:0] Active CFEB list sent to DMB

header23\_[9:5] r\_cfebs\_read[4:0] CFEBs read out for this event

header23\_[13:10] pop\_l1a\_match\_win[3:0] Position of l1a in window

header23\_[14] active\_feb\_src Active CFEB list source, 0=pretrig, 1=at TMB match

CLCT+ALCT Match Status:

header24\_[0] r\_tmb\_match ALCT and CLCT matched in time, pushed into L1A queue

header24\_[1] r\_tmb\_alct\_only Only ALCT triggered, pushed into L1A queue

header24\_[2] r\_tmb\_clct\_only Only CLCT triggered, pushed into L1A queue

header24\_[6:3] r\_tmb\_match\_win[3:0] Location of alct in clct window, pushed into L1A queue

header24\_[7] r\_no\_alct\_tmb; No ALCT

header24\_[8] r\_one\_alct\_tmb; One ALCT

header24\_[9] r\_one\_clct\_tmb; One CLCT

header24\_[10] r\_two\_alct\_tmb; Two ALCTs

header24\_[11] r\_two\_clct\_tmb; Two CLCTs

header24\_[12] r\_dupe\_alct\_tmb; ALCT0 copied into ALCT1 to make 2nd LCT

header24\_[13] r\_dupe\_clct\_tmb; CLCT0 copied into CLCT1 to make 2nd LCT

header24\_[14] r\_rank\_err\_tmb; LCT1 has higher quality than LCT0, error

CLCT Trigger Data:

header25\_[14:0] r\_clct0\_tmb[14:0] CLCT0 after drift lsbs

header26\_[14:0] r\_clct1\_tmb[14:0] CLCT1 after drift lsbs

header27\_[0] r\_clct0\_tmb[15] CLCT0 after drift msbs

header27\_[1] r\_clct1\_tmb[15] CLCT1 after drift msbs

header27\_[4:2] r\_clctc\_tmb[2:0] CLCT0/1 common after drift msbs

header27\_[5] r\_clct0\_invp CLCT0 had invalid pattern after drift delay

header27\_[6] r\_clct1\_invp CLCT1 had invalid pattern after drift delay

header27\_[7] r\_clct1\_busy 2nd CLCT busy, logic error indicator

header27\_[12:8] perr\_cfeb\_ff[4:0] CFEB raw hits RAM parity error, latched, SEU detection

header27\_[13] 0 perr\_rpc\_ff | perr\_mini\_ff RPC raw hits RAM parity error, latched, SEU detection

header27\_[14] 0 perr\_ff Raw hits RAM parity error summary, latched, SEU

header25-27 notes:

clct0, clct1, clctc packing format:

clct0[0] clct\_1st\_valid Valid pattern flag

clct0[3:1] hs\_hit\_1st[2:0] Hits on pattern 0-6

clct0[7:4] hs\_pid\_1st[3:0] Pattern shape 0-A

clct0[15:8] hs\_key\_1st[7:0] ½-strip ID number

clct1[0] clct\_2nd\_valid Valid pattern flag

clct1[3:1] hs\_hit\_2nd[2:0] Hits on pattern 0-6

clct1[7:4] hs\_pid\_2nd[3:0] Pattern shape 0-A

clct1[15:8] hs\_key\_2nd[7:0] ½-strip ID number

clctc[1:0] bxn\_counter\_ff[1:0] Bunch crossing number at pretrigger, common to clct0/1

clctc[2] sync\_err BX0 disagrees with BXN count, common to clct0/1

ALCT Trigger Data:

header28\_[0] alct\_1st\_valid ALCT0 valid pattern flag

header28\_[2:1] alct\_1st\_quality[1:0] ALCT0 quality

header28\_[3] alct\_1st\_amu ALCT0 accelerator muon flag

header28\_[10:4] alct\_1st\_key[6:0] ALCT0 key wire group

header28\_[14:11] alct\_pretrig\_win[3:0] ALCT active\_feb\_flag position in pretrig window

header29\_[0] alct\_2nd\_valid ALCT1 valid pattern flag

header29\_[2:1] alct\_2nd\_quality[1:0] ALCT1 quality

header29\_[3] alct\_2nd\_amu ALCT1 accelerator muon flag

header29\_[10:4] alct\_2nd\_key[6:0] ALCT1 key wire group

header29\_[12:11] drift\_delay[1:0] CLCT drift delay

header29\_[13] bcb\_read\_enable CFEB blocked DiStrip bits list included in readout

header29\_[14] hs\_layer\_trig Layer-mode trigger

header30\_[4:0] alct\_bxn[4:0] ALCT0/1 bxn

header30\_[6:5] alct\_ecc\_err[1:0] ALCT trigger path ECC error code

header30\_[11:7] cfeb\_badbits\_found[4:0] Bad distrip bits detected in cfeb[n]

header30\_[12] cfeb\_badbits\_blocked At least one CFEB has a bad bit that was blocked

header30\_[13] alct\_cfg\_done ALCT FPGA configuration done

header30\_[14] bx0\_match alct\_bx0==clct\_bx0, latched at clct\_bx0 time

MPC Frames:

header31\_[14:0] r\_mpc0\_frame0\_ff[14:0] MPC muon 0 frame 0 LSBs

header32\_[14:0] r\_mpc0\_frame1\_ff[14:0] MPC muon 0 frame 1 LSBs

header33\_[14:0] r\_mpc1\_frame0\_ff[14:0] MPC muon 1 frame 0 LSBs

header34\_[14:0] r\_mpc1\_frame1\_ff[14:0] MPC muon 1 frame 1 LSBs

header35\_[0] = r\_mpc0\_frame0\_ff[15] MPC muon 0 frame 0 MSB

header35\_[1] = r\_mpc0\_frame1\_ff[15] MPC muon 0 frame 1 MSB

header35\_[2] = r\_mpc1\_frame0\_ff[15] MPC muon 1 frame 0 MSB

header35\_[3] = r\_mpc1\_frame1\_ff[15] MPC muon 1 frame 1 MSB

header35\_[7:4] mpc\_tx\_delay[3:0] MPC transmit delay

header35\_[9:8] r\_mpc\_accept[1:0] MPC muon accept response

header35\_[14:10] cfeb\_en[4:0] CFEBs enabled for triggering (didn’t fit elsewhere)

header31-35 notes:

MPCframe packing format:

mpc0\_frame0[6:0] = alct0\_key[6:0];

mpc0\_frame0[10:7] = clct0\_pat[3:0];

mpc0\_frame0[14:11] = lct0\_quality[3:0];

mpc0\_frame0[15] = lct0\_vpf;

mpc0\_frame1[7:0] = {clct0\_cfeb[2:0],clct0\_key[4:0]};

mpc0\_frame1[8] = clct0\_bend;

mpc0\_frame1[9] = clct\_sync\_err & tmb\_sync\_err\_en[0];

mpc0\_frame1[10] = alct0\_bxn[0];

mpc0\_frame1[11] = clct\_bx0; // bx0 gets replaced after mpc\_tx\_delay, keep here to mollify xst

mpc0\_frame1[15:12] = csc\_id[3:0];

mpc1\_frame0[6:0] = alct1\_key[6:0];

mpc1\_frame0[10:7] = clct1\_pat[3:0];

mpc1\_frame0[14:11] = lct1\_quality[3:0];

mpc1\_frame0[15] = lct1\_vpf;

mpc1\_frame1[7:0] = {clct1\_cfeb[2:0],clct1\_key[4:0]};

mpc1\_frame1[8] = clct1\_bend;

mpc1\_frame1[9] = clct\_sync\_err & tmb\_sync\_err\_en[1];

mpc1\_frame1[10] = alct1\_bxn[0];

mpc1\_frame1[11] = alct\_bx0; // bx0 gets replaced after mpc\_tx\_delay, keep here to mollify xst

mpc1\_frame1[15:12] = csc\_id[3:0];

RPC Configuration:

header36\_[1:0] rd\_list\_rpc[1:0] RPCs included in read out

header36\_[3:2] r\_nrpcs\_read[1:0] Number of RPCs in readout, 0,1,2, 0 if header-only

header36\_[4] = rpc\_read\_enable RPC readout enabled

header36\_[9:5] fifo\_tbins\_rpc[4:0] Number RPC FIFO time bins to read out

header36\_[14:10] fifo\_pretrig\_rpc[4:0] Number RPC FIFO time bins before pretrigger

Buffer Status:

header37\_[10:0] r\_wr\_buf\_adr[10:0] Buffer RAM write address at pretrigger

header37\_[11] r\_wr\_buf\_ready Write buffer was ready at pretrig

header37\_[12] wr\_buf\_ready Write buffer ready now

header37\_[13] buf\_q\_full All raw hits ram in use, ram writing must stop

header37\_[14] buf\_q\_empty No fences remain on buffer stack

header38\_[10:0] r\_buf\_fence\_dist[10:0] Distance to 1st fence address at pretrigger

header38\_[11] buf\_q\_ovf\_err Tried to push when stack full

header38\_[12] buf\_q\_udf\_err Tried to pop when stack empty

header38\_[13] buf\_q\_adr\_err Fence adr popped from stack doesn’t match rls adr

header38\_[14] buf\_stalled\_once Buffer stalled at least once since last resync

header39\_[11:0] buf\_fence\_cnt[11:0] Number of fences in fence RAM currently

header39\_[12] reverse\_hs\_csc 1=Reverse staggered CSC, non-me1

header39\_[13] reverse\_hs\_me1a 1=ME1A hstrip order reversed

header39\_[14] reverse\_hs\_me1b 1=ME1B hstrip order reversed

header40\_[1:0] active\_feb\_mux[6:5]; Extend Hdr23[4:0] Active CFEB list sent to DMB

header40\_[3:2] r\_cfebs\_read[6:5]; Extend Hdr23[9:5] CFEBs read out for this event

header40\_[5:4] perr\_cfeb\_ff[6:5]; Extend Hdr27[12:8] CFEB RAM parity error, latched

header40\_[7:6] cfeb\_badbits\_found[6:5]; Extend Hdr30[11:7] CFEB[n] has at least 1 bad bit

header40\_[9:8] cfeb\_en[6:5]; Extend Hdr35[14:10] CFEBs enabled for triggering

header40\_[10] buf\_fence\_cnt\_is\_peak; Current fence is peak number of fences in RAM

header40\_[11] (MXCFEB==7); TMB has 7 DCFEBs so hdr40\_[10:0] are active

header40\_[13:12] r\_trig\_source\_vec[10:9] Pre-trigger source vector for ME1A/B

header40\_[14] r\_tmb\_trig\_pulse TMB trig\_pulse signal matched rtmb\_push

Spare Frame:

header41\_[0] tmb\_allow\_alct Allow ALCT-only tmb-matching

header41\_[1] tmb\_allow\_clct Allow CLCT-only tmb-matching

header41\_[2] tmb\_allow\_match Allow Match-only tmb-matching

header41\_[3] tmb\_allow\_alct\_ro Allow ALCT-only tmb-matching, non-trigger readout

header41\_[4] tmb\_allow\_clct\_ro Allow CLCT-only tmb-matching, non-trigger readout

header41\_[5] tmb\_allow\_match\_ro Allow Match-only tmb-matching, non-trigger readout

header41\_[6] r\_tmb\_alct\_only\_ro Only ALCT trig, pushed into L1A queue, non-triggering

header41\_[7] r\_tmb\_clct\_only\_ro Only CLCT trig, pushed into L1A queue, non-triggering

header41\_[8] r\_tmb\_match\_ro ALCT\*CLCT match, pushed into L1A queue, non-triggering

header41\_[9] r\_tmb\_trig\_keep This is a triggering readout event

header41\_[10] r\_tmb\_non\_trig\_keep This is a non-triggering readout event

header41\_[13:11] lyr\_thresh\_pretrig[2:0] Layer pre-trigger threshold

header41\_[14] layer\_trig\_en Layer-trigger mode enabled

TMB Data Format: Short Header Mode

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| FIFO Control | | | | DDU | TMB Data [14:0] | | | | | | | | | | | | | | | | |
| Frame  # | /write  fifo | DAV  Data  Available | last  word | d15  DDU  special | d14 | | d13 | d12 | d11 | d10 | d9 | | d8 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 |
| No  Write | **1** | **1** | 0 | 0 |  | |  |  |  |  |  | |  |  |  |  |  |  |  |  |  |
| 0 | 0 | 0 | 0 | **1** | DDU Code 1012 | | | | B0C16 | | | | | | | | | | | | |
| 1 | 0 | 0 | 0 | **1** | DDU Code 1012 | | | | BXN Counter at L1A arrival [11:0] | | | | | | | | | | | | |
| 2 | 0 | 0 | 0 | **1** | DDU Code 1012 | | | | L1A Rx Counter [11:0] | | | | | | | | | | | | |
| 3 | 0 | 0 | 0 | **1** | DDU Code 1012 | | | | Readout Counter[11:0] | | | | | | | | | | | | |
| 4 | 0 | 0 | 0 | 0 | sync  err | buf\_q  ovf | | run\_id[3:0] | | | | csc\_id[3:0] | | | | | board\_id[4:0] | | | | |
| 5 | 0 | 0 | 0 | 0 | buf  stalled | has  buf | | l1a\_type[1:0] | | rec\_type[1:0] | | fifo\_mode[2:0] | | | | nheader\_words[5:0] | | | | | |
| 6 | 0 | 0 | 0 | 0 | board\_status[14:0] | | | | | | | | | | | | | | | | |
| 7 | 0 | 0 | 0 | 0 | firmware\_revcode[14:0] | | | | | | | | | | | | | | | | |
| 8 | 0 | 0 | 0 | **1** | DDU Code 1012 | | | | EEF16 [11:0] (=E0F for full header events, EEF for short header) | | | | | | | | | | | | |
| 9 | 0 | 0 | 0 | **1** | DDU Code 1012 | | | | 1  TMB | CRC22[10:0] | | | | | | | | | | | |
| 10 | 0 | 0 | 0 | **1** | DDU Code 1012 | | | | 1  TMB | CRC22[21:11] | | | | | | | | | | | |
| 11 | 0 | 0 | **1** | **1** | DDU Code 1012 | | | | 1  TMB | Word Count [10:0] | | | | | | | | | | | |
| No  Write | **1** | 0 | 0 | 0 |  | |  |  |  |  |  | |  |  |  |  |  |  |  |  |  |
| Frame  # | /write  fifo | DAV  Data  Available | last  word | d15 | d14 | | d13 | d12 | d11 | d10 | d9 | | d8 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 |

ALCT Header/Trailer Format:

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| FIFO Control | | | | DDU | ALCT Data [14:0] | | | | | | | | | | | | | | |
| Frame  # | /write  fifo | DAV  Data  Available | last  word | d15  DDU  special | d14 | d13 | d12 | d11 | d10 | d9 | d8 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 |
| No  Write | **1** | **1** | 0 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0 | 0 | 0 | 0 | **1** | DDU Code 1012 | | | B0A16 | | | | | | | | | | | |
| 1 | 0 | 0 | 0 | **1** | DDU Code 1012 | | | BXN Counter at L1A arrival [11:0] | | | | | | | | | | | |
| 2 | 0 | 0 | 0 | **1** | DDU Code 1012 | | | L1A Rx Counter [11:0] | | | | | | | | | | | |
| 3 | 0 | 0 | 0 | **1** | DDU Code 1012 | | | Readout Counter[11:0] | | | | | | | | | | | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| n-3 | 0 | 0 | 0 | **1** | DDU Code 1012 | | | E0D16 [11:0] | | | | | | | | | | | |
| n-2 | 0 | 0 | 0 | **1** | DDU Code 1012 | | | 0  ALCT | CRC22[10:0] | | | | | | | | | | |
| n-1 | 0 | 0 | 0 | **1** | DDU Code 1012 | | | 0  ALCT | CRC22[21:11] | | | | | | | | | | |
| n | 0 | 0 | **1** | **1** | DDU Code 1012 | | | 0  CRC OK=1 | Word Count [10:0] | | | | | | | | | | |
| No  Write | **1** | 0 | 0 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Frame  # | /write  fifo | DAV  Data  Available | last  word | d15 | d14 | d13 | d12 | d11 | d10 | d9 | d8 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 |

Notes:

[1] CRC OK=1 is inserted by TMB after it calculates the CRC for data received from ALCT, and compares it to the CRC words sent by ALCT

TMB Data Format: Long Header-Only Mode

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| FIFO Control | | | | DDU | TMB Data [14:0] | | | | | | | | | | | | | | | | | | | | | | |
| Frame  # | /write  fifo | DAV  Data  Available | last  word | d15  DDU  special | d14 | d13 | d12 | d11 | d10 | | d9 | d8 | | | d7 | | | | d6 | d5 | d4 | | | d3 | d2 | d1 | d0 |
| No  Write | **1** | **1** | 0 | 0 |  |  |  |  |  | |  |  | | |  | | | |  |  |  | | |  |  |  |  |
| 0 | 0 | 0 | 0 | **1** | DDU Code 1012 | | | B0C16 | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 0 | **1** | DDU Code 1012 | | | BXN Counter at L1A arrival [11:0] | | | | | | | | | | | | | | | | | | | |
| 2 | 0 | 0 | 0 | **1** | DDU Code 1012 | | | L1A Rx Counter [11:0] | | | | | | | | | | | | | | | | | | | |
| 3 | 0 | 0 | 0 | **1** | DDU Code 1012 | | | Readout Counter[11:0] | | | | | | | | | | | | | | | | | | | |
| 4 | 0 | 0 | 0 | 0 | sync  err | buf\_q  ovf | run\_id[3:0] | | | | | csc\_id[3:0] | | | | | | | | | board\_id[4:0] | | | | | | |
| 5 | 0 | 0 | 0 | 0 | buf  stalled | has  buf | l1a\_type[1:0] | | rec\_type[1:0] | | | fifo\_mode[2:0] | | | | | | | | nheader\_words[5:0] | | | | | | | |
| 6 | 0 | 0 | 0 | 0 | board\_status[14:0] | | | | | | | | | | | | | | | | | | | | | | |
| 7 | 0 | 0 | 0 | 0 | firmware\_revcode[14:0] | | | | | | | | | | | | | | | | | | | | | | |
| 8 | 0 | 0 | 0 | 0 | lock  lost | clct1  discard | clct0  discard | bxn\_counter\_ff[11:0] | | | | | | | | | | | | | | | | | | | |
| 9 | 0 | 0 | 0 | 0 | pretrig\_counter[14:0] | | | | | | | | | | | | | | | | | | | | | | |
| 10 | 0 | 0 | 0 | 0 | pretrig\_counter[29:15] | | | | | | | | | | | | | | | | | | | | | | |
| 11 | 0 | 0 | 0 | 0 | clct\_counter[14:0] | | | | | | | | | | | | | | | | | | | | | | |
| 12 | 0 | 0 | 0 | 0 | clct\_counter[29:15] | | | | | | | | | | | | | | | | | | | | | | |
| 13 | 0 | 0 | 0 | 0 | trig\_counter[14:0] | | | | | | | | | | | | | | | | | | | | | | |
| 14 | 0 | 0 | 0 | 0 | trig\_counter[29:15] | | | | | | | | | | | | | | | | | | | | | | |
| 15 | 0 | 0 | 0 | 0 | alct\_counter[14:0] | | | | | | | | | | | | | | | | | | | | | | |
| 16 | 0 | 0 | 0 | 0 | alct\_counter[29:15] | | | | | | | | | | | | | | | | | | | | | | |
| 17 | 0 | 0 | 0 | 0 | uptime\_counter[14:0] | | | | | | | | | | | | | | | | | | | | | | |
| 18 | 0 | 0 | 0 | 0 | uptime\_counter[29:15] | | | | | | | | | | | | | | | | | | | | | | |
| 19 | 0 | 0 | 0 | 0 | miniscope  read ena | scope  esixts | fifo\_pretrig[4:0] | | | | | | | | fifo\_tbins[4:0] | | | | | | | | | | ncfebs[2:0] | | |
| 20 | 0 | 0 | 0 | 0 | stagger  csc | pid\_thresh\_postdrift[3:0] | | | | | hit\_thresh\_postdrift[2:0] | | | | | | | pid\_thresh\_pretrig[3:0] | | | | | | | hit\_thresh\_pretrig[2:0] | | |
| 21 | 0 | 0 | 0 | 0 | clct\_window[3:0] | | | | alct\_delay[3:0] | | | | | | | | | dmb\_thresh\_pretrig[2:0] | | | | triad\_persist[3:0] | | | | | |
| 22 | 0 | 0 | 0 | 0 | layers\_hit\_vec[5:0] | | | | | | | trig\_source\_vec[8:0] | | | | | | | | | | | | | | | |
| 23 | 0 | 0 | 0 | 0 | aff  source | l1a\_match\_win[3:0] | | | | | cfebs\_read[4:0] | | | | | | | | | | active\_cfeb[4:0] | | | | | | |
| 24 | 0 | 0 | 0 | 0 | lct rank err | dupe clct | dupe alct | two clct | two alct | | one clct | | one alct | | | no alct | | | match\_win[3:0] | | | | | | clct  only | alct  only | tmb  match |
| 25 | 0 | 0 | 0 | 0 | clct0[14:0] | | | | | | | | | | | | | | | | | | | | | | |
| 26 | 0 | 0 | 0 | 0 | clct1[14:0] | | | | | | | | | | | | | | | | | | | | | | |
| 27 | 0 | 0 | 0 | 0 | perr  summary | perr  rpc+mini | parity error cfeb ram[4:0] SEU | | | | | | | | clct1  busy | | | | clct1  invp | clct0  invp | clctc[2:0] | | | | | clct1[15] | clct0[15] |
| 28 | 0 | 0 | 0 | 0 | alct\_pretrig\_win[3:0] | | | | | alct0\_key[6:0] | | | | | | | | | | | alct0 amu | | | | alct0 quality[1:0] | | alct0  valid |
| 29 | 0 | 0 | 0 | 0 | layer  triggerd | bcb  readout | drift\_delay[1:0] | | | alct1\_key[6:0] | | | | | | | | | | | alct1 amu | | | | alct1 quality[1:0] | | alct1  valid |
| 30 | 0 | 0 | 0 | 0 | bx0  match | alct  cfg done | cfeb bits  blocked | cfeb\_badbits\_found[4:0] | | | | | | | | | | | alct\_ecc\_err[1:0] | | alct\_bxn[4:0] | | | | | | |
| 31 | 0 | 0 | 0 | 0 | mpc0\_frame0[14:0] | | | | | | | | | | | | | | | | | | | | | | |
| 32 | 0 | 0 | 0 | 0 | mpc0\_frame1[14:0] | | | | | | | | | | | | | | | | | | | | | | |
| 33 | 0 | 0 | 0 | 0 | mpc1\_frame0[14:0] | | | | | | | | | | | | | | | | | | | | | | |
| 34 | 0 | 0 | 0 | 0 | mpc1\_frame1[14:0] | | | | | | | | | | | | | | | | | | | | | | |
| 35 | 0 | 0 | 0 | 0 | cfeb\_en[4:0] | | | | | | mpc\_accept[1:0] | | | | | | mpc\_tx\_delay[3:0] | | | | | | | mpc1fr1  [15] | mpc1fr0  [15] | mpc0fr1  [15] | mpc0fr0  [15] |
| 36 | 0 | 0 | 0 | 0 | fifo\_pretrig\_rpc[4:0] | | | | | | fifo\_tbins\_rpc[4:0] | | | | | | | | | | rpc  read en | | | nrpcs[1:0] | | rpc\_list[1:0] | |
| 37 | 0 | 0 | 0 | 0 | buf\_q  empty | buf\_q  full | wr\_buf  ready | r\_wr\_buf  ready | r\_wr\_buf\_adr[10:0] | | | | | | | | | | | | | | | | | | |
| 38 | 0 | 0 | 0 | 0 | buf  stalled ff | buf\_q  adr err | buf\_q  udf err | buf\_q  ovf err | r\_buf\_fence\_dist[10:0] | | | | | | | | | | | | | | | | | | |
| 39 | 0 | 0 | 0 | 0 | reverse  me1b | reverse  me1a | reverse  csc | buf\_fence\_cnt[11:0] | | | | | | | | | | | | | | | | | | | |
| 40 | 0 | 0 | 0 | 0 | tmb trig  pulse | trig\_src\_vec[10:9] | | mxcfeb=7 | peak fence | | cfeb\_en[6:5] | | | perr\_cfeb[6:5] | | | | | | cfeb\_badbits\_found[6:5 | | | cfebs\_read[6:5] | | | active\_cfeb[6:5] | |
| 41 | 0 | 0 | 0 | 0 | layer trig  enabled | lyr\_thresh\_pretrig[2:0] | | | non-trig  readout | | triggered  readout | non-trig  match ro | | non-trig  clct ro | | | | | non-trig  alct o | allow  match ro | allow  clct ro | | allow  alct ro | | allow  match | allow  clct | allow  alct |
| 42 | 0 | 0 | 0 | 0 | 6 | | | EOB End Header Block | | | | | | | | | | | | | | | | | | | |
| 43 | 0 | 0 | 0 | 0 | 6 | | | E0C End Cathode Block | | | | | | | | | | | | | | | | | | | |
| 44 | 0 | 0 | 0 | **1** | DDU Code 1012 | | | E0F16 [11:0] | | | | | | | | | | | | | | | | | | | |
| 45 | 0 | 0 | 0 | **1** | DDU Code 1012 | | | 1  TMB | CRC22[10:0] | | | | | | | | | | | | | | | | | | |
| 46 | 0 | 0 | 0 | **1** | DDU Code 1012 | | | 1  TMB | CRC22[21:11] | | | | | | | | | | | | | | | | | | |
| 47 | 0 | 0 | **1** | **1** | DDU Code 1012 | | | 1  TMB | Word Count [10:0] | | | | | | | | | | | | | | | | | | |
| No  Write | **1** | 0 | 0 | 0 |  |  |  |  |  | |  |  | | |  | | | |  |  |  | | |  |  |  |  |
| Frame# | /write  fifo | DAV  Data  Available | last  word | d15 | d14 | d13 | d12 | d11 | d10 | | d9 | d8 | | | d7 | | | | d6 | d5 | d4 | | | d3 | d2 | d1 | d0 |

TMB Data Format: Full-Readout Mode

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| FIFO Control | | | | DDU | TMB Data [14:0] | | | | | | | | | | | | | | | | | | |
| Frame# | /write  fifo | DAV  Data  Available | last  word | d15  DDU  special | d14 | d13 | d12 | | | d11 | d10 | d9 | d8 | d7 | | d6 | d5 | | d4 | d3 | d2 | d1 | d0 |
| No  Write | **1** | **1** | 0 | 0 |  |  |  | | |  |  |  |  |  | |  |  | |  |  |  |  |  |
| 0 | 0 | 0 | 0 | **1** | DDU Code 1012 | | | | | B0C16 | | | | | | | | | | | | | |
| 1 | 0 | 0 | 0 | **1** | DDU Code 1012 | | | | | BXN Counter at L1A arrival [11:0] | | | | | | | | | | | | | |
| 2 | 0 | 0 | 0 | **1** | DDU Code 1012 | | | | | L1A Rx Counter [11:0] | | | | | | | | | | | | | |
| 3 | 0 | 0 | 0 | **1** | DDU Code 1012 | | | | | Readout Counter[11:0] | | | | | | | | | | | | | |
| 4 | 0 | 0 | 0 | 0 | sync  err | buf\_q  ovf | run\_id[3:0] | | | | | | csc\_id[3:0] | | | | | | board\_id[4:0] | | | | |
| 5 | 0 | 0 | 0 | 0 | buf  stalled | has  buf | l1a\_type[1:0] | | | | rec\_type[1:0] | | fifo\_mode[2:0] | | | | nheader\_words[5:0] | | | | | | |
| 6 | 0 | 0 | 0 | 0 | board\_status[14:0] | | | | | | | | | | | | | | | | | | |
| 7 | 0 | 0 | 0 | 0 | firmware\_revcode[14:0] | | | | | | | | | | | | | | | | | | |
| 8 | 0 | 0 | 0 | 0 | lock  lost | clct1  discard | clct0  discard | | bxn\_counter\_ff[11:0] | | | | | | | | | | | | | | |
| 9 | 0 | 0 | 0 | 0 | pretrig\_counter[14:0] | | | | | | | | | | | | | | | | | | |
| 10 | 0 | 0 | 0 | 0 | pretrig\_counter[29:15] | | | | | | | | | | | | | | | | | | |
| 11 | 0 | 0 | 0 | 0 | clct\_counter[14:0] | | | | | | | | | | | | | | | | | | |
| 12 | 0 | 0 | 0 | 0 | clct\_counter[29:15] | | | | | | | | | | | | | | | | | | |
| 13 | 0 | 0 | 0 | 0 | trig\_counter[14:0] | | | | | | | | | | | | | | | | | | |
| 14 | 0 | 0 | 0 | 0 | trig\_counter[29:15] | | | | | | | | | | | | | | | | | | |
| 15 | 0 | 0 | 0 | 0 | alct\_counter[14:0] | | | | | | | | | | | | | | | | | | |
| 16 | 0 | 0 | 0 | 0 | alct\_counter[29:15] | | | | | | | | | | | | | | | | | | |
| 17 | 0 | 0 | 0 | 0 | uptime\_counter[14:0] | | | | | | | | | | | | | | | | | | |
| 18 | 0 | 0 | 0 | 0 | uptime\_counter[29:15] | | | | | | | | | | | | | | | | | | |
| 19 | 0 | 0 | 0 | 0 | miniscoperead ena | scope  esixts | fifo\_pretrig[4:0] | | | | | | | fifo\_tbins[4:0] | | | | | | | ncfebs[2:0] | | |
| 20 | 0 | 0 | 0 | 0 | stagger  csc | pid\_thresh\_postdrift[3:0] | | | | | | hit\_thresh\_postdrift[2:0] | | | pid\_thresh\_pretrig[3:0] | | | | | | hit\_thresh\_pretrig[2:0] | | |
| 21 | 0 | 0 | 0 | 0 | clct\_window[3:0] | | | | | | alct\_delay[3:0] | | | | dmb\_thresh\_pretrig[2:0] | | | | | triad\_persist[3:0] | | | |
| 22 | 0 | 0 | 0 | 0 | layers\_hit\_vec[5:0] | | | | | | | | trig\_source\_vec[8:0] | | | | | | | | | | |
| 23 | 0 | 0 | 0 | 0 | aff  source | l1a\_match\_win[3:0] | | | | | | febs\_read[4:0] | | | | | | | active\_feb[4:0] | | | | |
| 24 | 0 | 0 | 0 | 0 | lct rank err | dupe clct | dupe alct | | | two clct | two alct | one clct | one alct | no alct | | match\_win[3:0] | | | | | clct  only | alct  only | tmb  match |
| 25 | 0 | 0 | 0 | 0 | clct0[14:0] | | | | | | | | | | | | | | | | | | |
| 26 | 0 | 0 | 0 | 0 | clct1[14:0] | | | | | | | | | | | | | | | | | | |
| 27 | 0 | 0 | 0 | 0 | perr  summary | perr  rpc+mini | | parity error cfeb ram[4:0] SEU | | | | | | clct1  busy | | clct1  invp | clct0  invp | | clctc[2:0] | | | clct1[15] | clct0[15] |
| 28 | 0 | 0 | 0 | 0 | alct\_pretrig\_win[3:0] | | | | | | alct0\_key[6:0] | | | | | | | | alct0 amu | | alct0 quality[1:0] | | alct0  valid |
| 29 | 0 | 0 | 0 | 0 | layer  triggerd | bcb  readout | drift\_delay[1:0] | | | | alct1\_key[6:0] | | | | | | | | alct1 amu | | alct1 quality[1:0] | | alct1  valid |
| 30 | 0 | 0 | 0 | 0 | bx0  match | alct  cfg done | cfeb bits  blocked | | | cfeb\_badbits\_found[4:0] | | | | | | alct\_ecc\_err[1:0] | | | alct\_bxn[4:0] | | | | |
| 31 | 0 | 0 | 0 | 0 | mpc0\_frame0[14:0] | | | | | | | | | | | | | | | | | | |
| 32 | 0 | 0 | 0 | 0 | mpc0\_frame1[14:0] | | | | | | | | | | | | | | | | | | |
| 33 | 0 | 0 | 0 | 0 | mpc1\_frame0[14:0] | | | | | | | | | | | | | | | | | | |
| 34 | 0 | 0 | 0 | 0 | mpc1\_frame1[14:0] | | | | | | | | | | | | | | | | | | |
| 35 | 0 | 0 | 0 | 0 | cfeb\_en[4:0] | | | | | | | mpc\_accept[1:0] | | mpc\_tx\_delay[3:0] | | | | | | mpc1fr1  [15] | mpc1fr0  [15] | mpc0fr1  [15] | mpc0fr0  [15] |
| 36 | 0 | 0 | 0 | 0 | fifo\_pretrig\_rpc[4:0] | | | | | | | fifo\_tbins\_rpc[4:0] | | | | | | rpc  read en | | nrpcs[1:0] | | rpc\_list[1:0] | |
| 37 | 0 | 0 | 0 | 0 | buf\_q  empty | buf\_q  full | wr\_buf  ready | | | r\_wr\_buf  ready | r\_wr\_buf\_adr[10:0] | | | | | | | | | | | | |
| 38 | 0 | 0 | 0 | 0 | buf  stalled ff | buf\_q  adr err | buf\_q  udf err | | | buf\_q  ovf err | r\_buf\_fence\_dist[10:0] | | | | | | | | | | | | |
| 39 | 0 | 0 | 0 | 0 | reverse  me1b | reverse  me1a | reverse  csc | | | buf\_fence\_cnt[11:0] | | | | | | | | | | | | | |
| 40 | 0 | 0 | 0 | 0 | tmb trig  pulse | trig\_src\_vec[10:9] | | | | mxcfeb=7 | peak fence | cfeb\_en[6:5] | | perr\_cfeb[6:5] | | | cfeb\_badbits\_found[6:5 | | | cfebs\_read[6:5] | | active\_cfeb[6:5] | |
| 41 | 0 | 0 | 0 | 0 | layer trig  enabled | lyr\_thresh\_pretrig[2:0] | | | | | non-trig  readout | triggered  readout | non-trig  match ro | non-trig  clct ro | | non-trig  alct o | allow  match ro | | allow  clct ro | allow  alct ro | allow  match | allow  clct | allow  alct |
| 42 | 0 | 0 | 0 | 0 | 6 | | | | | EOB End Header Block | | | | | | | | | | | | | |
| 43 |  |  |  |  | CFEB 0 | | | | | Tbin 0 | | | | Ly0[7:0] Triad bits | | | | | | | | | |
| 44 |  |  |  |  | CFEB 0 | | | | | Tbin 0 | | | | Ly1[7:0] | | | | | | | | | |
| 45 |  |  |  |  | CFEB 0 | | | | | Tbin 0 | | | | Ly2[7:0] | | | | | | | | | |
| 46 |  |  |  |  | CFEB 0 | | | | | Tbin 0 | | | | Ly3[7:0] | | | | | | | | | |
| 47 |  |  |  |  | CFEB 0 | | | | | Tbin 0 | | | | Ly4[7:0] | | | | | | | | | |
| 48 |  |  |  |  | CFEB 0 | | | | | Tbin 0 | | | | Ly5[7:0] | | | | | | | | | |
| 49 |  |  |  |  | CFEB 0 | | | | | Tbin 1 | | | | Ly0[7:0] | | | | | | | | | |
| 50 |  |  |  |  | CFEB 0 | | | | | Tbin 1 | | | | Ly1[7:0] | | | | | | | | | |
| 51 |  |  |  |  | CFEB 0 | | | | | Tbin 1 | | | | Ly2[7:0] | | | | | | | | | |
| 52 |  |  |  |  | CFEB 0 | | | | | Tbin 1 | | | | Ly3[7:0] | | | | | | | | | |
| 53 |  |  |  |  | CFEB 0 | | | | | Tbin 1 | | | | Ly4[7:0] | | | | | | | | | |
| 54 |  |  |  |  | CFEB 0 | | | | | Tbin 1 | | | | Ly5[7:0] | | | | | | | | | |
| 55-246 |  |  |  |  | --- | | | | | --- | | | | --- | | | | | | | | | |
| 247 |  |  |  |  | CFEB 4 | | | | | Tbin 6 | | | | Ly0[7:0] | | | | | | | | | |
| 248 |  |  |  |  | CFEB 4 | | | | | Tbin 6 | | | | Ly1[7:0] | | | | | | | | | |
| 249 |  |  |  |  | CFEB 4 | | | | | Tbin 6 | | | | Ly2[7:0] | | | | | | | | | |
| 250 |  |  |  |  | CFEB 4 | | | | | Tbin 6 | | | | Ly3[7:0] | | | | | | | | | |
| 251 |  |  |  |  | CFEB 4 | | | | | Tbin 6 | | | | Ly4[7:0] | | | | | | | | | |
| 252 |  |  |  |  | CFEB 4 | | | | | Tbin 6 | | | | Ly5[7:0] | | | | | | | | | |
| 253 |  |  |  |  | 6 | | | | | B0416 Begin RPC Raw Hits (if RPC readout enabled) | | | | | | | | | | | | | |
| 254 |  |  |  |  | RPC 0 | | | | | Tbin 0 | | | | Pads[7:0] RPC0 Pads | | | | | | | | | |
| 255 |  |  |  |  | RPC 0 | | | | | clct  pretrigger | rpc\_bxn[2:0] | | | Pads[15:8] | | | | | | | | | |
| 256 |  |  |  |  | RPC 0 | | | | | Tbin 1 | | | | Pads[7:0] | | | | | | | | | |
| 257 |  |  |  |  | RPC 0 | | | | | clct  pretrigger | rpc\_bxn[2:0] | | | Pads[15:8] | | | | | | | | | |
| 258 |  |  |  |  | RPC 0 | | | | | Tbin 2 | | | | Pads[7:0] | | | | | | | | | |
| 259 |  |  |  |  | RPC 0 | | | | | clct  pretrigger | rpc\_bxn[2:0] | | | Pads[15:8] | | | | | | | | | |
| 260 |  |  |  |  | RPC 0 | | | | | Tbin 3 | | | | Pads[7:0] | | | | | | | | | |
| 261 |  |  |  |  | RPC 0 | | | | | clct  pretrigger | rpc\_bxn[2:0] | | | Pads[15:8] | | | | | | | | | |
| 262 |  |  |  |  | RPC 0 | | | | | Tbin 4 | | | | Pads[7:0] | | | | | | | | | |
| 263 |  |  |  |  | RPC 0 | | | | | clct  pretrigger | rpc\_bxn[2:0] | | | Pads[15:8] | | | | | | | | | |
| 264 |  |  |  |  | RPC 0 | | | | | Tbin 5 | | | | Pads[7:0] | | | | | | | | | |
| 265 |  |  |  |  | RPC 0 | | | | | clct  pretrigger | rpc\_bxn[2:0] | | | Pads[15:8] | | | | | | | | | |
| 266 |  |  |  |  | RPC 0 | | | | | Tbin 6 | | | | Pads[7:0] | | | | | | | | | |
| 267 |  |  |  |  | RPC 0 | | | | | clct  pretrigger | rpc\_bxn[2:0] | | | Pads[15:8] | | | | | | | | | |
| 268 |  |  |  |  | RPC 1 | | | | | Tbin 0 | | | | Pads[7:0] RPC1 Pads | | | | | | | | | |
| 269 |  |  |  |  | RPC 1 | | | | | clct  pretrigger | rpc\_bxn[2:0] | | | Pads[15:8] | | | | | | | | | |
| 270-279 |  |  |  |  | -- | | | | | -- | | | | -- | | | | | | | | | |
| 280 |  |  |  |  | RPC 1 | | | | | Tbin 6 | | | | Pads[7:0] | | | | | | | | | |
| 281 |  |  |  |  | RPC 1 | | | | | clct  pretrigger | rpc\_bxn[2:0] | | | Pads[15:8] | | | | | | | | | |
| 282 |  |  |  |  | 6 | | | | | E0416 End RPC Raw Hits | | | | | | | | | | | | | |
| 283 |  |  |  |  | 6 | | | | | E0C16 End Cathode Data | | | | | | | | | | | | | |
| opt |  |  |  |  | 2AAA16[14:0] (Optional to make word count multiple of 4) | | | | | | | | | | | | | | | | | | |
| opt |  |  |  |  | 555516[14:0] (Optional to make word count multiple of 4) | | | | | | | | | | | | | | | | | | |
| 284 | 0 | 0 | 0 | **1** | DDU Code 1012 | | | | | E0F16 [11:0] | | | | | | | | | | | | | |
| 285 | 0 | 0 | 0 | **1** | DDU Code 1012 | | | | | 1  TMB | CRC22[10:0] | | | | | | | | | | | | |
| 286 | 0 | 0 | 0 | **1** | DDU Code 1012 | | | | | 1  TMB | CRC22[21:11] | | | | | | | | | | | | |
| 287 | 0 | 0 | **1** | **1** | DDU Code 1012 | | | | | 1  TMB | Word Count [10:0] | | | | | | | | | | | | |
| No  Write | **1** | 0 | 0 | 0 |  |  |  | | |  |  |  |  |  | |  |  | |  |  |  |  |  |

Sample TMB Raw Hits Dump

TMB internal pattern injector + RPC internal pattern injector

7-Time bins, full 5 CLCTs+ 2 RPCs raw hits readout (Blocked CFEB DiStrips list turned off)

Adr= 0 Data=2DB0C

Adr= 1 Data=0DCC8

Adr= 2 Data=0D001

Adr= 3 Data=0D001

Adr= 4 Data=04045

Adr= 5 Data=0226A

Adr= 6 Data=0777F

Adr= 7 Data=0512C

Adr= 8 Data=00C47

Adr= 9 Data=00001

Adr= 10 Data=00000

Adr= 11 Data=00001

Adr= 12 Data=00000

Adr= 13 Data=00001

Adr= 14 Data=00000

Adr= 15 Data=00001

Adr= 16 Data=00000

Adr= 17 Data=002DD

Adr= 18 Data=00000

Adr= 19 Data=0023D

Adr= 20 Data=04204

Adr= 21 Data=01A46

Adr= 22 Data=07E01

Adr= 23 Data=003E1

Adr= 24 Data=00301

Adr= 25 Data=005AD

Adr= 26 Data=00000

Adr= 27 Data=0531C

Adr= 28 Data=010A7

Adr= 29 Data=01000

Adr= 30 Data=00001

Adr= 31 Data=07D0A

Adr= 32 Data=02605

Adr= 33 Data=00000

Adr= 34 Data=00000

Adr= 35 Data=07C01

Adr= 36 Data=008FB

Adr= 37 Data=01E25

Adr= 38 Data=007FF

Adr= 39 Data=00001

Adr= 40 Data=06001

Adr= 41 Data=02326

Adr= 42 Data=06E0B

Adr= 43 Data=00000

Adr= 44 Data=00000

Adr= 45 Data=00000

Adr= 46 Data=00000

Adr= 47 Data=00000

Adr= 48 Data=00000

Adr= 49 Data=00100

Adr= 50 Data=00100

Adr= 51 Data=00100

Adr= 52 Data=00100

Adr= 53 Data=00100

Adr= 54 Data=00100

Adr= 55 Data=00202

Adr= 56 Data=00202

Adr= 57 Data=00202

Adr= 58 Data=00202

Adr= 59 Data=00202

Adr= 60 Data=00202

Adr= 61 Data=00300

Adr= 62 Data=00302

Adr= 63 Data=00300

Adr= 64 Data=00302

Adr= 65 Data=00300

Adr= 66 Data=00302

Adr= 67 Data=00402

Adr= 68 Data=00400

Adr= 69 Data=00402

Adr= 70 Data=00400

Adr= 71 Data=00402

Adr= 72 Data=00400

Adr= 73 Data=00500

Adr= 74 Data=00500

Adr= 75 Data=00500

Adr= 76 Data=00500

Adr= 77 Data=00500

Adr= 78 Data=00500

Adr= 79 Data=00600

Adr= 80 Data=00600

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Adr= 86 Data=01000

Adr= 87 Data=01000

Adr= 88 Data=01000

Adr= 89 Data=01000

Adr= 90 Data=01000

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Adr= 97 Data=01200

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Adr= 103 Data=01300

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Adr= 107 Data=01300

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Adr= 109 Data=01400

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Adr= 165 Data=02600

Adr= 166 Data=02600

Adr= 167 Data=02600

Adr= 168 Data=02600

Adr= 169 Data=03000

Adr= 170 Data=03000

Adr= 171 Data=03000

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Adr= 178 Data=03100

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Adr= 246 Data=04500

Adr= 247 Data=04600

Adr= 248 Data=04600

Adr= 249 Data=04600

Adr= 250 Data=04600

Adr= 251 Data=04600

Adr= 252 Data=04600

Adr= 253 Data=06B04

Adr= 254 Data=00000

Adr= 255 Data=00000

Adr= 256 Data=00100

Adr= 257 Data=00000

Adr= 258 Data=00200

Adr= 259 Data=007AB

Adr= 260 Data=00301

Adr= 261 Data=006AB

Adr= 262 Data=00402

Adr= 263 Data=005AB

Adr= 264 Data=00503

Adr= 265 Data=004AB

Adr= 266 Data=00604

Adr= 267 Data=003AB

Adr= 268 Data=01000

Adr= 269 Data=01000

Adr= 270 Data=01100

Adr= 271 Data=01000

Adr= 272 Data=01200

Adr= 273 Data=017CD

Adr= 274 Data=01301

Adr= 275 Data=016CD

Adr= 276 Data=01402

Adr= 277 Data=015CD

Adr= 278 Data=01503

Adr= 279 Data=014CD

Adr= 280 Data=01604

Adr= 281 Data=013CD

Adr= 282 Data=06E04

Adr= 283 Data=06E0C

Adr= 284 Data=0DE0F

Adr= 285 Data=0D94F

Adr= 286 Data=0DDF2

Adr= 287 Data=1D920

Configuration

Shunt Settings

Table 3: Shunts

|  |  |  |  |
| --- | --- | --- | --- |
| # | Shunt | Default | Function |
| 1 | SH501 [CLK SRC] | 1-2 [CCB] | 1-2 [CCB] CCB sources TMB s 40MHz Main clock  2-3 [XTAL] Onboard crystal sources TMBs 40MHz Main clock |
| 2 | SH502 [CFEB CLK] | **2-3** [DCC] | 1-2 [NRM] CFEB clocks sourced by 3D3444 64/36 duty-cycle  2-3 [DCC] CFEB clocks duty-cycle corrected |
|  | | | |
| 3 | SH55 [GBL] | 1-2 [ENA] | 1-2 [ENA] Boot Register responds to TMB VME Global Address  2-3 [DIS] Boot Register ignores TMB VME Global Address |
| 4 | SH56 [GEO] | 1-2 [ENA] | 1-2 [ENA] Boot Register responds to VME Geographic Address  2-3 [DIS] Boot Register ignores VME Geographic Address |
| 5 | SH57 [ADM] | 1-2 [REQ] | 1-2 [REQ] Boot Register requires VME Address Mode 39h or 3Dh  2-3 [PAS] Boot Register accepts any VME Address Mode |
| 6 | SH97 [FPGA] | 1-2 [ENA] | 1-2 [ENA] Cleared Boot Register enables FPGA VME access  2-3 [DIS] Cleared Boot Register disables FPGA VME access |
|  | | | |
| 7 | SH69-1 [REG IN] | **2-3** [REG] | 1-2 [BPL] Disconnect +3.3V from U69 1.5V regulator input  2-3 [REG] Connect +3.3V to U69 1.5V regulator input |
| 8 | SH69-2 [REG OUT] | **2-3** [REG] | 1-2 [BPL] Backplane sources +1.5Vtt  2-3 [REG] Onboard regulator U69 sources +1.5Vtt |
|  | | | |
| 9 | SH95 [BOOT] | 1-2 [EN] | 1-2 [EN] CCB hard-reset clears Boot Register  2-3 [DIS] CCB hard-reset does not clear Boot Register |
| 10 | SH104 [VME] | 1-2 [EN] | 1-2 [EN] VME write to Boot Register can hard-reset TMB or ALCT  2-3 [DIS] Boot Register can not hard-reset TMB or ALCT |
| 11 | SH105 [CCB] | 1-2 [EN] | 1-2 [EN] CCB can hard-reset TMB or ALCT  2-3 [DIS] CCB can not hard-reset TMB or ALCT |
| 12 | SH106 [ALCT] | 1-2 [EN] | 1-2 [EN] TMB FPGA can hard-reset ALCT board if enabled by Boot  2-3 [DIS] TMB FPGA firmware can not hard-reset ALCT board |
| 13 | SH107 [SELF] | **2-3** [DIS] | 1-2 [EN] TMB FPGA firmware can hard-reset TMB  2-3 [DIS] TMB FPGA firmware can not hard-reset TMB |
|  | | | |
| 14 | SH1081 [ALCT] | 1-2 [EN] | 1-2 [EN] TMB can send hard-reset to ALCT board  2-3 [DIS] TMB can not send hard-reset to ALCT board |
| 15 | SH1082 [TMB] | 1-2 [EN] | 1-2 [EN] TMB can send hard-reset to TMB  2-3 [DIS] TMB can not send hard-reset to TMB |
| 16 | SH1083 [RPC] | 1-2 [EN] | 1-2 [EN] TMB can send hard-reset to RAT/RPC board  2-3 [DIS] TMB can not send hard-reset to RAT/RPC board |
| 17 | SH1084 [PUP] | 1-2 [EN] | 1-2 [EN] Issue hard-reset to TMB on power-up  2-3 [DIS] Do not issue hard-reset to TMB on power-up |
|  | | | |
| 18 | SH62 [VMEADR] | 1-2 [GEO] | 1-2 [GEO] Slot Address derived from VME backplane GEO pins  2-3 [LCL] Slot Address derived from SW2/SW1 hex switches |
| 19 | SH74 [JTAG SRC] | **2-3** [SW3] | 1-2 [XBL] X-blaster board sources JTAG chain address  2-3 [SW3] Onboard SW3 hex switch sources JTAG chain address |
| 20 | SH921 [RAT ADC] | 1-2 [ACORE] | 1-2 [ACORE] ADC Ch9 measures RAT core current  2-3 [+3.3VR] ADC Ch9 measures RAT main +3.3V supply |

Switch Settings

Table 4: Switch Settings

|  |  |  |  |
| --- | --- | --- | --- |
| Switch | Module | Default | Function |
| SW1 | VME | A | SW2/SW1 Form the VME slot address for Local Mode addressing and for the Boot Register Global Address.  Normally, SH62 [VMEADR] will be set to 1-2 [GEO] and the VME Slot-Address is determined by the Slot-ID signals from the VME P1 backplane connector.  SW2/SW1 should be set to 1A [26 decimal] to specify the Boot Register Global Address. SW2 is the most-significant hex digit.  If SH62 [VMEADR] is set 2-3 [LCL], hex rotary switches SW2/SW1 determine the VME slot address for the module, and the P1 Geographic Address signals are ignored. |
| SW2 | VME | 1 |
| SW3 | JTAG | 4 | Selects the JTAG Chain Address for the Xblaster when SH74 [JTAG ADR SRC] is set to 2-3 [SW3]. If SH74 is set 1-2 [XBL], the JTAG Chain Address is determined by the Xblaster.  0000 0 ALCT SLOW USER  0001 1 ALCT SLOW PROM  0010 2 ALCT FPGA USER  0011 3 ALCT FPGA PROMs  01XX 4 TMB FPGA PROMs  10XX 8 TMB User PROMs  1100 C TMB FPGA Loop (for TMB self-test)  1101 D RAT FPGA PROM |

Fuses

Table 5: Fuses for TMB2005

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Fuse | Circuit | Amps | LED | Function | Littelfuse Part # |
| F1 | +5.0V | 5A | D\_F1 Red | VME-bus I/O | 154005.DR |
| F2 | +3.3V | 10A | D\_F2 Red | Main board logic, FPGA IOBs | 154010.DR |
| F3 | +1.5V | 5A | None | GTLP termination | 154005.DR |
| F4 | +3.3VXB | 1A | D\_F4 Grn | Xblaster power | 154001.DR |

Table 6A: Fuses for TMB2013

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Fuse | Circuit | Amps | LED | Function | Littelfuse Part # |
| F1 | +5.0V | 10A | D\_F1 Red | VME-bus I/O | 0451010.MRL |
| F2 | +3.3V | 15A | D\_F2 Red | Main board logic, FPGA IOBs | 0451015.MRL |
| F3 | +1.5V | 10A | None | GTLP termination | 0451010.MRL |
| F4 | +3.3VXB | 1A | D\_F4 Grn | Xblaster power | 154001.DR |

Signal Summary

CCB

* 1 Input LVDS 40MHz clock
* 46 Inputs GTLP at 40MHz
* 46 Outputs GTLP at 40MHz

Table 7: CCB Signal Summary

| Signal | Bits | Dir | Logic | Function |
| --- | --- | --- | --- | --- |
| **Clock Bus** | | | | |
| ccb\_clock40 | 1 | In | LVDS |  |
| Total | 1 |  |  |  |
| **Fast Control Bus** | | | | |
| ccb\_clock40\_enable | 1 | In | GTLP |  |
| ccb\_cmd[5..0] | 6 | In | GTLP |  |
| ccb\_evcntres | 1 | In | GTLP |  |
| ccb\_bcntres | 1 | In | GTLP |  |
| ccb\_cmd\_strobe | 1 | In | GTLP |  |
| ccb\_bx0 | 1 | In | GTLP |  |
| ccb\_l1accept | 1 | In | GTLP |  |
| ccb\_data[7..0] | 8 | In | GTLP |  |
| ccb\_data\_strobe | 1 | In | GTLP |  |
| ccb\_reserved[4..0] | 5 | In | GTLP |  |
| Total | 26 |  |  |  |
| **TMB Reload Bus: ALCT+CLCT+TMB FPGA Reload** | | | | |
| tmb\_hard\_reset | 1 | In | GTLP |  |
| tmb\_cfg\_done[8..0] | 9 | Out | GTLP |  |
| alct\_hard\_reset | 1 | In | GTLP |  |
| alct\_cfg\_done[8..0] | 9 | Out | GTLP |  |
| tmb\_reserved[1..0] | 2 | In | GTLP |  |
| Total | 22 |  |  |  |
| **DAQ Special Purpose Bus [Used by DMB and TMB]** | | | | |
| dmb\_cfeb\_calibrate[2..0] | 3 | In | GTLP |  |
| dmb\_l1a\_release | 1 | (In) | GTLP |  |
| dmb\_reserved\_out[4..0] | 5 | In | GTLP |  |
| dmb\_reserved\_in[2..0] | 3 | (In) | GTLP |  |
| Total | 12 |  |  |  |
| **Trigger Special Purpose Bus [Used by TMB only]** | | | | |
| alct\_adb\_pulse\_sync | 1 | In | GTLP |  |
| alct\_adb\_pulse\_async | 1 | In | GTLP |  |
| clct\_external\_trigger | 1 | In | GTLP |  |
| alct\_external\_trigger | 1 | In | GTLP |  |
| clct\_status[8..0] | 9 | Out | GTLP |  |
| alct\_status[8..0] | 9 | Out | GTLP |  |
| tmb\_l1a\_request | 1 | Out | GTLP |  |
| tmb\_l1a\_release | 1 | Out | GTLP |  |
| tmb\_reserved\_in[4..0] | 5 | Out | GTLP |  |
| tmb\_reserved\_out[2..0] | 3 | In | GTLP |  |
| Total | 32 |  |  |  |

ALCT

* 29 Inputs LVDS Multiplexed at 80 MHz
* 20 Outputs LVDS Multiplexed at 80 MHz
* 1 Output LVDS 40MHz clock

Table 8: ALCT Signal Summary

| Signal | Bits | Pins | Mux | Dir | Logic | Function |
| --- | --- | --- | --- | --- | --- | --- |
| **Inputs** | | | | | | |
| first\_valid | 1 | 0.5 | Yes | In | LVDS | Valid Pattern Flag, best muon |
| first\_quality[1..0] | 2 | 1 | Yes | In | LVDS | Pattern Quality, best muon |
| first\_amu | 1 | 0.5 | Yes | In | LVDS | Accelerator Muon Flag, best muon |
| first\_key[6..0] | 7 | 3.5 | Yes | In | LVDS | Key Wire Group, best muon |
| second\_valid | 1 | 0.5 | Yes | In | LVDS | Valid Pattern Flag, 2nd best muon |
| second\_quality[1..0] | 2 | 1 | Yes | In | LVDS | Pattern Quality, 2nd best muon |
| second\_amu | 1 | 0.5 | Yes | In | LVDS | Accelerator Muon Flag, 2nd best muon |
| second\_key[6..0] | 7 | 3.5 | Yes | In | LVDS | Key Wire Group, 2nd best muon |
| bxn[4..0] | 5 | 2.5 | Yes | In | LVDS | Bunch Crossing Number |
| daq\_data[13..0] | 14 | 7 | Yes | In | LVDS | DAQ data |
| /wr\_fifo | 1 | 0.5 | Yes | In | LVDS | /Write\_enable DAQ FIFO |
| lct\_special | 1 | 0.5 | Yes | In | LVDS | LCT Special Word Flag |
| ddu\_special | 1 | 0.5 | Yes | In | LVDS | DAQ Special Word Flag |
| first\_frame | 1 | 0.5 | Yes | In | LVDS | First DAQ Frame |
| last\_frame | 1 | 0.5 | Yes | In | LVDS | Last DAQ Frame |
| seq\_status[1..0] | 2 | 1 | Yes | In | LVDS | Sequencer Status |
| seu\_status[1..0] | 2 | 1 | Yes | In | LVDS | Radiation SEU Status |
| active\_feb\_flag | 1 | 0.5 | Yes | In | LVDS | Active FEB Flag (ALCT pre-triggered) |
| cfg\_done | 1 | 0.5 | Yes | In | LVDS | FPGA configuration done |
| reserved\_out[3..0] | 4 | 2 | Yes | In | LVDS | Future use |
| tdo | 1 | 1 | No | In | LVDS | JTAG tdo from ALCT |
| Total Inputs | 57 | 29 |  |  |  |  |
| **Outputs** | | | | | | |
| ccb\_brcst[7..0] | 8 | 4 | Yes | Out | LVDS | CCB broadcast command |
| brcst\_str | 1 | 0.5 | Yes | Out | LVDS | ccb\_brcst strobe |
| dout\_str | 1 | 0.5 | Yes | Out | LVDS | ccb\_dout strobe |
| subadr\_str | 1 | 0.5 | Yes | Out | LVDS | ccb\_subaddr strobe |
| bx0 | 1 | 0.5 | Yes | Out | LVDS | Bunch Crossing Zero |
| ext\_inject | 1 | 0.5 | Yes | Out | LVDS | External Test Pattern Inject Command |
| ext\_trig | 1 | 0.5 | Yes | Out | LVDS | External Trigger Command |
| level1\_accept | 1 | 0.5 | Yes | Out | LVDS | Level 1 Accept |
| sync\_adb\_pulse | 1 | 0.5 | Yes | Out | LVDS | Synchronous ADB Test Pulse |
| seq\_cmd[2..0] | 3 | 1.5 | Yes | Out | LVDS | Sequencer Command |
| reserved\_in[4..0] | 5 | 2.5 | Yes | Out | LVDS | Future use |
| clock | 1 | 1 | No | Out | LVDS | 40MHz clock |
| clock\_en | 1 | 1 | No | Out | LVDS | Clock enable |
| hard\_reset | 1 | 1 | No | Out | LVDS | FPGA Reload Command |
| async\_adb\_pulse | 1 | 1 | No | Out | LVDS | Asynchronous ADB Test Pulse |
| jtag\_select[1..0] | 2 | 2 | No | Out | LVDS | JTAG Chain Select |
| tck | 1 | 1 | No | Out | LVDS | JTAG tck to ALCT |
| tms | 1 | 1 | No | Out | LVDS | JTAG tms to ALCT |
| tdi | 1 | 1 | No | Out | LVDS | JTAG tdi to ALCT |
| Total Outputs | 33 | 21 |  |  |  |  |

DMB

* 3 Inputs LVTTL at 40 MHz
* 45 Outputs1 LVTTL at 40 MHz (see note[[1]](#footnote-1) below)
* 47 Outputs2 LVTTL at 40 MHz (see note[[2]](#footnote-2) below)

Table 9: DMB Signal Summary

| Signal | Bits | Dir | Logic | Function |
| --- | --- | --- | --- | --- |
| Outputs | | | | |
| tmb\_data[14:0] | 15 | Out | LVTTL | TMB data[14:0] to DMB FIFO |
| alct\_data[14:0] | 15 | Out | LVTTL | ALCT data [14:0] to DMB FIFO |
| tmb\_ddu\_special | 1 | Out | LVTTL | TMB DDU Special Word Flag |
| tmb\_last\_frame | 1 | Out | LVTTL | TMB Last FIFO frame |
| tmb\_data\_available | 1 | Out | LVTTL | TMB Data Available |
| /tmb\_write\_enable\_fifo | 1 | Out | LVTTL | TMB FIFO /write\_enable |
| tmb\_active\_feb\_flag | 1 | Out | LVTTL | TMB Active Front-End-Board Flag |
| tmb\_active\_feb[4…0] 1 | 5 | Out | LVTTL | TMB Active FEB indicators[4...0] 1 |
| tmb\_active\_feb[6…0] 2 | 7 | Out | LVTTL | TMB Active FEB indicators[6...0] 2 |
| fifo\_clock | 1 | Out | LVTTL | 40MHz FIFO storage clock [= tmb\_clock] |
| alct\_ddu\_special | 1 | Out | LVTTL | ALCT DDU Special Word Flag |
| alct\_last\_frame | 1 | Out | LVTTL | ALCT Last FIFO frame |
| alct\_first\_frame(dav) | 1 | Out | LVTTL | ALCT First FIFO frame, data available |
| /alct\_write\_enable\_fifo | 1 | Out | LVTTL | ALCT FIFO /write\_enable |
| reserved\_to\_dmb | 5 | Out | LVTTL | Unassigned |
| Total Outputs | 57 |  |  |  |
| Inputs |  |  |  |  |
| dmb\_request\_lct | 1 | In | LVTTL | DMB requests active\_feb\_flag from TMB |
| dmb\_ext\_trig | 1 | In | LVTTL | DMB external trigger to TMB |
| dmb\_fpga\_pgm\_done | 1 | In | LVTTL | DMB FPGA Program Done |
| reserved\_from\_dmb | 3 | In | LVTTL | Unassigned |
| Total Inputs | 6 |  |  |  |

CFEB

120 Inputs LVDS data multiplexed at 80 MHz

5 Outputs LVDS 40MHz clock

Table 10: CFEB Signal Summary

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Signal | Bits | Pins | Dir | Logic | Function |
| cfeb0\_ly[5..0]\_tr[7..0] | 48 | 24 | In | LVDS | CFEB0 6 layers x 8 triads, 80MHz |
| cfeb1\_ly[5..0]\_tr[7..0] | 48 | 24 | In | LVDS | CFEB1 6 layers x 8 triads, 80MHz |
| cfeb2\_ly[5..0]\_tr[7..0] | 48 | 24 | In | LVDS | CFEB2 6 layers x 8 triads, 80MHz |
| cfeb3\_ly[5..0]\_tr[7..0] | 48 | 24 | In | LVDS | CFEB3 6 layers x 8 triads, 80MHz |
| cfeb4\_ly[5..0]\_tr[7..0] | 48 | 24 | In | LVDS | CFEB4 6 layers x 8 triads, 80MHz |
| Total Inputs | 240 | 120 |  |  |  |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Signal | Bits | Pins | Dir | Logic | Function |
| cfeb0\_lct\_clock | 1 | 1 | Out | LVDS | CFEB 1 40MHz clock |
| cfeb1\_lct\_clock | 1 | 1 | Out | LVDS | CFEB 2 40MHz clock |
| cfeb2\_lct\_clock | 1 | 1 | Out | LVDS | CFEB 3 40MHz clock |
| cfeb3\_lct\_clock | 1 | 1 | Out | LVDS | CFEB 4 40MHz clock |
| cfeb4\_lct\_clock | 1 | 1 | Out | LVDS | CFEB 5 40MHz clock |
| Total Outputs | 5 | 5 |  |  |  |

MPC

1 Input GTLP at 80MHz

32 Outputs GTLP at 80MHz

Table 11: MPC Signal Summary

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | Signal | Bits | Pins | Dir | Logic | Function |
| First In Time | alct\_first\_key[6:0] | 7 | 3.5 | Out | GTLP | LCT 0 ALCT key wire-group |
| clct\_first\_pat[3:0] | 4 | 2 | Out | GTLP | LCT 0 CLCT pattern number |
|  |  |  |  |  |  |
| lct\_first\_quality[3:0] | 4 | 2 | Out | GTLP | LCT 0 Muon quality |
| first\_vpf | 1 | 0.5 | Out | GTLP | LCT 0 Valid pattern flag |
| alct\_second\_key[6:0] | 7 | 3.5 | Out | GTLP | LCT 1 ALCT key wire-group |
| clct\_second\_pat[3:0] | 4 | 2 | Out | GTLP | LCT 1 CLCT pattern number |
|  |  |  |  |  |  |
| lct\_second\_quality[3:0] | 4 | 2 | Out | GTLP | LCT 1 Muon quality |
| second\_vpf | 1 | 0.5 | Out | GTLP | LCT 1 Valid pattern flag |
|  |  | 0 | 0 |  |  |  |
| Second In Time | clct\_first\_key[7:0] | 8 | 4 | Out | GTLP | LCT 0 CLCT key ½-strip |
| clct\_first\_bend | 1 | 0.5 | Out | GTLP | LCT 0 CLCT bend direction |
| lct 0 sync\_err | 1 | 0.5 | Out | GTLP | LCT 0 BXN does not match at BX0 |
| alct\_first\_bxn[0] | 1 | 0.5 | Out | GTLP | LCT 0 ALCT bunch crossing number |
| clct\_first\_bx0\_local | 1 | 0.5 | Out | GTLP | LCT 0 local BXN from CLCT |
| csc\_id[3:0] | 4 | 2 | Out | GTLP | CSC chamber ID |
| clct\_second\_key[7:0] | 8 | 4 | Out | GTLP | LCT 1 CLCT key ½-strip |
| clct\_second\_bend | 1 | 0.5 | Out | GTLP | LCT 1 CLCT bend direction |
| lct 1 sync\_err | 1 | 0.5 | Out | GTLP | LCT 1 BXN does not match at BX0 |
| alct\_second\_bxn[0] | 1 | 0.5 | Out | GTLP | LCT 1 ALCT bunch crossing number |
| clct\_second\_bx0\_local | 1 | 0.5 | Out | GTLP | LCT 1 local BXN from CLCT |
| csc\_id[3:0] | 4 | 2 | Out | GTLP | CSC chamber ID |
|  | Total Output Signals | 37 | 18.5 |  |  | 2:1 Multiplexing at 80 MHz |
| 1st | lct0\_accept | 1 | 0.5 | In | GTLP | LCT 0 Accepted by MPC best 3 of 18 sort |
| 2nd | lct1\_accept | 1 | 0.5 | In | GTLP | LCT 1 Accepted by MPC best 3 of 18 sort |
|  | Total Input Signals | 76 | 38 |  |  | 2:1 Multiplexing at 80 MHz |

RPC

80 Inputs 40MHz LVTTL [from receivers on transition module]

0 Outputs

Table 12: RPC Signal Summary

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Signal | Bits | Dir | Logic | Function |
| rpc0\_seg[15..0] | 16 | In | LVTTL | RPC Segment[15..0] |
| rpc0\_bxn[2..0] | 3 | In | LVTTL | Bunch Crossing Number [2..0] |
| rpc0\_clock | 1 | In | LVTTL | Clock from RPC Link Board |
| rpc1\_seg[15..0] | 16 | In | LVTTL | RPC Segment[15..0] |
| rpc1\_bxn[2..0] | 3 | In | LVTTL | Bunch Crossing Number [2..0] |
| rpc1\_clock | 1 | In | LVTTL | Clock from RPC Link Board |
| Total data bits | 40 |  |  |  |

VME

24 Inputs TTL Address

16 BiDir TTL Data

Table 13: VME Signal Summary

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Signal | Bits | Dir | Logic | Function |
| address | 24 | In | TTL | VME Address[23..0] |
| data | 16 | BiDir | TTL | VME Data[15..0] |
| control in |  | In | TTL | VME Control Inputs |
| control out |  | Out | TTL | VME Control Outputs |

JTAG

5 Inputs LVDS

1 Outputs LVDS

Table 14: JTAG Signal Summary

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Signal | Bits | Dir | Logic | Function |
| tck | 1 | In | LVDS | JTAG TCK |
| tms | 1 | In | LVDS | JTAG TMS |
| tdi | 1 | In | LVDS | JTAG TDI |
| chain\_select | 2 | In | LVDS | Chain Select Address |
| tdo | 1 | Out | LVDS | JTAG TDO |

LEDs & Testpoints

Table 15: TMB Front Panel LEDs

|  |  |  |
| --- | --- | --- |
| LED Label | Color | Function |
| LCT | Blue | ALCT vpf and CLCT vpf match within the 75ns ALCT window  (see note[[3]](#footnote-3) below) |
| ALCT | Green | ALCT active FEB flag  (may not always be the same as ALCT valid pattern flag) |
| CLCT | Green | CLCT active FEB flag  Or any external trigger except ALCT |
| L1A | Green | Level 1 Accept arrived in L1A window |
| INVP | Yellow | Invalid CLCT pattern after drift delay  Pattern dropped below threshold, probably triggered on noise |
| NMAT | Yellow | ALCT vpf or CLCT vpf arrived but did not match in ALCT window |
| NL1A | Red | No Level 1 Accept arrived in L1A window after TMB triggered  Constant flash rate = buffers full |
| VME | Green | ON = TMB FPGA loaded successfully from PROM  Flashes OFF when module addressed by VME |

Table 12A: Mez-2013 SMT LEDs

|  |  |  |
| --- | --- | --- |
| LED Label | Color | Function |
| D1 | Blue | When lit, indicates at least one fiber link had an error since last reset |
| D2 | Green | When lit, indicates TMB clock0 MMCM has locked since the last reset |
| D3 | Yellow | When lit, indicates TMB clock0 MMCM is not currently locked |
| D4 | Red | When lit, indicates TMB clock0 MMCM lost lock at least once since the last reset |
| D5 | Green | When lit, indicates the QPLL has locked since the last reset |
| D6 | Yellow | When lit, indicates the QPLL is not currently locked |
| D7 | Red | When lit, indicates the QPLL lost lock at least once since the last reset |
| D8 | Green | When lit, indicates at least one fiber link has a stable input |
| D0 | Yellow | When lit, indicated the FPGA is Not Programmed (i.e. DONE is False) |

Table 12B: Mez-2013 Testpoints

|  |  |
| --- | --- |
| Testpoint Label | Function |
| 9 | TRUE indicates at least one fiber link had over 100 errors since the last reset |
| 8 | TRUE indicates all fiber links have a stable input |
| 7:1 | TRUE signas indicate that links 7:1 have a stable input, respectively |

TMB Total I/O Count

Table 16: TMB Total I/O Count

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Bits | Pins | Dir | Logic | Connect To | Function |
| 1 | 2 | In | LVDS | CCB | Clock Bus |
| 26 | 26 | In | GTLP | CCB | Fast Control Bus |
| 4 | 4 | In | GTLP | CCB | TMB Reload Bus |
| 12 | 12 | In | GTLP | CCB + 9 DMB + 9 TMB | DAQ Special Purpose Bus |
| 7 | 7 | In | GTLP | CCB + 9 TMB | Trigger Special Purpose Bus |
| 240 | 120 | In | LVDS | 5 CFEBs | CFEB Comparators |
| 57 | 29 | In | LVDS | ALCT | ALCT Module |
| 6 | 6 | In | LVTTL | 1 DMB | DMB commands |
| 2 | 1 | In | GTLP | MPC | MPC winner |
| 80 | 40 | In | LVTTL | RPC | RPC Inputs |
| 24 | 24 | In | TTL | VME | VME Address |
| 16 | 16 | BiDir | TTL | VME | VME Data |
| 5 | 5 | In | LVTTL | JTAG | JTAG |
| 480 | 292 |  |  |  | Totals |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Bits | Pins | Dir | Logic | Connect To | Function |
| 0 | 0 | Out | LVDS | CCB | Clock Bus |
| 0 | 0 | Out | GTLP | CCB | Fast Control Bus |
| 18 | 18 | Out | GTLP | CCB | TMB Reload Bus |
| 0 | 0 | Out | GTLP | CCB + 9 DMB + 9 TMB | DAQ Special Purpose Bus |
| 25 | 25 | Out | GTLP | CCB + 9 TMB | Trigger Special Purpose Bus |
| 5 | 5 | Out | LVDS | 5 CFEBs | CFEB Comparators |
| 33 | 21 | Out | LVDS | ALCT | ALCT Module |
| 50 | 50 | Out | LVTTL | 1 DMB | DMB data |
| 64 | 32 | Out | GTLP | MPC | MPC winner |
| 0 | 0 | Out | LVTTL | RPC | RPC Inputs |
| 0 | 0 | Out | TTL | VME | VME data is BiDir |
| 1 | 1 | Out | LVTTL | JTAG | JTAG |
| 196 | 152 |  |  |  | Totals |

FPGA I/O Estimate: 392 in – 7 clock + 152 out = 537

# 

Connectors

TMB Connector Summary

Table 17: TMB2005 Connector Summary

|  |  |  |  |
| --- | --- | --- | --- |
| ID | Pins | Type | Function |
| J0 | 50 | SCSI-II | CFEB0 Inputs + Clock Out |
| J1 | 50 | SCSI-II | CFEB1 Inputs + Clock Out |
| J2 | 50 | SCSI-II | CFEB2 Inputs + Clock Out |
| J3 | 50 | SCSI-II | CFEB3 Inputs + Clock Out |
| J4 | 50 | SCSI-II | CFEB4 Inputs + Clock Out |
| J5 | 50 | SCSI-II | ALCT Cable 1 Inputs |
| J6 | 50 | SCSI-II | ALCT Cable 2 I/O |
| J7 | 10 | Header | Xilinx LVDS X-Blaster I/O |
| P1 | 160 | VME64x | VME J1/P1 Bus I/O |
| P2A | 125 | Z-Pack 25x5 | CCB + DMB I/O |
| P2B | 55 | Z-Pack 11x5 | DMB I/O |
| P3A | 55 | Z-Pack 11x5 | MPC I/O |
| P3B | 125 | Z-Pack 25x5 | RPC Inputs + ALCT alternate I/O |
| MTP Rx | - | aqua MTP with reduced flange & SC footprint | 10 Gbps panel-mount adapter to receive up to 12 fiber links carrying DCFEB comparator data to Mez-2013 boards |

J0-J4 CFEB0-CFEB4 Connectors

Function: Receives 80MHz data from CFEBs. Transmits 40MHz clock.

Connector Type: PCB: AMP 787190-5  
Cable: AMP 749111-4  
Shell: AMP 749889-3 [with latches]

Table 18: J0-J4 CFEB0/4-to-TMB Connectors

(This table uses Layer numbers Ly0-to-Ly5, Triad numbers Tr0-to-Tr7)

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Pair | Pin | | Dir | Logic | Multiplexed Signals | |
| 1 | 1+ | 2- | In | LVDS | Ly0Tr0 | Ly3Tr0 |
| 2 | 3+ | 4- | In | LVDS | Ly0Tr2 | Ly3Tr2 |
| 3 | 5+ | 6- | In | LVDS | Ly5Tr0 | Ly4Tr0 |
| 4 | 7+ | 8- | In | LVDS | Ly5Tr2 | Ly4Tr2 |
| 5 | 9+ | 10- | In | LVDS | Ly1Tr0 | Ly2Tr0 |
| 6 | 11+ | 12- | In | LVDS | Ly1Tr2 | Ly2Tr2 |
| 7 | 13+ | 14- | In | LVDS | Ly0Tr4 | Ly3Tr4 |
| 8 | 15+ | 16- | In | LVDS | Ly0Tr6 | Ly3Tr6 |
| 9 | 17+ | 18- | In | LVDS | Ly5Tr4 | Ly4Tr4 |
| 10 | 19+ | 20- | In | LVDS | Ly5Tr6 | Ly4Tr6 |
| 11 | 21+ | 22- | In | LVDS | Ly1Tr4 | Ly2Tr4 |
| 12 | 23+ | 24- | In | LVDS | Ly1Tr6 | Ly2Tr6 |
| 13 | 25+ | 26- | Out | LVDS | LCT\_Clock | |
| 14 | 27+ | 28- | In | LVDS | Ly1Tr7 | Ly2Tr7 |
| 15 | 29+ | 30- | In | LVDS | Ly1Tr5 | Ly2Tr5 |
| 16 | 31+ | 32- | In | LVDS | Ly5Tr7 | Ly4Tr7 |
| 17 | 33+ | 34- | In | LVDS | Ly5Tr5 | Ly4Tr5 |
| 18 | 35+ | 36- | In | LVDS | Ly0Tr7 | Ly3Tr7 |
| 19 | 37+ | 38- | In | LVDS | Ly0Tr5 | Ly3Tr5 |
| 20 | 39+ | 40- | In | LVDS | Ly1Tr3 | Ly2Tr3 |
| 21 | 41+ | 42- | In | LVDS | Ly1Tr1 | Ly2Tr1 |
| 22 | 43+ | 44- | In | LVDS | Ly5Tr3 | Ly4Tr3 |
| 23 | 45+ | 46- | In | LVDS | Ly5Tr1 | Ly4Tr1 |
| 24 | 47+ | 48- | In | LVDS | Ly0Tr3 | Ly3Tr3 |
| 25 | 49+ | 50- | In | LVDS | Ly0Tr1 | Ly3Tr1 |

J5 ALCT Cable1 Connector (Receiver)

Function: Receives 80MHz data from ALCT.

Connector Type: PCB: AMP 787190-5  
Cable: AMP 749111-4  
Shell: AMP 749889-3 [with latches]

Table 19: J5 ALCT Cable1 Connector [J10 on ALCT board]

Modified 4/12/01 to match ALCT2001 PCB. Stinking bad signal inversion = ☹

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Pair | Inverted | Pin | | Dir | Logic | Multiplexed Signals | |
|  |  | + | - |  |  | First in Time | Second in Time |
| 1 | ☹ | 1+ | 2- | In | LVDS | first\_valid | second\_valid |
| 2 |  | 49+ | 50- | In | LVDS | first\_amu | second\_amu |
| 3 | ☹ | 3+ | 4- | In | LVDS | first\_quality0 | second\_quality0 |
| 4 |  | 47+ | 48- | In | LVDS | first\_quality1 | second\_quality1 |
| 5 | ☹ | 5+ | 6- | In | LVDS | first\_key0 | second\_key0 |
| 6 |  | 45+ | 46- | In | LVDS | first\_key1 | second\_key1 |
| 7 | ☹ | 7+ | 8- | In | LVDS | first\_key2 | second\_key2 |
| 8 |  | 43+ | 44- | In | LVDS | first\_key3 | second\_key3 |
| 9 | ☹ | 9+ | 10- | In | LVDS | first\_key4 | second\_key4 |
| 10 |  | 41+ | 42- | In | LVDS | first\_key5 | second\_key5 |
| 11 | ☹ | 11+ | 12- | In | LVDS | first\_key6 | second\_key6 |
| 12 |  | 39+ | 40- | In | LVDS | bxn0 | bxn3 |
| 13 | ☹ | 13+ | 14- | In | LVDS | bxn1 | bxn4 |
| 14 |  | 37+ | 38- | In | LVDS | bxn2 | /wr\_fifo |
| 15 | ☹ | 15+ | 16- | In | LVDS | daq\_data0 | daq\_data7 |
| 16 |  | 35+ | 36- | In | LVDS | daq\_data1 | daq\_data8 |
| 17 | ☹ | 17+ | 18- | In | LVDS | daq\_data2 | daq\_data9 |
| 18 |  | 33+ | 34- | In | LVDS | daq\_data3 | daq\_data10 |
| 19 | ☹ | 19+ | 20- | In | LVDS | daq\_data4 | daq\_data11 |
| 20 |  | 31+ | 32- | In | LVDS | daq\_data5 | daq\_data12 |
| 21 | ☹ | 21+ | 22- | In | LVDS | daq\_data6 | daq\_data13 |
| 22 |  | 29+ | 30- | In | LVDS | lct\_special | first\_frame |
| 23 | ☹ | 23+ | 24- | In | LVDS | parity\_out0 seq\_status0 | parity\_out2 seu\_status0 |
| 24 |  | 27+ | 28- | In | LVDS | parity\_out1 seq\_status1 | parity\_out3 seu\_status1 |
| 25 | ☹ | 25+ | 26- | In | LVDS | ddu\_special | last\_frame |

J6 ALCT Cable2 Connector (Transmitter)

Function: Sends/Receives 80MHz data to/from ALCT.

Connector Type: PCB: AMP 787190-5  
Cable: AMP 749111-4  
Shell: AMP 749889-3 [with latches]

Table 20: J6 ALCT Cable2 Connector [J11 on ALCT board]

Modified 4/12/01 to match ALCT2001 PCB. Stinking bad signal inversion ☹

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Pair | Inverted | Pin | | Dir | Logic | Multiplexed Signals | |
|  |  | + | - |  |  | First in Time | Second in Time |
| 1 |  | 1+ | 2- | Out | LVDS | tdi | |
| 2 | ☹ | 49+ | 50- | Out | LVDS | tms | |
| 3 |  | 3+ | 4- | Out | LVDS | tck | |
| 4 | ☹ | 47+ | 48- | Out | LVDS | jtag\_select0 | |
| 5 |  | 5+ | 6- | Out | LVDS | jtag\_select1 | |
| 6 | ☹ | 45+ | 46- | Out | LVDS | ccb\_brcst0 | ccb\_brcst4 |
| 7 |  | 7+ | 8- | Out | LVDS | ccb\_brcst1 | ccb\_brcst5 |
| 8 | ☹ | 43+ | 44- | Out | LVDS | ccb\_brcst2 | ccb\_brcst6 |
| 9 |  | 9+ | 10- | Out | LVDS | ccb\_brcst3 | ccb\_brcst7 |
| 10 | ☹ | 41+ | 42- | Out | LVDS | brcst\_str1 | subaddr\_str |
| 11 |  | 11+ | 12- | Out | LVDS | dout\_str | bx0 |
| 12 | ☹ | 39+ | 40- | Out | LVDS | ext\_inject | ext\_trig |
| 13 |  | 13+ | 14- | Out | LVDS | level1\_accept | sync\_adb\_pulse |
| 14 | ☹ | 37+ | 38- | Out | LVDS | seq\_cmd0 | seq\_cmd2 |
| 15 |  | 15+ | 16- | Out | LVDS | seq\_cmd1 | seq\_cmd3 reserved\_in4 |
| 16 | ☹ | 35+ | 36- | Out | LVDS | parity\_in0 reserved\_in0[[4]](#footnote-4) | parity\_in2 reserved\_in2 |
| 17 |  | 17+ | 18- | Out | LVDS | parity\_in1 reserved\_in1 | parity\_in3 reserved\_in3 |
| 18 | ☹ | 33+ | 34- | Out | LVDS | async\_adb\_pulse | |
| 19 |  | 19+ | 20- | Out | LVDS | /hard\_reset | |
| 20 | ☹ | 31+ | 32- | Out | LVDS | clock\_en | |
| 21 |  | 21+ | 22- | Out | LVDS | clock | |
| 22 |  | 29+ | 30- | In | LVDS | tdo | |
| 23 | ☹ | 23+ | 24- | In | LVDS | parity\_out4 reserved\_out0 | parity\_out6 reserved\_out2 |
| 24 |  | 27+ | 28- | In | LVDS | parity\_out5 reserved\_out1 | alct\_bx0 reserved\_out3 |
| 25 | ☹ | 25+ | 26- | In | LVDS | active\_feb\_flag | cfg\_done |

J1-J6 SCSI-II 50-Pin Connector Pin Convention

Figure 5: 50-Pin PCB Connector (Female)[[5]](#footnote-5)

(Looking into PCB Connector)   
-------------------------------------   
\ 25 1/  
\ 26 50/   
 ---------------------------------

Figure 6: 50 Pin Cable Connector (Male)

(Looking into Cable Connector)   
-------------------------------------   
\ 1 25/   
\ 50 26/   
 ---------------------------------

Figure 7: 50 Pin PCB Connector Pin Convention

(Looking At Top of PCB)

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | | | |  | | | |
| 1 | • |  |  | 50 | • |  |  |
|  |  | 2 | • |  |  | 49 | • |
| 3 | • |  |  | 48 | • |  |  |
|  |  | 4 | • |  |  | 47 | • |
| 5 | • |  |  | 46 | • |  |  |
| Cable Side |  | 6 | • |  |  | 45 | • |
| 7 | • |  |  | 44 | • |  |  |
|  |  | 8 | • |  |  | 43 | • |
| 9 | • |  |  | 42 | • |  |  |
|  |  | 10 | • |  |  | 41 | • |
| 11 | • |  |  | 40 | • |  |  |
|  |  | 12 | • |  |  | 39 | • |
| 13 | • |  |  | 38 | • |  |  |
|  |  | 14 | • |  |  | 37 | • |
| 15 | • |  |  | 36 | • |  |  |
|  |  | 16 | • |  |  | 35 | • |
| 17 | • |  |  | 34 | • |  |  |
|  |  | 18 | • |  |  | 33 | • |
| 19 | • |  |  | 32 | • |  |  |
|  |  | 20 | • |  |  | 31 | • |
| 21 | • |  |  | 30 | • |  |  |
|  |  | 22 | • |  |  | 29 | • |
| 23 | • |  |  | 28 | • |  |  |
|  |  | 24 | • |  |  | 27 | • |
| 25 | • |  |  | 26 | • |  |  |

J7 Xilinx LVDS Xilinx X-Blaster Connector

Function: Connects TMB2005 to LVDS x-Blaster for programming FPGAs and PROMs.

The LVDS signals and voltage sources on this connector are not directly compatible with the standard Xilinx programming cable.

JTAG chain select signals SEL[3:0] are TTL ☹.

Connector Type: PCB: 3M 3316-5002 16-pin right angle center key Cable: 3M 3452-6600 16-pin center bump

Table 21: J8 Xilinx LVDS X-Blaster Connector

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| +TCK | In | 1 |  | 2 | In | -TCK |
| +TDO | Out | 3 |  | 4 | Out | -TDO |
| +TMS | In | 5 |  | 6 | In | -TMS |
| +3.3V | Out | 7 |  | 8 | - | GND |
| +TDI | In | 9 |  | 10 | In | -TDI |
| +3.3V | In | 11 |  | 12 | In | JTAG\_EN(TTL) |
| SEL0 (TTL) | Out | 13 |  | 14 | In | SEL1 (TTL) |
| SEL2 (TTL) | In | 15 |  | 16 | In | SEL3 (TTL) |

P1 Backplane VME64x J1/P1 Connector

Function: VME interface.

Connector Type: PCB: Harting 02-02-160-2101 Male Right-Angle Backplane: Harting 02-01-160-2201 Female

Address bits: 24

Data bits: 16

Geographic Address bits: 5

Table 22: P1 VME64x Connector

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Pin | Row z | Row a | Row b | Row c | Row d |
| 1 | MPR | D00 | BBSY\* | D08 | VPC |
| 2 | GND | D01 | BCLR\* | D09 | GND |
| 3 | MCLK | D02 | ACFAIL\* | D10 | +V1 |
| 4 | GND | D03 | BG0IN\* | D11 | +V2 |
| 5 | MSD | D04 | BG0OUT\* | D12 | RsvU |
| 6 | GND | D05 | BG1IN\* | D13 | -V1 |
| 7 | MMD | D06 | BG1OUT\* | D14 | -V2 |
| 8 | GND | D07 | BG2IN\* | D15 | RsvU |
| 9 | MCTL | GND | BG2OUT\* | GND | GAP\* |
| 10 | GND | SYSCLK | BG3IN\* | SYSFAIL\* | GA0\* |
| 11 | RESP\* | GND | BG3OUT\* | BERR\* | GA1\* |
| 12 | GND | DS1\* | BR0\* | SYSRESET\* | +3.3V |
| 13 | RsvBus1 | DS0\* | BR1\* | LWORD\* | GA2\* |
| 14 | GND | WRITE\* | BR2\* | AM5 | +3.3V |
| 15 | RsvBus2 | GND | BR3\* | A23 | GA3\* |
| 16 | GND | DTACK\* | AM0 | A22 | +3.3V |
| 17 | RsvBus3 | GND | AM1 | A21 | GA4\* |
| 18 | GND | AS\* | AM2 | A20 | +3.3V |
| 19 | RsvBus4 | GND | AM3 | A19 | RsvBus11 |
| 20 | GND | IACK\* | GND | A18 | +3.3V |
| 21 | RsvBus5 | IACKIN\* | SERCLK | A17 | RsvBus12 |
| 22 | GND | IACKOUT\* | SERDAT | A16 | +3.3V |
| 23 | RsvBus6 | AM4 | GND | A15 | RsvBus13 |
| 24 | GND | A07 | IRQ7\* | A14 | +3.3V |
| 25 | RsvBus7 | A06 | IRQ6\* | A13 | RsvBus14 |
| 26 | GND | A05 | IRQ5\* | A12 | +3.3V |
| 27 | RsvBus8 | A04 | IRQ4\* | A11 | LI/I\* |
| 28 | GND | A03 | IRQ3\* | A10 | +3.3V |
| 29 | RsvBus9 | A02 | IRQ2\* | A09 | LI/O\* |
| 30 | GND | A01 | IRQ1\* | A08 | +3.3V |
| 31 | RsvBus10 | -12V | +5VSTDBY | +12V | GND |
| 32 | GND | +5V | +5V | +5V | VPC |

P2A Backplane CCB+DMB Connector

Function: Sends and receives data to/from CCB, and carries some DMB signals.

Connector Type: PCB: AMP Z-Pack 125 (25 rows of 5 pins) female AMP 100145-1 Backplane: AMP Z-Pack 125 (25 rows of 5 pins) male AMP ?

Table 23: P2A Backplane CCB+DMB Connector

|  |  |  |  |
| --- | --- | --- | --- |
| Pin | Dir | Logic | Signal |
| A1 | In | LVDS | ccb\_clock40+ |
| A2 | In | GTLP | ccb\_clock40\_enable |
| A3 | In | GTLP | ccb\_cmd0 |
| A4 | In | GTLP | ccb\_cmb4 |
| A5 | In | GTLP | ccb\_cmd\_strobe |
| A6 | In | GTLP | ccb\_data0 |
| A7 | In | GTLP | ccb\_data4 |
| A8 | In | GTLP | ccb\_reserved0 |
| A9 | In | GTLP | tmb\_hard\_reset |
| A10 | In | GTLP | alct\_adb\_pulse\_sync |
| A11 | Out | GTLP | clct\_status0 |
| A12 | Out | GTLP | clct\_status4 |
| A13 | Out | GTLP | clct\_status6 |
| A14 | Out | GTLP | alct\_status3 |
| A15 | Out | GTLP | alct\_status7 |
| A16 | Out | GTLP | tmb\_reserved\_in0 |
| A17 | Out | GTLP | tmb\_reserved\_in4 |
| A18 |  |  |  |
| A19 | In | GTLP | dmb\_cfeb\_calibrate0 |
| A20 | In | GTLP | dmb\_reserved\_out0 |
| A21 | In | GTLP | dmb\_reserved\_out4 |
| A22 |  |  |  |
| A23 | Out | LVTTL | tmb\_data0 |
| A24 | Out | LVTTL | tmb\_data4 |
| A25 | Out | LVTTL | tmb\_data8 |

|  |  |  |  |
| --- | --- | --- | --- |
| Pin | Dir | Logic | Signal |
| B1 | In | LVDS | ccb\_clock40- |
| B2 | In | GTLP | ccb\_reserved4 |
| B3 | In | GTLP | ccb\_cmd1 |
| B4 | In | GTLP | ccb\_cmb5 |
| B5 | In | GTLP | ccb\_bx0 |
| B6 | In | GTLP | ccb\_data1 |
| B7 | In | GTLP | ccb\_data5 |
| B8 | In | GTLP | ccb\_reserved1 |
| B9 | In | GTLP | alct\_hard\_reset |
| B10 | In | GTLP | alct\_adb\_pulse\_async |
| B11 | Out | GTLP | clct\_status1 |
| B12 | Out | GTLP | clct\_status5 |
| B13 | Out | GTLP | alct\_status0 |
| B14 | Out | GTLP | alct\_status4 |
| B15 | Out | GTLP | alct\_status8 |
| B16 | Out | GTLP | tmb\_reserved\_in1 |
| B17 | In | GTLP | tmb\_reserved\_out0 |
| B18 |  |  |  |
| B19 | In | GTLP | dmb\_cfeb\_calibrate1 |
| B20 | In | GTLP | dmb\_reserved\_out1 |
| B21 | (In)1 | GTLP | dmb\_reserved\_in0 |
| B22 |  |  |  |
| B23 | Out | LVTTL | tmb\_data1 |
| B24 | Out | LVTTL | tmb\_data5 |
| B25 | Out | LVTTL | tmb\_data9 |

Pins C1 through C25 are connected to Backplane Ground

Notes:

1. TMB can monitor signals to/from DMB, but can not assert them.

P2A Backplane CCB+DMB Connector Continued

Table 20: P2A Backplane CCB Connector Continued

|  |  |  |  |
| --- | --- | --- | --- |
| Pin | Dir | Logic | Signal |
| D1 | Out | GTLP | tmb\_config\_done |
| D2 |  |  |  |
| D3 | In | GTLP | ccb\_cmd2 |
| D4 | In | GTLP | ccb\_evcntres |
| D5 | In | GTLP | ccb\_l1accept |
| D6 | In | GTLP | ccb\_data2 |
| D7 | In | GTLP | ccb\_data6 |
| D8 | In | GTLP | ccb\_reserved2 |
| D9 | In | GTLP | tmb\_reserved0 |
| D10 | In | GTLP | clct\_external\_trigger |
| D11 | Out | GTLP | clct\_status2 |
| D12 | Out | GTLP | clct\_status6 |
| D13 | Out | GTLP | clct\_status1 |
| D14 | Out | GTLP | alct\_status5 |
| D15 | Out | GTLP | tmb\_l1a\_request |
| D16 | Out | GTLP | tmb\_reserved\_in2 |
| D17 | In | GTLP | tmb\_reserved\_out1 |
| D18 |  |  |  |
| D19 | In | GTLP | dmb\_cfeb\_calibrate2 |
| D20 | In | GTLP | dmb\_reserved\_out2 |
| D21 | (In)1 | GTLP | dmb\_reserved\_in1 |
| D22 |  |  |  |
| D23 | Out | LVTTL | tmb\_data2 |
| D24 | Out | LVTTL | tmb\_data7 |
| D25 | Out | LVTTL | tmb\_data11 |

|  |  |  |  |
| --- | --- | --- | --- |
| Pin | Dir | Logic | Signal |
| E1 | Out | GTLP | alct\_config\_done |
| E2 |  |  |  |
| E3 | In | GTLP | ccb\_cmd3 |
| E4 | In | GTLP | ccb\_bcntres |
| E5 | In | GTLP | ccb\_data\_strobe |
| E6 | In | GTLP | ccb\_data3 |
| E7 | In | GTLP | ccb\_data7 |
| E8 | In | GTLP | ccb\_reserved3 |
| E9 | In | GTLP | tmb\_reserved1 |
| E10 | In | GTLP | alct\_external\_trigger |
| E11 | Out | GTLP | clct\_status3 |
| E12 | Out | GTLP | clct\_status7 |
| E13 | Out | GTLP | alct\_status2 |
| E14 | Out | GTLP | alct\_status6 |
| E15 | Out | GTLP | tmb\_l1a\_release |
| E16 | Out | GTLP | tmb\_reserved\_in3 |
| E17 | In | GTLP | tmb\_reserved\_out2 |
| E18 |  |  |  |
| E19 | (In)1 | GTLP | dmb\_l1a\_release |
| E20 | In | GTLP | dmb\_reserved\_out3 |
| E21 | (In)1 | GTLP | dmb\_reserved\_in2 |
| E22 |  |  |  |
| E23 | Out | LVTTL | tmb\_data3 |
| E24 | Out | LVTTL | tmb\_data7 |
| E25 | Out | LVTTL | tmb\_data11 |

Notes:

1) TMB can monitor signals to/from DMB, but can not assert them.

P2B Backplane DMB Connector

Function: Sends and receives data to/from DMB.

Connector Type: PCB: AMP Z-Pack 55 (11 rows of 5 pins) female AMP 100161-1 Backplane: AMP Z-Pack 55 (11 rows of 5 pins) male AMP ?

Table 24: P2B Backplane DMB Connector

|  |  |  |  |
| --- | --- | --- | --- |
| Pin | Dir | Logic | Signal |
| A1 | Out | LVTTL | tmb\_data12 |
| A2 | Out | LVTTL | alct\_data1 |
| A3 | Out | LVTTL | alct\_data5 |
| A4 | Out | LVTTL | alct\_data9 |
| A5 | Out | LVTTL | alct\_data13 |
| A6 | Out | LVTTL | tmb\_data\_available |
| A7 | Out | LVTTL | tmb\_active\_feb1 |
| A8 | Out | LVTTL | fifo\_clock |
| A9 | Out | LVTTL | alct\_last\_frame |
| A10 | In | LVTTL | res\_from\_dmb2 |
| A11 | Out | LVTTL | tmb\_active\_feb6 (v6) |

|  |  |  |  |
| --- | --- | --- | --- |
| Pin | Dir | Logic | Signal |
| B1 | Out | LVTTL | tmb\_data13 |
| B2 | Out | LVTTL | alct\_data2 |
| B3 | Out | LVTTL | alct\_data6 |
| B4 | Out | LVTTL | alct\_data10 |
| B5 | Out | LVTTL | alct\_data14 |
| B6 | Out | LVTTL | /tmb\_write\_enable\_fifo |
| B7 | Out | LVTTL | tmb\_active\_feb2 |
| B8 | In | LVTTL | dmb\_request\_lct |
| B9 | In | LVTTL | dmb\_ext\_trig |
| B10 | In | LVTTL | res\_from\_dmb3 |
| B11 | Out | LVTTL | res\_to\_dmb3 |

|  |  |  |  |
| --- | --- | --- | --- |
| Pin | Dir | Logic | Signal |
| C1 | In | Pwr | Gnd |
| C2 | In | Pwr | VTT (+1.5V) |
| C3 | In | Pwr | Gnd |
| C4 | In | Pwr | VTT |
| C5 | In | Pwr | Gnd |
| C6 | In | Pwr | VTT |
| C7 | In | Pwr | Gnd |
| C8 | In | Pwr | VTT |
| C9 | In | Pwr | Gnd |
| C10 | In | Pwr | VTT |
| C11 | In | Pwr | Gnd |

|  |  |  |  |
| --- | --- | --- | --- |
| Pin | Dir | Logic | Signal |
| D1 | Out | LVTTL | tmb\_data14 |
| D2 | Out | LVTTL | alct\_data3 |
| D3 | Out | LVTTL | alct\_data7 |
| D4 | Out | LVTTL | alct\_data11 |
| D5 | Out | LVTTL | tmb\_ddu\_special |
| D6 | Out | LVTTL | tmb\_active\_feb\_flag |
| D7 | Out | LVTTL | tmb\_active\_feb3 |
| D8 | Out | LVTTL | /alct\_write\_enable\_fifo |
| D9 | In | LVTTL | res\_from\_dmb1 |
| D10 | Out | LVTTL | res\_to\_dmb5 |
| D11 | Out | LVTTL | res\_to\_dmb4 |

|  |  |  |  |
| --- | --- | --- | --- |
| Pin | Dir | Logic | Signal |
| E1 | Out | LVTTL | alct\_data0 |
| E2 | Out | LVTTL | alct\_data4 |
| E3 | Out | LVTTL | alct\_data8 |
| E4 | Out | LVTTL | alct\_data12 |
| E5 | Out | LVTTL | tmb\_last\_frame |
| E6 | Out | LVTTL | tmb\_active\_feb0 |
| E7 | Out | LVTTL | tmb\_active\_feb4 |
| E8 | Out | LVTTL | alct\_ddu\_special |
| E9 | Out | LVTTL | alct\_data\_available |
| E10 | Out | LVTTL | tmb\_active\_feb5 (v6) |
| E11 | In | LVTTL | dmb\_fpga\_pgm\_done |

P3A Backplane MPC+RPC Connector

Function: Sends and receives data to/from MPC.  
 Sends and receives data to/from RPC.

Connector Type: PCB: AMP Z-Pack 110 (25 rows of 5 pins) Female AMP 5352068-1 Backplane: AMP Z-Pack 110 (25 rows of 5 pins) Male  
Column C is connected to Ground

Table 25: P3A Backplane MPC Connector

See ADR\_MPCx\_FRAMEx on p48 for signal assignments

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Pin | Signal |  | Pin | Signal |  | Pin | Signal |  | Pin | Signal |
| A1 | /mpc\_out0 |  | B1 | /mpc\_out1 |  | D1 | /mpc\_out2 |  | E1 | /mpc\_out3 |
| A2 | /mpc\_out4 |  | B2 | /mpc\_out5 |  | D2 | /mpc\_out6 |  | E2 | /mpc\_out7 |
| A3 | /mpc\_out8 |  | B3 | /mpc\_out9 |  | D3 | /mpc\_out10 |  | E3 | /mpc\_out11 |
| A4 | /mpc\_out12 |  | B4 | /mpc\_out13 |  | D4 | /mpc\_out14 |  | E4 | /mpc\_out15 |
| A5 | /mpc\_out16 |  | B5 | /mpc\_out17 |  | D5 | /mpc\_out18 |  | E5 | /mpc\_out19 |
| A6 | /mpc\_out20 |  | B6 | /mpc\_out21 |  | D6 | /mpc\_out22 |  | E6 | /mpc\_out23 |
| A7 | /mpc\_out24 |  | B7 | /mpc\_out25 |  | D7 | /mpc\_out26 |  | E7 | /mpc\_out27 |
| A8 | /mpc\_out28 |  | B8 | /mpc\_out29 |  | D8 | /mpc\_out30 |  | E8 | /mpc\_out31 |
| A9 | /mpc\_in0 |  | B9 | /mpc\_in1 |  | D9 | NC |  | E9 | NC |
| A10 | NC |  | B10 | NC |  | D10 | NC |  | E10 | NC |
| A11 | NC |  | B11 | NC |  | D11 | NC |  | E11 | NC |
| A12 | NC |  | B12 | NC |  | D12 | NC |  | E12 | NC |
| A13 | NC |  | B13 | GND |  | D13 | NC |  | E13 | GND |
| A14 | NC |  | B14 | NC |  | D14 | NC |  | E14 | NC |
| A15 | rpc\_txa0 |  | B15 | +VcoreRAT |  | D15 | +AcoreRAT |  | E15 | +V3.3RAT |
| A16 | +3.3V |  | B16 | rpc\_txa3 |  | D16 | rpc\_txa2 |  | E16 | rpc\_txa1 |
| A17 | rpc\_txa7 |  | B17 | rpc\_txa6 |  | D17 | rpc\_txa5 |  | E17 | rpc\_txa4 |
| A18 | +3.3V |  | B18 | rpc\_rxa31 |  | D18 | rpc\_rxa38 |  | E18 | rpc\_rxa30 |
| A19 | rpc\_rxa27 |  | B19 | rpc\_rxa28 |  | D19 | rpc\_rxa29 |  | E19 | rpc\_rxa39 |
| A20 | +3.3V |  | B20 | rpc\_rxa24 |  | D20 | rpc\_rxa25 |  | E20 | rpc\_rxa26 |
| A21 | rpc\_rxa20 |  | B21 | rpc\_rxa21 |  | D21 | rpc\_rxa22 |  | E21 | rpc\_rxa23 |
| A22 | +3.3V |  | B22 | rpc\_rxa17 |  | D22 | rpc\_rxa18 |  | E22 | rpc\_rxa19 |
| A23 | rpc\_rxa13 |  | B23 | rpc\_rxa14 |  | D23 | rpc\_rxa15 |  | E23 | rpc\_rxa16 |
| A24 | +3.3V |  | B24 | rpc\_rxa10 |  | D24 | rpc\_rxa11 |  | E24 | rpc\_rxa12 |
| A25 | rpc\_rxa6 |  | B25 | rpc\_rxa7 |  | D25 | rpc\_rxa8 |  | E25 | rpc\_rxa9 |

P3B Backplane RPC+ALCT Connector

Function: Sends and receives data to/from ALCT.  
 Sends and receives data to/from RPC.

Connector Type: PCB: AMP Z-Pack 110 (25 rows of 5 pins) Female AMP 5352068-1 Backplane: AMP Z-Pack 110 (25 rows of 5 pins) Male

Table 26: P3B Backplane RPC+ALCT Connector

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Pin | Signal |  | Pin | Signal |  | Pin | Signal |  | Pin | Signal |  | Pin | Signal |
| A1 | +3.3V |  | B1 | rpc\_rxa3 |  | C1 | GND |  | D1 | rpc\_rxa4 |  | E1 | rpc\_rxa5 |
| A2 | rpc\_rxa35 |  | B2 | rpc\_rxa0 |  | C2 | GND |  | D2 | rpc\_rxa1 |  | E2 | rpc\_rxa2 |
| A3 | +3.3V |  | B3 | rpc\_rxa32 |  | C3 | GND |  | D3 | rpc\_rxa33 |  | E3 | rpc\_rx34 |
| A4 | alct\_txa1 |  | B4 | alct\_txa0 |  | C4 | GND |  | D4 | rpc\_rxa36 |  | E4 | rpc\_rxa37 |
| A5 | +3.3V |  | B5 | alct\_txa4 |  | C5 | GND |  | D5 | alct\_txa3 |  | E5 | rpc\_txa2 |
| A6 | alct\_txa8 |  | B6 | alct\_txa7 |  | C6 | GND |  | D6 | alct\_txa6 |  | E6 | rpc\_txa5 |
| A7 | +3.3V |  | B7 | alct\_txa11 |  | C7 | GND |  | D7 | alct\_txa10 |  | E7 | rpc\_txa9 |
| A8 | alct\_txa15 |  | B8 | alct\_txa14 |  | C8 | GND |  | D8 | alct\_txa13 |  | E8 | rpc\_txa12 |
| A9 | +3.3V |  | B9 | alct\_txa18 |  | C9 | GND |  | D9 | alct\_txa17 |  | E9 | rpc\_txa16 |
| A10 | alct\_txa25 |  | B10 | alct\_txa27 |  | C10 | GND |  | D10 | alct\_txa26 |  | E10 | rpc\_txa19 |
| A11 | +3.3V |  | B11 | alct\_txa22 |  | C11 | GND |  | D11 | alct\_txa21 |  | E11 | rpc\_txa20 |
| A12 | NC |  | B12 | NC |  | C12 | NC |  | D12 | NC |  | E12 | NC |
| A13 | +3.3V |  | B13 | NC |  | C13 | NC |  | D13 | NC |  | E13 | NC |
| A14 | NC |  | B14 | NC |  | C14 | NC |  | D14 | NC |  | E14 | NC |
| A15 | +3.3V |  | B15 | alct\_rear\_rxoe\_out |  | C15 | GND |  | D15 | alct\_txa24 |  | E15 | rpc\_txa23 |
| A16 | alct\_rxa0 |  | B16 | rpc\_smbtx\_out |  | C16 | GND |  | D16 | /hard\_reset\_rpc\_out |  | E16 | rpc\_free0\_out |
| A17 | +3.3V |  | B17 | alct\_rxa3 |  | C17 | GND |  | D17 | alct\_rxa2 |  | E17 | rpc\_rxa1 |
| A18 | alct\_rxa7 |  | B18 | alct\_rxa6 |  | C18 | GND |  | D18 | alct\_rxa5 |  | E18 | rpc\_rxa4 |
| A19 | +3.3V |  | B19 | alct\_rxa10 |  | C19 | GND |  | D19 | alct\_rxa9 |  | E19 | rpc\_rxa8 |
| A20 | alct\_rxa14 |  | B20 | alct\_rxa13 |  | C20 | GND |  | D20 | alct\_rxa12 |  | E20 | rpc\_rxa11 |
| A21 | +3.3V |  | B21 | alct\_rxa17 |  | C21 | GND |  | D21 | alct\_rxa16 |  | E21 | rpc\_rxa15 |
| A22 | alct\_rxa21 |  | B22 | alct\_rxa20 |  | C22 | GND |  | D22 | alct\_rxa19 |  | E22 | rpc\_rxa18 |
| A23 | +3.3V |  | B23 | alct\_rxa24 |  | C23 | GND |  | D23 | alct\_rxa23 |  | E23 | rpc\_rxa22 |
| A24 | alct\_rxa28 |  | B24 | alct\_rxa27 |  | C24 | GND |  | D24 | alct\_rxa26 |  | E24 | rpc\_rxa25 |
| A25 | +3.3V |  | B25 | alct\_rxa31 |  | C25 | GND |  | D25 | alct\_rxa30 |  | E25 | rpc\_rxa29 |

Backplane Pin Diagram



Front Panel Connector Locations

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Front Panel 🡪 |

| Multipurpose connector goes here

| ----

||. . | CFEB0

|| . .|

||. . |

|| . .|

||. . |

----- || . .| <- Pin 1 here (10.510)

Pin ^ | ----

one | |

| | ----

| ||. . |

to 2.130” || . .|

| ||. . |

Pin | || . .|

one \/ ||. . |

----- || . .| <- Pin 1 here (8.380)

Pin ^ | ----

one | |

| | ----

| ||. . |

to 2.130” || . .|

| ||. . |

Pin | || . .|

one \/ ||. . |

----- || . .| <- Pin 1 here (6.250)

Pin ^ | ----

one | |

| | ----

| ||. . |

to 2.130” || . .|

| ||. . |

Pin | || . .|

one \/ ||. . |

----- || . .| <- Pin 1 here (4.120)

Pin ^ | ----

one | |

| | ----

| ||. . |

to 2.130” || . .|

| ||. . |

Pin | || . .|

one \/ ||. . |

----- || . .| <- Pin 1 here (moved up from previous position 4/11/2001)

Pin ^ | ----

one | |

to 1.990” | Optical output here

bottom | |

edge \/ |

----- ----------------------------------------

CCB Front Panel

Table : Connector CCB Input connector P10

|  |  |  |
| --- | --- | --- |
| Pin  (+) | Pin  (-) | Signal |
| 1 | 2 | external\_clock40 |
| 3 | 4 | external\_clock40\_enable |
| 5 | 6 | external\_l1accept |
| 7 | 8 | dmb\_cfeb\_calibrate[0] |
| 9 | 10 | dmb\_cfeb\_calibrate[1] |
| 11 | 12 | dmb\_cfeb\_calibrate[2] |
| 13 | 14 | alct\_adb\_pulse\_sync |
| 15 | 16 | alct\_adb\_pulse\_async |
| 17 | 18 | clct\_external\_trigger |
| 19 | 20 | alct\_external\_trigger |
| 21 | 22 | tmb\_l1a\_request |
| 23 | 24 | ccb\_fp\_reserved\_in[0] |
| 25 | 26 | ccb\_fp\_reserved\_in[1] |
| 27 | 28 |  |
| 29 | 30 |  |
| 31 | 32 |  |
| 33 | 34 |  |

Table : CCB Output connector P11

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Pin  (+) | Pin  (-) | Signal | Test  Point | TMB  Assignment | Description |
| 1 | 2 | clct\_status[0] | 391-1 | pretrig | Sequencer pre-triggered |
| 3 | 4 | clct\_status[1] | 391-2 | seq\_busy | Sequencer busy |
| 5 | 6 | clct\_status[2] | 391-3 | invpat | Invalid pattern after drift delay |
| 7 | 8 | clct\_status[3] | 391-4 | daqmb | Dump to DMB in progress |
| 9 | 10 | clct\_status[4] | 391-5 | l1a\_window | L1A window |
| 11 | 12 | clct\_status[5] | 391-6 | l1a | L1A (should be in L1A window) |
| 13 | 14 | clct\_status[6] | 391-7 | tmb | CLCT sent for TMB match |
| 15 | 16 | clct\_status[7] | 391-8 | tmb\_flush | TMB found no match or rejected trigger |
| 17 | 18 | clct\_status[8] | 391-9 | nol1a\_flush | No L1A, Sequencer flushing event |
| 19 | 20 | ccb\_clock40 |  |  |  |
| 21 | 22 | ccb\_bx0 |  |  |  |
| 23 | 24 | ccb\_l1accept |  |  |  |
| 25 | 26 | ccb\_cmdstr |  |  |  |
| 27 | 28 | ccb\_fp\_reserved\_out[0] |  |  |  |
| 29 | 30 |  |  |  |  |
| 31 | 32 |  |  |  |  |
| 33 | 34 |  |  |  |  |

Table : CCB Output connector P12

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Pin  (+) | Pin  (-) | Signal | Test  Point | TMB  Assignment | Description |
| 1 | 2 | alct\_status[0] | 392-1 | alct\_active\_feb | ALCT fast active AFEB |
| 3 | 4 | alct\_status[1] | 392-2 | first\_valid | First muon valid pattern flag |
| 5 | 6 | alct\_status[2] | 392-3 | second\_valid | Second muon valid pattern flag |
| 7 | 8 | alct\_status[3] | 392-4 | first\_amu | First accelerator muon flag |
| 9 | 10 | alct\_status[4] | 392-5 | second\_amu | Second accelerator muon flag |
| 11 | 12 | alct\_status[5] | 392-6 | /wr\_fifo(alct) | ALCT /write enable raw-hit FIFO |
| 13 | 14 | alct\_status[6] | 392-7 | alct\_vpf | ALCT 1st Valid Pattern (TMB pipe) |
| 15 | 16 | alct\_status[7] | 392-8 | clct\_vpf | CLCT 1st Valid Pattern (TMB pipe) |
| 17 | 18 | alct\_status[8] | 392-9 | scint\_veto | Scintillator Veto (clears via VME) |
| 19 | 20 |  |  |  |  |
| 21 | 22 |  |  |  |  |
| 23 | 24 |  |  |  |  |
| 25 | 26 |  |  |  |  |
| 27 | 28 |  |  |  |  |
| 29 | 30 |  |  |  |  |
| 31 | 32 |  |  |  |  |
| 33 | 34 |  |  |  |  |

Documentation Revision History

| Version | Date | Action |
| --- | --- | --- |
| 1.00 | 07/12/2003 | Initial, copied from TMB2001 |
| 1.01 | 10/29/2003 | Replaced PHOS4 registers with DDD, update shunts table, rat signals updated |
| 1.02 | 03/15/2004 | Update 3D3444 registers, add RAT/RPC registers |
| 1.03 | 03/16/2004 | Move RAT register addy to match bdtest.v |
| 1.04 | 04/15/2004 | Copy from TMB2003 |
| 2.01 | 05/19/2004 | Add RPC Readout |
| 2.01 | 06/09/2004 | New registers B6-CC, 4 new header words, new raw hits format, started logic docs |
| 2.02 | 06/10/2004 | Add mpc\_tx\_delay, modify header 21,22 |
| 2.03 | 06/18/2004 | Add register CE for new scope trigger source, add mpc data format |
| 2.04 | 07/23/2004 | Add nph\_pattern to header word 21 |
| 2.05 | 08/03/2004 | Add counter registers |
| 2.06 | 10/01/2004 | Add scp bit to header |
| 2.07 | 10/04/2004 | Add mpc\_bx0 to reg ADR\_TMB\_TRIG |
| 2.08 | 10/07/2004 | Typos fixed |
| 2.09 | 12/15/2004 | Typos fixed |
| 3.00 | 06/02/2005 | Ported from TMB2004 v2.09 dated 12/15/04 |
| 3.00 | 06/09/2005 | Add rpc\_hard\_reset to boot reg, update ADR\_LOOPBK for RAT signals |
| 3.01 | 06/28/2005 | alct\_rxoe, alct\_txoe in 0E are now readonly to foil errant software |
| 3.02 | 08/01/2005 | Change default alct\_status\_en, tmb\_status\_en=0 for multi-crate use |
| 3.03 | 08/08/2005 | Change c\_status\_oe to ccb\_status\_oe |
| 3.04 | 02/27/2006 | Add configuration section |
| 3.05 | 05/24/2006 | Add jtag state machine registers, add alct scope channels |
| 3.06 | 07/28/2006 | Add vme state machine registers, update raw hits header, add prom info |
| 3.07 | 08/08/2006 | Add layer-or trigger mode |
| 3.08 | 09/05/2006 | Add rat delay registers |
| 3.09 | 09/15/2006 | Add CLCT processing steps |
| 3.10 | 10/16/2006 | Add ISE Version register, triad persistence default now 6 for 6 clocks |
| 3.11 | 04/09/2007 | Reduce RPCs from 4 to 2, add mpc\_oe, affects 86,B6,BA,BE,C4,CA,CC,header22 |
| 3.12 | 04/11/2007 | Remove duplicate header22 description, update header tables |
| 3.13 | 04/27/2007 | Add ignore ttc\_start/stop to Adr 2C, expand fmm\_state in Adr 9C |
| 3.14 | 05/16/2007 | New pattern finder registers |
| 4.01 | 05/24/0207 | New clct pattern finder algorithm |
| 4.02 | 06/21/2007 | New pattern ID numbers, new layer triggermods to Adrs 10,D4, and A0,A6,A8,AA,CA,CC,header16 |
| 4.03 | 07/05/2007 | Key layer shifted from ly3 to ly2, adjcfeb\_dist expanded to 6 bits, activefeb bugfix |
| 4.04 | 07/10/2007 | Firmware update, no change to doc |
| 4.05 | 07/24/2007 | Update Adr 78,88,8C descriptions to match current CLCT0/1 4-bit pattern IDs |
| 4.06 | 07/26/2007 | Fix text for adr 68, 6C, A6 |
| 4.07 | 08/06/2007 | Increase injector read-write adr to 10 bins in Adr 44, Adr BE |
| 4.08 | 08/30/2007 | New header/trailer format |
| 4.09 | 09/04/2007 | Mods to header format, expand VME counters to 30 bits |
| 4.10 | 09/10/2007 | New fields in header 24, new VME counters |
| 4.11 | 09/14/2007 | Header bug fixes, new no-alct counter |
| 4.12 | 09//21/2007 | Push hsds bit into pat[3] in documentation |
| 4.13 | 12/17/2007 | Switch to big-buffer logic |
| 4.14 | 01/28/2008 | Replace entire L1A logic, replace lct\_ quality |
| 4.15 | 02/05/2008 | Add raw hits RAM parity errors to header27 |
| 4.16 | 04/29/2008 | Major update for new flow-through triggering |
| 4.17 | 05/01/2008 | All scope channels reassigned, header frame bug fixes |
| 4.18 | 05/12/2008 | Add clct + alct bx0 heartbeat to mpc\_tx[11], mpc\_tx[27] |
| 4.19 | 05/23/2008 | Adr B0[15:14] Add clock\_lock\_lost and sync\_er |
| 4.20 | 06/03/2008 | Add counter clears on ttc\_resync, add aclt debug to scope, new active\_feb\_flag |
| 4.21 | 07/09/2008 | Replace jtag state machine, rename thresh signals, add pid\_thresh\_postdrift |
| 4.22 | 07/15/2008 | non-trigger readout mods |
| 4.23 | 08/12/2008 | Add bx0\_match, add me1a/b separation ram mux, add alct data tx delay |
| 4.24 | 08/28/2008 | Programmable stagger removed, csc firmware types created, new counters |
| 4.25 | 09/12/2008 | Add tmb logic signals to header40,41 |
| 4.26 | 09/16/2008 | Update tables for header words 36(rpc),40,41. Updated sample raw hits dump |
| 4.27 | 10/01/2008 | Mod header08,36,40,41, replaced scope module and vme register, jtag sel |
| 4.28 | 11/18/2008 | Add reg FE, L1A and parity logic mods, add sync err and parity err counters |
| 4.29 | 11/19/2008 | Remove stagger\_csc from Adr F4[1], staggering info is in Adr CC |
| 4.30 | 12/10/2008 | Add l1a\_lookback mode, l1a\_lookback reg + sequencer debug reg; add parity ram |
| 4.31 | 02/05/2009 | Add alct-loopback logic in alct.v module |
| 4.32 | 03/16/2009 | Add ecc to alct data, add ecc counters, add cfeb counters |
| 4.33 | 04/15/2009 | Updates for alct 80MHz output stages |
| 4.34 | 05/15/2009 | Miniscope added, RPC readout mods, bx0 test mode |
| 4.35 | 05/29/2009 | Add alct muonic timing |
| 4.36 | 06/22/2009 | More alct muonic mods |
| 4.37 | 06/29/2009 | Replace alct\_txd, alct\_rxd DDD delays with digital phase shifters |
| 4.38 | 07/13/2009 | Add cfeb muonic timing, 5 digital phase shifters, 2 vme delay registers |
| 4.39 | 08/14/2009 | CFEB muonic version, removed cfeb and alct\_rx posnegs, still has alct\_tx posneg |
| 4.40 | 08/25/2009 | ALCT+CFEB muonic with posneg sync stages, ISE 8.2sp3 |
| 4.41 | 09/02/2009 | Correct adr 16 |
| 4.42 | 09/08/2009 | Add digital phase shifter autostart |
| 4.43 | 09/21/2009 | Add sync register 0x120, limit bxn offsets to be < lhc\_cycle |
| 4.44 | 10/15/2009 | Add alct0==alct1 error counter, change D0[5] default to 1, enables alct err counter |
| 4.45 | 11/23/2009 | Text corrections |
| 4.46 | 12/09/2009 | Add alct and cfeb muonic figures |
| 4.47 | 12/16/2009 | Add cfeb bad bit detection and registers |
| 4.48 | 01/14/2010 | Add cfeb bad bit list to header30, mod bad bit ctrl reg |
| 4.49 | 02/10/2010 | Add event clear for aff, clct, mpc VME diagnostic registers |
| 4.50 | 03/12/2010 | Add blocked bits readout, clct-only mode bug fix |
| 4.51 | 04/09/1200 | Fix header30 typo, add firmware log for 3/19/2010 version |
| 4.52 | 05/14/2010 | Mod Adr 0x2A and Adr 0x120, add firmware log for 5/14/10 version |
| 4.53 | 07/02/2010 | Mod Adr 0x32, 0x42, 0x9E, 0x100, and hdr38[14] |
| 4.54 | 07/08/2010 | Move injector ram msbs to lookback reg, revert injector wen,ren |
| 4.55 | 07/15/2010 | Add miniscope section to header chapter |
| 4.56 | 09/03/2010 | Convert to MS Word 2010 |
| 4.57 | 08/17/2012 | Add startup delay for ALCT Spartan-6 mezzanine |
| 4.58 | 09/16/2012 | Add Virtex-6 GTX optical receivers |
| 4.59 | 09/23/2012 | Add Virtex-6 Sysmon |
| 4.60 | 10/15/2012 | Change pid\_thresh descriptions in adr 0xF4 |
| 4.61 | 03/07/2013 | Convert doc to docx, mod header + add registers for 7 DCFEB Virtex-6 |
| 4.62 | 2013/10/24 | Change order of keys in LCT quality module, documentation updated accordingly |
| 5.01 | 2013/12/19 | Created assignments for Mez-2013 TPs & SMT LEDs: qpll & mmcm lock monitoring. Also minor corrections for VME GTX register table (Adr 14C-158) |
| 5.02 | 2014/01/06 | Changes to Reset for CFEB badbits, fiber link monitor logic & GTX VME registers 14A-158 |
| 5.03 | 2014/01/08 | Add optical links to Fig. 1 and made some minor format changes for some tables |
| 5.04 | 2014/04/24 | Format cleaning. The following styles applied consistently throughout the text:  section title – “My Heading 1”  subsection title – “My Heading 2”  normal text – “Normal”  code excerpt – “Code in fixed font”  paragraph title – “Paragraph heading”  tables – “No spacing”  text on figures – “Text box in plot”  The styles are stored within document and accessible in Home -> Styles tab in Word |
| 5.05 | 2014/04/28 | Andrew Peck updated tables with the correct TMB2005 backplane pin assignments and connector (now 24,25). Some other minor formatting changes in that general section |
| 5.06 | 2014/05/15 | Add description of 5 new VME registers 17C – 188 to access data sent to MPC stored in FIFO (up to 512 last trigger events) |
| 5.07 | 2014/06/26 | Edited signal synchronization section. Start to edit list of VME addresses |
| 5.08 | 2014/07/31  2014/08/04 | Fix table with bits for Adr 15A ADR\_V6\_SYSMON Virtex-6 Sysmon ADC  Fix table for Adr 16A and 16C changing cfeb0 to cfeb5 and cfeb6 |
| 5.09 | 2015/02/12 | Edit VME register details for Adr 146 - 158, also 16A, 16C and 11E  Added startup timers in VME Adr 186 - 192 |

Firmware Change Log

Version 1/20/2015

Has redefined **enable** and **reset** control for Virtex-6 SNAP12 GTX fiber optic receivers (Adr 14A-158), and these now control GTX reset and GTX resync respectively

Added registers to monitor startup timing for several modules after a Hard Reset, with 100 ns units (Adr 186-192)

No longer uses the GTX internal RX Delay Align module for DCFEB fibers (which never worked well), but now uses just 2 phasers with one to control A-side DCFEB links (Adr 16A, used to be cfeb5\_rxd) and the other for B-side links (Adr 16C, used to be cfeb6\_rxd), and Adr 11E is also changed (rxd\_int\_delay control)

Version 12/26/2014

Improved enable and reset control for Virtex-6 SNAP12 GTX fiber optic receivers (Adr 14A-158)

Added registers to count “lock lost” conditions for MMCM and QPLL (Adr 146 and 148)

Now using the GTX internal RX Delay Align module for DCFEB fibers instead of the phaser clocks

Version 01/06/2014

Improved control & monitoring for Virtex-6 SNAP12 GTX fiber optic receivers

First applied in firmware version 12302013

TTC\_Resync now included in reset logic for CFEB badbits

cfeb\_badbits\_reset[4:0] = (cfeb\_badbits\_ctrl\_wr[4:0] | {5{ttc\_resync}});

cfeb\_badbits\_reset[6:5] = (cfeb\_v6\_badbits\_ctrl\_wr[1:0] | {2{ttc\_resync}});

GTX VME registers 14A-158 changed significantly to reflect improved fiber link monitor & control logic

Removed functions that were not useful (previously accessed in bits 10, 7:4, 2)

Reassigned some other functions to different bits (previous bit 9 🡪 bit 7, bit 3 🡪 bit 2)

Added new functions to bits 6:3 (gtx\_link\_bad, gtx\_link\_had\_err, gtx\_link\_good, gtx\_rx\_sync\_done)

Changed the readout response for bits 2:0 in registers 14C – 158 when master GTX control is asserted

When the master GTX control bits are set in register 14A (bits 2:0) they are now accurately reflected in the respective readout bits for the individual GTX links (bitwise OR in each GTX)

The error count now counts link sync failures when the PRBS function is not enabled

An occassional loss of sync for a link is expected due to SEUs, but large numbers of them or repeated occurrences may indicate a problem in the system

Increased the error count size to 8 bits and assigned this to bits 15:8

For registers 14C – 158 the maximum error count is hex E0 (n.b. a count larger than 1 is severe)

Register 14A is the sum of the other 7 counters, with maximum allowed value of hex FE

Version 12/19/2013

Adds diagnostic features for Mez-2013

Applied in firmware versions 12162013 – 12172013

Assign Mez-2013 SMT LEDs to indicate qpll & mmcm lock conditions and status changes

See Table 12A

Assign additional diagnostic signals to the Mez-2013 test points and SMT LEDs

See Tables 12A and 12B

Minor corrections to the table for VME GTX registers (Adr 14C-158)

Removed references to “all”

Version 03/08/2013

Adds support for 7 DCFEBs with Virtex-6

1) Modified ADR\_SEQCLCTM=0xB0 Sequencer CLCT msbs Register, Readonly

Added seq\_clctmsb\_rd[9:8] = clctf\_vme[6:5], bits were formerly unused

Now seq\_clctmsb\_rd[9:3] = clctf\_vme[6:0] Active cfeb list at TMB match

2) ADR\_PARITY=0xFA Parity errors

Changed sub-address assignments to accommodate DCFEB[6:5]

3) Modified ADR\_CNT\_CTRL=0xD0 Status Counter Control

Inserted 2 new counters after cnt[18], shifts subsequent counter addresses by 2

cnt\_en[19] <= cfeb\_hit\_at\_pretrig[5] CLCT pretrigger is on CFEB5

cnt\_en[20] <= cfeb\_hit\_at\_pretrig[6] CLCT pretrigger is on CFEB6

4) Modified ADR\_DELAY1\_INT=0x11E DDR Interstage delays for DCFEB[6:5]

Added:

cfeb5\_rxd\_int\_delay[3:0] = delay1\_int\_wr[7:4];

cfeb6\_rxd\_int\_delay[3:0] = delay1\_int\_wr[11:8];

5) Added ADR\_V6\_CFEB\_BADBITS\_CTRL=0x15C CFEB Bad Bits Control/Status

For DCFEB[6:5] badbits, extends 5 bit fields from ADR\_CFEB\_BADBITS\_CTRL

6) Added 6 new bad bit VME registers

ADR\_V6\_CFEB5\_BADBITS\_LY01 = 0x15E CFEB5 Bad Bit Array

ADR\_V6\_CFEB5\_BADBITS\_LY23 = 0x160 CFEB5 Bad Bit Array

ADR\_V6\_CFEB5\_BADBITS\_LY45 = 0x162 CFEB5 Bad Bit Array

ADR\_V6\_CFEB6\_BADBITS\_LY01 = 0x164 CFEB6 Bad Bit Array

ADR\_V6\_CFEB6\_BADBITS\_LY23 = 0x166 CFEB6 Bad Bit Array

ADR\_V6\_CFEB6\_BADBITS\_LY45 = 0x168 CFEB6 Bad Bit Array

7) Added 2 new Digital Phase Shifter VME registers

ADR\_V6\_PHASER7=0x16A DCM Phase Shifter Register: CFEB5 rxd

ADR\_V6\_PHASER8=0x16C DCM Phase Shifter Register: CFEB6 rxd

8) Added 6 New hot channel mask registers

ADR\_V6\_HCM501 = 0x16E CFEB5 Ly0,Ly1 Hot Channel Mask

ADR\_V6\_HCM523 = 0x170 CFEB5 Ly2,Ly3 Hot Channel Mask

ADR\_V6\_HCM545 = 0x172 CFEB5 Ly4,Ly5 Hot Channel Mask

ADR\_V6\_HCM601 = 0x174 CFEB6 Ly0,Ly1 Hot Channel Mask

ADR\_V6\_HCM623 = 0x176 CFEB6 Ly2,Ly3 Hot Channel Mask

ADR\_V6\_HCM645 = 0x178 CFEB6 Ly4,Ly5 Hot Channel Mask

9) Modified ADR\_MOD\_CFG 0x28 TMB Module Configuration Register

Replaced led\_flash\_rate from mod\_cfg\_wr[11:10] with cfeb\_exists[6:5]

Now: mod\_cfg\_rd[11:5] = cfeb\_exists[6:0] = CFEBs instantiated in this firmware

10) Added new VME register ADR\_V6\_EXTEND = 0x17A: DCFEB 7-bit extensions

Extends 5-bit cfeb fields in Adr 0x42 and 0x68 to 7 bits

mask\_all[6:5] =[1:0] Extend 0x42[4:0] = mask\_all[4:0]1=Enable, 0=Turn off all CFEB inputs

inj\_febsel[6:5] =[3:2] Extend 0x42[9:5] = inj\_febsel[4:0]1=Select CFEBn for RAM read/write

injector\_mask\_cfeb[6:5]=[5:4] Extend 0x42[14:10] = injector\_mask\_cfeb[4:0] 1=Enable CFEB(n) for injector

cfeb\_en\_vme[6:5] =[7:6] Extend 0x68[14:10] = cfeb\_en\_vme[4:0] 1=Enable CFEBs for triggering

11) Modified ADR\_LOOPBK 0x0E Loop-Back Control Register 2 remove 2 spare DMB signals

Reassigned dmb\_tx\_reserved to remove the 2 new active feb bits from the unused list

Updated bits [10:5] to match current firmware

12) TMB-to-DMB Active CFEB List backplane signals extended 5 bits to 7

Assigned 2 new bits to the next available spare DMB signals.

dmb\_tx[45:44] <= active\_feb\_list[6:5]

TMB schematic signals:

Signal res\_to\_dmb1 is now active\_feb\_list[5] on backplane pin E10

Signal res\_to\_dmb2 is now active\_feb\_list[6] on backplane pin A11

13) Modified header40\_[11:0] for 7-bit extensions to various 5-bit header fields

Header40\_[11:0] used to contain the peak RAM fence counter for raw hits storage debugging.

The peak count has been removed, but can still be read out with VME, and its dynamic

status is indicated by header40\_[10].

The flag bit in header40\_[11] indicates when bits [10:0] are valid for7-dcfeb firmware versions.

header40\_[1:0] = active\_feb\_mux[6:5]; Extend Hdr23[4:0] Active CFEB list sent to DMB

header40\_[3:2] = r\_cfebs\_read[6:5]; Extend Hdr23[9:5] CFEBs read out for this event

header40\_[5:4] = perr\_cfeb\_ff[6:5]; Extend Hdr27[12:8] CFEB RAM parity error, latched

header40\_[7:6] = cfeb\_badbits\_found[6:5]; Extend Hdr30[11:7] CFEB[n] has at least 1 bad bit

header40\_[9:8] = cfeb\_en[6:5]; Extend Hdr35[14:10] CFEBs enabled for triggering

header40\_[10] = buf\_fence\_cnt\_is\_peak; Current fence is peak number of fences in RAM

header40\_[11] = (MXCFEB==7); TMB has 7 DCFEBs so hdr40\_[10:0] are active

14) Modified raw hits readout

Readout can now include raw hits from 0 to 7 CFEBs, as

indicated by cfebs\_read[6:0]. The 7-bit CFFEB list cfebs\_read[6:0] is constructed

from cfebs\_read[4:0] in header23\_[9:5] and cfebs\_read[6:5] in header40\_[3:2].

In 5-CFEB firmware versions, header40[11] is zero (unless the is a fault in the readout logic).

A zero in header40\_[11] indicates a 5-CFEB TMB, and the bits in header40\_[10:0] should

not be used to extend 5-bit fields (cfebs\_read for instance).

15) Blocked bits readout

Readout can now include blocked hits from 0 to 7 CFEBs, as

indicated by cfebs\_read[6:0].

Version 09/23/2012

Add VME register 0x15A: ADR\_VIRTEX6\_SYSMON

Version 09/16/2012

Adds support for Virtex-6 SNAP12 GTX fiber optic receivers

Add VME register 0x148: ADR\_VIRTEX6\_SNAP12\_QPLL

Virtex-6 mezzanine QPLL reset and status

Virtex-6 mezzanine SNAP12 receiver serial interface

Add VME register 0x14A: ADR\_VIRTEX6\_GTX\_RX\_ALL

GTX control and status common to all 7 receivers

3) Add 7 VME registers 0x14C-0x158: ADR\_VIRTEX6\_GTX\_RX0 - ADR\_VIRTEX6\_GTX\_RX6

GTX control and status for individual receivers

4) Add event counters 79-85:

GTX receiver counters for fibers 0-6

Clears on gtx\_rx\_reset\_err\_cnt

5) Add mezzanine test points for GTX receiver [0]

`ifdef VIRTEX6

assign meztp20 = gtx\_rx\_start[0];

assign meztp21 = gtx\_rx\_valid[0];

assign meztp22 = gtx\_rx\_match[0];

assign meztp23 = gtx\_rx\_fc[0];

assign meztp24 = alct\_wait\_cfg;

assign meztp25 = lock\_tmb\_clock0;

assign meztp26 = 0;

assign meztp27 = sump;

`else

assign meztp20 = alct\_startup\_msec;

assign meztp21 = alct\_wait\_dll;

assign meztp22 = alct\_startup\_done;

assign meztp23 = alct\_wait\_vme;

assign meztp24 = alct\_wait\_cfg;

assign meztp25 = lock\_tmb\_clock0;

assign meztp26 = 0;

assign meztp27 = sump;

`endif

Version 08/17/2012

Delay JTAG PROM data stream to ALCT by 116msec to allow Spartan-6 mezzanine to finish configuration.

Spartan-6 takes 212msec to configure and TMB takes 100msec.

TMB sends JTAG data to ALCT 100+116=216msec, after a

simultaneous hard reset.

The 4msec pad allows ALCTs DLL/PLL time to lock.

2) Add VME register Adr 0x144 ALCT Spartan-6 startup delay

3) Add VME register Adr 0x146 ALCT Spartan-6 startup state machine status

4) Change Adr 0xD4[2]=jsm\_sel, was Write-only, is now Read/Write

Version 07/07/2010

1) Injector RAM mods:

Move injector RAM data msbs [17:16] from 0x44 to 0x100

Revert 0x44 wen and ren to independent RAM enables

Version 07/04/2010

1) Changed default Adr 0x100[15] l1a\_win\_pri\_en = 1

Enables window prioritizing mode to limit TMB to 1 readout per L1A

Version 07/01/2010

1) Bug fix in alct\*clct matching for a rare case when 2 CLCTs are exactly clct\_window bx apart in time.

Caused 1st CLCT to be replaced by 2nd CLCT, sending 2 identical events to L1A pipeline.

2) New algorithm for L1A matching prevents multiple events from reading out for 1 L1A.

Original algorithm allowed multiple events to read out if they were within the L1A window.

A system downstream of TMB apparently fails to tolerate multiple readouts per L1A.

Adr 0x100[15] l1a\_win\_pri\_en = 0 enables original multiple event readouts per L1A mode

l1a\_win\_pri\_en = 1 enables a prioritizing mode that limits TMB to 1 readout per L1A

Current default l1a\_win\_pri\_en = 0 to allow checking alct\*clct matching logic.

Next firmware release will set the default to 1.

3) New counter 58 is inserted after counter 57, all subsequent counters shift up 1channel number.

Counter 58 counts events lost from readout queue due to L1A window prioritizing that limits TMB to

1 event readout per L1A.

4) A buffer stalled-at-least-once bit has been added to Adr 0x9E[7] and Header38[14].

Indicates there was a least one buffer stall since the last resync.

5) Adr 0x44 rebuilt to expand CFEB pattern injectors to also assert L1A and ALCTs at an arbitrary time.

The 3 individual injector RAM select bits ren and wen have been replaced by 2-bit RAM addresses.

Injector RAM data width expanded from 16 to 18 bits to provide storage for 2 ALCTs and L1A.

6) Adr 0x32[3] alct\_inj\_ram\_en = 1 enables ALCT pattern injector RAM

Adr 0x32[4] l1a\_inj\_ram\_en = 1 enables L1A pattern injector RAM

7) Miniscope is now turned on by default: Adr 0x10C[0] mini\_read\_enable = 1.

Miniscope word count automatically inserted in readout stream by default Adr 0x10C[2]=1

New channel assignments, see Adr 0x10C section.

Version 05/14/2010

1) Add bx0 emulator enable to Adr 0x2A[15]. Power-up default is 0.

Generates bx0 that is ORed with ttc\_bx0. For use in systems lacking a CCB.

2) Add clock\_lock\_lost\_err\_en to Adr 0x120[5] (shifts other bits left by 1).

Add clock\_lock\_lost\_err\_ff to Adr 0x120[14].

Add force\_sync\_err to Adr 0x120[15].

3) Redesign vme.v to use initial blocks to specify power-up state for VME registers instead of load pulse

Add explicit integer widths to VME address decoder case statement.

Replace constants passed as signals from top level module with defparam mechanism.

4) Remove clock\_lock\_lost from OR with bx0\_sync\_err in sequencer.v

Add clock\_lock\_lost term to sync\_err\_ff in sync\_err\_ctrl.v

Remove bx0\_sync\_err from sync\_err\_ff, add it as an independent OR with sync\_err signal.

Fixes sync\_err fails-to-clear bug:

Sync\_err\_ff clears on ttc\_resync but bx0\_sync\_err takes n bx to clear.

TMB was synchronizing correctly on ttc\_resync, but incorrectly latched sync\_err=1.

5) Modify bx0 sync error counter[61] to count only when TMB is in trigger-run state.

Was counting sync errors before ttc\_resync arrived, now only counts errors that occur after a resync.

A non-zero value in this counter indicates incorrect bxns in TMB readouts and LCTs.

6) Modify FMM state machine fmm\_trig\_stop signal to power up as a 1.

Was powering up as 0, then set to 1 after the 1st clock cycle.

Entered trigger-run state for 1bx but was ignored since pre-trigger logic is held off 5bx after power up

7) Fix tmb.v kill\_clct logic for type C|D for 1 clct + 2 alct case where clct is on ME1A

Version 03/19/2010

1) Mod cfeb.v module busy hs delimiters for me1a me1b cscs to separate cfeb4 from cfebs0-3.

Prevents pattern finder from discarding 2nd CLCT at the me1a|me1b boundary.

Version 03/07/2010

1) Added requested mod that blocks bad cfeb distrips from both trigger path and data path.

2) Add bcb\_read\_enable to Adr72[15] p44 to include blocked CFEB DiStrip list in the

DMB readout stream:

Blocked bits include:

CFEB DiStrip bits turned off in the Hot Channel Mask,

CFEB DiStrip bits turned off by automatic bad-bits detection

Entire CFEBs turned off via mask\_all

Set Adr72[[15]=1 to enable blocked bits readout.

Power up default is 0, which is backwards compatible with older versions of the readout stream.

3) Add bcb\_read\_enable to Header29[13]

4) Document CFEB blocked DiStrip readout format, p98

5) Bug fix for CLCT-only trigger mode

The 2nd CLCT in previous firmware versions had bxn=0 in the LCT sent to MPC when using the clct-only mode, and there was also no ALCT coincidence.

Version 02/10/2010

1. Add event\_clear\_vme to AdrAC[15] to clear aff, clct, and mpc VME read-back registers
2. Add active\_feb list reversal for TypeB CSCs

Version 01/14/2010 CFEB bad di-strip bit detection

1) Header30[11:7] = cfeb\_badbits\_found[4:0] Bad distrip bits detected in cfebn[n]

Header30[12] = 0

2) New VME regisers Adr 0x122 to 0x142

Adr 122 ADR\_CFEB\_BADBITS\_CTRL, CFEB Bad Bits Control/Status

[04:00] RW cfeb\_badbits\_reset[4:0] Reset bad cfeb bits FFs for cfeb[n]

[09:05] RW cfeb\_badbits\_block[4:0] Block bad cfeb bits in cfeb[n]

[14:10] R cfeb\_badbits\_found[4:0] CFEB[n] has at least 1 bad bit

[15] R cfeb\_badbits\_blocked At least one CFEB has a bad bit that was blocked

Adr 124 ADR\_CFEB\_BADBITS\_TIMER CFEB Bad Bits Check Interval

Sets number of bx a bit must be continuously high before being marked as bad.

Adr 126 ADR\_CFEB0\_BADBITS\_LY01 CFEB0 Ly0,Ly1 Bad Bits List

Adr 128 ADR\_CFEB0\_BADBITS\_LY23 CFEB0 Ly2,Ly3 Bad Bits List

Adr 12A ADR\_CFEB0\_BADBITS\_LY45 CFEB0 Ly4,Ly5 Bad Bits List

Adr 12C ADR\_CFEB1\_BADBITS\_LY01 CFEB1 Ly0,Ly1 Bad Bits List

Adr 12E ADR\_CFEB1\_BADBITS\_LY23 CFEB1 Ly2,Ly3 Bad Bits List

Adr 130 ADR\_CFEB1\_BADBITS\_LY45 CFEB1 Ly4,Ly5 Bad Bits List

Adr 132 ADR\_CFEB2\_BADBITS\_LY01 CFEB2 Ly0,Ly1 Bad Bits List

Adr 134 ADR\_CFEB2\_BADBITS\_LY23 CFEB2 Ly2,Ly3 Bad Bits List

Adr 136 ADR\_CFEB2\_BADBITS\_LY45 CFEB2 Ly4,Ly5 Bad Bits List

Adr 138 ADR\_CFEB3\_BADBITS\_LY01 CFEB3 Ly0,Ly1 Bad Bits List

Adr 13A ADR\_CFEB3\_BADBITS\_LY23 CFEB3 Ly2,Ly3 Bad Bits List

Adr 13C ADR\_CFEB3\_BADBITS\_LY45 CFEB3 Ly4,Ly5 Bad Bits List

Adr 13E ADR\_CFEB4\_BADBITS\_LY01 CFEB4 Ly0,Ly1 Bad Bits List

Adr 140 ADR\_CFEB4\_BADBITS\_LY23 CFEB4 Ly2,Ly3 Bad Bits List

Adr 142 ADR\_CFEB4\_BADBITS\_LY45 CFEB4 Ly4,Ly5 Bad Bits List

Usage Notes:

1) Dead channel detection:

Detects CFEB channels that never fire

Set Adr122[09:5]=0x00 to turn off badbit blocking

Set Adr124[15:0]=0x0001 to set high-time threshold to 1 bx

Read dead channel list from Adrs126-142

2) Noisy channel detection:

Detects CFEB channels that have after-pulsing or frequent firing,

for instance, 3 consecutive triad starts)

Set Adr122[09:5]=0x00 to turn off badbit blocking

Set Adr124[15:0]=0x0007 to set high-time threshold to 7 bx

Read noisy channel list from Adrs126-142

3) Bad bit detection or blocking

Detects CFEB channels that are always high or high for an unreasonable length of time

Set Adr122[09:5]=0x1F to turn on badbit blocking (or set 0x00 for just monitoring)

Set Adr124[15:0]=0x0DEC to set high-time threshold to 3564 bx or something similar

Read bad channel list from Adrs126-142

Version 10/15/09 ALCT duplicate alct detection + Header r-type

1) Header05[10:9] r\_type always == 1 on previous versions.

It should equal fifo\_mode unless the event buffer is full.

2) Added ALCT structure error counter cnt[75] to count events where alct0==alct1.

3) AdrD0[5] Changed default to cnt\_alct\_debug=1 to enable ALCT data structure error counters.

N.B. The ALCT structure error counters are only 8 bits, and could reach full scale quickly.

So, AdrD0[02] cnt\_stop\_on\_ovf should be 0, when setting cnt\_alct\_debug=1, otherwise

all event counters will stop counting if there are excessive ALCT errors.

Version 09/21/09 Synchronization Error Control Register + bxn offset limit

Add limits for bxn\_offset\_pretrig and bxn\_offset\_l1a

bxn\_offset > lhc\_cycle is converted to lhc\_cycle-1

Add sync\_err\_ctrl register Adr 0x120

Version 09/08/09 Digital Phase Shifter Autostart

Add vsm\_phaser\_auto to AdrDA[11].

Default = 1, starts digital phase shifters after VME user PROM is read

Version 08/25/09 PosNeg sync FFs for ALCT and CFEBs

Same as 8/14/09 version but has ALCT and CFEB posneg sync stages enabled.

Switched to ISE 8.2sp3 because ISE 10.1sp3 could not complete PAR.

Documentation updates to conform firmware to c++ demo code:

Phaser register signal names now absorb hcycle and qcycle bits into 1 8-bit phase delay:

Adr10E: alct\_rxd\_delay[7:0] Delays latching data received from ALCT in 0.1ns steps

Adr110: alct\_txd\_delay[7:0] Delays data transmitted to ALCT in 0.1ns steps

Adr112-11A: cfeb[n]\_rxd\_delay[7:0] Delays latching data received from CFEB[n] in 0.1ns steps

Modify interstage delay signals to make it clear they are integer bx delays:

Adr38: alct\_txd\_int\_delay[3:0] Delay data transmitted to ALCT by integer bx

Adr11C-11E: cfeb[n]\_rxd\_int\_delay[3:0] Delay data received from CFEB[n] by integer bx

Version 08/14/09 Digital Phase shifters for CFEBs

Has both ALCT and CFEB muonic timing.

Disabled cfeb posnegs and alct\_rxd\_posneg else compile fails. Alct\_txd\_posneg is OK.

Notes on ALCT and CFEB timing adjustments:

ALCT:

1) Select a Time of Flight delay:

Using DDD 2ns steps, ranging from 0 to 12, spanning 0 to 24ns

Based on distance from IP to “some point” on the CSC

Also compensate for tmb-to-alct cable propagation delay differences between CSCs

Write alct\_tof\_delay to DDD chip in Adr16[3:0]

2) Tune alct\_rxd\_delay to the good-data window center

Using Digital Phase Shifter 0.1ns steps, ranging from 0 to 255, spanning 0 to 25ns

Put ALCT into loopback mode to send a test pattern to TMB

Scan alct\_rxd\_delay 0-255 using Phaser0 Adr10E[15:8]

Scan alct\_rxd\_posneg 0-1 using Phaser0 Adr10E[15:8] (disabled in 8/14/09 firmware)

3) Tune alct\_txd\_delay to the good-data window center

Using Digital Phase Shifter 0.1ns steps, ranging from 0 to 255, spanning 0 to 25ns

Put ALCT into loopback mode to send a test pattern to TMB

Scan alct\_txd\_delay 0-255 using Phaser1 Adr110[15:8]

Scan alct\_rxd\_posneg 0-1 using Phaser1 Adr110[15:8] (not disabled in 8/14/09 firmware)

CFEBs:

1) Select a Time of Flight delay:

Using DDD 2ns steps, ranging from 0 to 12, spanning 0 to 24ns

Based on distance from IP to “some point” on the CSC

Also compensate for tmb-to-cfeb cable propagation delay differences between CSCs

Write cfeb\_tof\_delay to DDD chip in Adr18[11:8]

2) Tune cfeb[n] clock delays for simultaneous arrival at all 5 cfebs

Using DDD 2ns steps, ranging from 0 to 12, spanning 0 to 24ns

Delays might be set according to known cable propagation delays

Delays might be determined empirically by setting high comparator thresholds to make

the analog signal time-over-threshold less than 25ns, then scanning DDD delay vs

6-hit efficiency.

Write cfeb[n] clock delays to DDD channels in Adr18[15:12] and Adr1A[15:0]

3) Tune cfeb\_rxd\_delay for cfeb[n] to the good-data window center

Using Digital Phase Shifter 0.1ns steps, ranging from 0 to 255, spanning 0 to 25ns

Generate CFEB test pulses or use muon tracks

Scan cfeb\_rxd\_delay 0-255 using Phaser2-6 Adr112-Adr11A bits[15:8]

Scan cfeb\_rxd\_posneg 0-1 using Phaser2-6 Adr112-Adr11A

4) Tune cfeb inter-stage integer delay for cfeb[n]

Set a delay 0-15bx so that triad bits from all 5 CFEBs arrive at TMB on the same bxn

Might be done by pulsing all 5 CFEBs simultaneously, then checking the CFEB

raw hits readout to see that triad start bits all appear in the same bxn.

Set cfeb[n] inter-stage delays in Adr11C-Adr11E

Version 07/13/09 Digital Phase shifters for CFEBs

Added 5 digital phase shifters for cfeb rxd delays: Adr112-Adr11A

Add 2 VME registers: Adr11C-Adr11E for CFEB interstage delays

Version 06/29/09 Digital Phase shifters for ALCT

Two digital phase shifters replace DDD delays for alct\_txd\_delay and alct\_rxd\_delay

Add VME registers Adr10E and Adr110 for digital phase shifters

Adr14[13,11,10] reverted to old format, removed phase shifter DCM locks

Adr30[15:13] removed posnegs, they now reside in Adr10E and Adr110, cfeb posneg is gone for now

Version 06/22/09 Muonic Timing for ALCT

Added muonic timing to float ALCT board in clock-space independently

of good-data rxd|txd windows.

Changes to DLL lock register:

Adr14[10] lock\_alct\_rxd [these get undone in 6/29/09 version]

Adr14[11] lock alct\_txd

Adr 14[13] lock\_cfeb\_rxd

Changes to DDD delay and posneg registers:

Adr16[3:0] alct\_tof\_delay Shift entire ALCT in clock-space to compensate for muon time of flight

Adr16[7:4] alct\_txd\_delay Latches TMB-to-ALCT data in middle of transmit data window

Adr16[11:8] dmb\_tx\_delay Change default to 6

Adr18[3:0] alct\_rxd\_delay Latches ALCT-to-TMB data in middle of receive data window

Adr18[7:4] cfeb\_rxd\_delay Latches CFEB-to-TMB data in middle of receive data window

Adr18[11:8] cfeb\_tof\_delay Shift all CFEBs in clock-space to compensate for muon time of flight.

Adr30[8] alct\_clock\_en\_use\_ccb moved from [11]

Adr30[9] alct\_clock\_en\_use\_vme moved from [12]

Adr30[10] alct\_muonic 1=ALCT muonic version instantiated, readonly

Adr30[11] cfeb\_muonic 1=CFEB muonic version instantiated, readonly

Adr30[12] unassigned

[These changes get undone in 6/29/09 version:]

Adr30[13] cfeb\_rxd\_posneg Sets receive data posneg clock polarity (new signal)

Adr30[14] alct\_txd\_posneg Sets transmit data posneg clock polarity, (was alct\_posneg)

Adr30[15] alct\_rxd\_posneg Sets receive data posneg clock polarity (new signal)

Changed 8bx constant delay in alct random number pipeline to be VME programmable

Added 2bx to compensate for muonic sync stages.

Default delay is now 8+2-1=9bx

Good spots for reference TMB+ALCT384 occur at pipedepth 4 when alct\_sync\_rxdata\_pre=9

Adr104[15:12] = alct\_sync\_rxdata\_pre[3:0], default=9

Changed Adr 0E[15:11] to connect dmb\_tx\_reserved[4:0] to dmb\_tx[48:44]

Adr 0E[15:11] =dmb\_tx\_reserved[4:0], just set to 0 for now

Version 06/05/09

Re-structure dmb\_tx[48:0] flip-flops to force IOB instantiation

No other changes

Version 05/15/09

Added miniscope to monitor clct pretrigger processing and alct\*clct matching.

Added miniscope VME register Adr 0x10C.

Rebuilt parity register Adr 0xFA to accept miniscope RAM parity.

Restructured DMB image RAM from 5 BRAMs down to 4 BRAMs to free up 1 RAM

Reduced ALCT raw hits storage RAM from 2048bx down to 1024bx to free up 1 RAM

Replaced Virtex-E era RPC de-mux and pipeline stages to minimize latency.

Added clct pre-trigger signal to RPC readout to DMB in a former always-zero bit.

Added data=address test mode to RPC storage RAM

Added 8bx constant delay in alct random number pipeline. Good spots at depth 12 before are now at 4.

Removed legacy alct signals from Adr 0x38,0x30 and Hdr 30[12:7] that are now used for ECC parity.

Added alct\_ecc\_err\_blank to Adr 038[2] to blank alct data that has uncorrected ecc errors.

Added counter[6] to count alct data blanked due to uncorrected ecc errors

Adr 0x30: Removed Adr30[11:8] alct\_reserved\_out[3:0], as these bits now carry ecc parity.

Adr 0x38: Adr38 has been reorganized to make room for the new alct\_ecc\_err\_blank signal

**Moved alct\_ecc\_en to Adr38[1] n.b. this affects loop-back test software**

Added alct\_ecc\_err\_blank to Adr38[2] blanks alcts with uncorrected ecc errors.

**Moved alct\_sync\_ecc\_err to Adr38[4:3] n.b. this affects loop-back test software**

Removed Adr38[2:1] seq\_status[1:0]

Removed Adr38[4:3] seu\_status[1:0]

Removed Adr38[8:5] reserved\_out[3:0]

alct\_stat\_rd[0] = alct\_cfg\_done; // R ALCT FPGA loaded

alct\_stat\_rd[1] = alct\_ecc\_en; // RW Enable ALCT ECC decoder, else do no ECC correction

alct\_stat\_rd[2] = alct\_ecc\_err\_blank; // RW Blank alcts with uncorrected ecc errors

alct\_stat\_rd[4:3] = alct\_sync\_ecc\_err[1:0];// R ALCT sync mode ecc error syndrome

alct\_stat\_rd[11:5] = alct\_stat\_wr[11:5]; // RW Free

alct\_stat\_rd[15:12] = alct\_txd\_delay[3:0]; // RW ALCT data transmit delay, integer bx

Adr 0xFA: AdrFA has been reorganized to make room for the new miniscope RAM parity

perr\_adr[] expanded from 3 to 4 bits.

Adr 0x10C: New Miniscope control register.

Adr 0xBC[14] Added rpc\_tbins\_test for RPC RAM data=address test mode

Adr 0xCA[9] Moved bx0\_match to [10]

Added bx0\_vpf\_test to [9]

Hdr27[13] now ORs miniscope RAM parity errors with RPC RAM parity errors

Hdr19[14] vme\_exists replaced by mini\_read\_enable

RPC readout format: unused tbin bit[11] was always 0, now has clct-pretrigger flag

Counter[06]: Inserted scnt[06]="ALCT: trigger path ECC>=2-bit error, ALCT discarded"

Shifts subsequent counters up by 1 address.

TMB readout format changed to include miniscope data and markers when mini\_read\_enable=1.

By default, inserts B07 marker, 22 scope words, then E07 marker after RPC data.

ALCT legacy cable signals that are now ecc parity updated in

Table 18: J5 ALCT Cable1 Connector [J10 on ALCT board]

Table 19: J6 ALCT Cable2 Connector [J11 on ALCT board]

Versions 04/07/2009 - 04/14/09

Added TMB-to-ALCT sync-stage and inter-stage in alct.v module.

Improves alct\_rx\_clock windows, and allows a ½-cycle shift

in alct\_rx\_clock at inter-stage, but adds 2bx to output signals.

Add Adr 30[14] alct\_posneg

Modified UCF to constrain ALCT inter-stage flip-flops to FPGA slice locations near ALCT IOBs

Compiled 1 version with ALCT 80 MHz IOBs set to Slew=Fast | Drive=12

Another version has ALCT 80 MHz IOBs set to LVDCI\_33 (Digitally Controlled Impedance, 50Ω)

Added TMB-to-ALCT 80MHz diagram to this doc

Version 03/16/2009

New Features:

Error Correcting Code to ALCT-to-TMB trigger data path, using reserved rx signals

Error Correcting Code to TMB-to-ALCT TTC command path, using reserved tx signals

Separate bxn counter and offset for L1A

New event counters + re-numbered ALCT-counter-group 0-11 [see counter register adr 0x000]

(see AdrD0 p61 for details)

3 for ECC rx data

3 for ECC tx data

5 for individual CFEB pre-triggers

1 for alct\_bx0

Register Changes:

Adr 016 change delay\_ch0[3:0] alct\_tx\_clock default to 11 for use with reference ALCT

Adr 076 rename from adr\_seq\_offset to adr\_seq\_offset0

Adr 076 rename bxn\_offset[11:0] to bxn\_offset\_pretrig[11:0]

Adr 0D0 increase cnt\_select[6:0] by 1 bit to address more event counters

Adr 0D0 move perr\_reset from AdrD0[15] to AdrFA[6]

Adr 10A new register adr\_seq\_offset1

Adr 10A add bxn\_offset\_pretrig[11:0], which is a separate bxn offset for the new L1A bxn counter

Adr038[10:9] new signal: alct\_sync\_ecc\_err[1:0] is ALCT sync-mode ECC error code, readonly

Adr038[11] new signal: alct\_ecc\_en is ALCT ECC trigger data correction enable with default=1

N.B. setting alct\_ecc\_en =0 stops ALCT trigger data correction, but does not affect ECC counters

Header Changes:

Header30[6:5] now contains alct\_ecc\_err[1:0]

ALCT Cable Signal Changes for ECC

|  |  |  |
| --- | --- | --- |
| Old | New | Comment |
| reserved\_in[0] | parity\_in[0] | ECC parity [5:0] for TMB-to-ALCT |
| reserved\_in[1] | parity\_in[1] | “” |
| reserved\_in[2] | parity\_in[2] | “” |
| reserved\_in[3] | parity\_in[3] | “” |
| seq\_cmd[0] | seq\_cmd[0] | Activates ALCT sync mode |
| seq\_cmd[1] | parity\_in[4] seq\_cmd[1] | Parity sent unless in sync mode |
| seq\_cmd[2] | seq\_cmd[2] | Activates ALCT sync mode |
| seq\_cmd[3] | seq\_cmd[3] | parity\_in[5] | Parity sent unless in sync mode |
|  |  |  |
| seq\_status[0] | parity\_out[0] | ECC parity [6:0] for ALCT-to-TMB |
| seq\_status[1] | parity\_out[1] | “” |
| seu\_status[0] | parity\_out[2] | “” |
| seu\_status[1] | parity\_out[3] | “” |
| reserved\_out[0] | parity\_out[4] | “” |
| reserved\_out[1] | parity\_out[5] | “” |
| reserved\_out[02] | parity\_out[6] | “” |

Version 02/05/2009

Added ALCT-TMB sync mode loop-back test logic to alct.v module.

Mod Adr F2: Change compiler ID field to accommodate extra digit for ISE 10.1I

Add Adr104, Adr106, Adr108 for ALCT sync-mode data

Version 01/13/2009

Rename ALCT cable 2 pair 15 from reserved\_in4 to seq\_cmd3

Adr 30: alct\_cfg: rename Adr30[7] to seq\_cmd3, replaces reserved\_in4

Version 12/10/2008

Add L1A-only readout mode with full header and raw hits

Add L1A lookback offset in new VME register Adr 0x100

Add sequencer debug signals to new VME register Adr 0x102

Replaced parity errors Adr 0x0FA with sub-adr multiplexing

Add 35-bit RAM parity error array to Adr 0x0FA

Version 11/18/2008

Replaced L1A data storage logic:

Moved L1A data from header RAM to fence queue RAM

Allows L1A-only TMB readout mode to have valid data in short-header (i.e. bxn at L1A arrival)

To enable L1A-only TMB readout

[1] fifo\_mode=3 sets short header

[2] l1a\_allow\_notmb=1 allows readout when tmb didn’t trigger for that L1A

[3] turn off TMB pre-triggers (set mask\_all=0 or halt pre-trigger machine)

[4] send L1A via TTC....all ~500 TMBs should send short header to DDU

Inverted raw hits RAM parity.

Now parity bit=1 if RAM data[7:0]=8’b00000000

Modified CFEB and RPC raw hits RAMB16s to be read-first instead of write-first.

Guarantees parity data on port B is valid before writing new data to port A.

AdrFE[2] BXN latched at last L1A

New Event Counters

Inserted 2 new counters after counter[47]

counter[48]= Sync error, bxn!=offset at bx0 arrival or bx0 did not arrive at bxn==offset

counter[49]= Raw hits RAM parity error, possible radiation SEU

Note on enabling internal scope readout to DMB/DDU

Adr98 = 0x108B

Adr9A = 0x0000

AdrCE = 0x0000

Version 09/30/2008

AdrD4[2] add jsm\_sel to select old/new alct user prom format.

This is a write-only bit, it reads back the value of vsm\_jtag\_auto

New Internal Scope Logic:

Allows scope channel data to be inserted in DMB readout stream

All scope channel signal assignments have bee replaced

Adr98 Replaced with new internal scope signals

Adr9A Replaced with new internal scope signals

To enable scope data in DMB readout, set

scp\_ch\_trig\_en =1

scp\_runstop=1

scp\_force\_trig=0

scp\_auto=1 (also appears in Header19[13]

scp\_tbins=4 (may be 0 to 7, number of scope tbins = 64\*(scp\_tbins+1), thus spanning 64 to 512)

scp\_nowrite=0

Rename Event Counters to better describe their functions

counter[22]= TMB matching discarded an ALCT pair (all alcts in the pair were discarded)

counter[23]= TMB matching discarded a CLCT pair (all clcts in the pair were discarded)

New Event Counters

Inserted 2 new counters after counter[23]

counter[24]= TMB matching discarded CLCT0 from ME1A

counter[25]= TMB matching discarded CLCT1 from ME1A

Shifts all subsequent counter addresses up by 2

Header Updates:

header08\_[12] r\_tmb\_clct0\_discard; TMB discarded clct0 from ME1A

header08\_[13] r\_tmb\_clct1\_discard; TMB discarded clct1 from ME1A

Version 09/12/2008

Added tmb\_trig\_pulse to header40[14]

Added tmb\_trig\_keep to header41[9]

Added tmb\_non\_trig\_keep to header41[10]

Version 09/05/2008

Add blocking of LCTs to MPC for ME1A

Version 08/28/2008

Logic modifications:

Firmware compile type codes introduced, replaces programmable stagger and reversal

Added hs reversal for ME1A and ME1B and full hs reversal for non-ME1A/B CSCs

Added blocking for ME1A to MPC, but is not yet functional in this release

Added 2 state machines to detect and count TTC lock loss signals from CCB

Adr 2E[9]: Add ccb\_ttcrx\_ready TTC ready signal from CCB

Adr 2E[10]: Add ccb\_qpll\_locked Lock signal from CCB

Adr 2E changed register symbolic name from ADR\_CCB\_STAT to ADR\_CCB\_STAT0

Adr FA[15:0] Add new register ADR\_PARITY contains parity SEU error status

Adr FC[15:0] Add new register ADR\_CCB\_STAT1 contains TTC lock status from lock state machines

Rename event counter [5] “Pre-trigger was on any cfeb”

Inserted 2 new event counters after counter[5], shifts all other counter addresses up 2

[6] Pre-trigger was on ME1A cfeb4 only

[7] Pre-trigger was on ME1B cfebs0-3 only

Add 2 new event counters after counter[57],

[58] CCB: TTCrx lock lost

[59] CCB: qPLL lock lost

Add new register AdrFC for CCB lock detection

AdrFC[00] ccb\_ttcrx\_lock\_never TTCrx lock never achieved

AdrFC [01] ccb\_ttcrx\_lost\_ever TTCrx lock was lost at least once

AdrFC [02] ccb\_qpll\_lock\_never QPLL lock never achieved

AdrFC [03] ccb\_qpll\_lost\_ever QPLL lock was lost at least once

Extended trigger source vector in VME and Header:

Adr7C[9] me1a\_only\_pretrig

Adr7C[10] me1b\_only\_pretrig

Hdr40[12]=r\_trig\_source\_vec[9]

Hdr40[13]=r\_trig\_source\_vec[10]

Introduced Firmware Compile Type Codes

A=Normal CSC

B=Reversed CSC

C=Normal ME1B, Reversed ME1A

D=Reversed ME1B, Normal ME1A

Extended ½-strip reversal and ME1A/B signals to Adr CC

Adr CC[05] csc\_me1ab 1= CSC is ME1A or ME1B. 0=normal CSC

Adr CC[06] stagger\_hs\_csc 1=Staggered Adr CSC, 0=non-staggered

Adr CC[07] reverse\_hs\_csc 1=Reversed staggered CSC, non-me1

Adr CC[08] reverse\_hs\_me1a 1=reversed me1a hstrips

Adr CC[09] reverse\_hs\_me1b 1=reversed me1b hstrips

Adr CC[15:12] csc\_type[3:0] Firmware compile type A, B,C or D

Added ½-strip reversal signals to Header

Header does not contain csc\_type explicitly, but csc\_type can be inferred from reversal signals

in Hdr39[14:12] and Hdr20[14]

Hdr20[14] stagger\_hs\_csc CSC Staggering ON

Hdr39[12] reverse\_hs\_csc 1=Reverse staggered CSC, non-me1

Hdr39[13] reverse\_hs\_me1a 1=ME1A hstrip order reversed

Hdr39[14] reverse\_hs\_me1b 1=ME1B hstrip order reversed

Added ME1A LCT blocking to MPC [not yet functional in this release]

Adr CC[03] mpc\_me1a\_block Block ME1A LCTs from MPC, still queue for readout

Adr CC[04] cnt\_non\_me1ab\_en Allow clct pretrig counters count non me1ab events

End of 8/28/2008 mods

Version 08/12/2008

Adr38[15:12] add alct\_txd\_delay[3:0] to delay alct tx data, delay=0 by default has same timing as previous firmware versions.

Adr CA[9]: add bx0\_match

Hdr30[14]: add bx0\_match

Version 08/04/2008

Adr F6[6]: add clct\_sep\_ram\_sel\_ab to select A or B separation RAM data readback

Version 08/01/2008

Adr F4[1]: stagger\_csc is now read-only, set at firmware compile time

Header36: r\_nrpcs\_read in header now gated with rpc\_read\_enable.

now indicates 0 rpcs when rpc readout is disabled

Version 07/15/2008

Added ability to readout non-triggering events

Header41[0] = VME settings for tmb\_allow\_alct, for trigger and readout

Header41[1] = VME settings for tmb\_allow\_clct, for trigger and readout

Header41[2] = VME settings for tmb\_allow\_match, for trigger and readout

Header41[3] = VME settings for tmb\_allow\_alct\_ro, for non-triggering readout

Header41[4] = VME settings for tmb\_allow\_clct\_ro, for non-triggering readout

Header41[5] = VME settings for tmb\_allow\_match\_ro, for non-triggering readout

Header41[6] = alct-only non-triggering event

Header41[7] = clct-only non-triggering event

Header41[8] = alct\*clct match non-triggering event

Header41[9] = This event is a non-triggering readout

New Event counter at subadr[19] counts non-triggering events queued for readout

Shifts all subsequent counter addresses up 1

New VME register adrCC:

AdrCC[0] = tmb\_allow\_alct\_ro allow alct-only non-triggering event readout

AdrCC[1] = tmb\_allow\_clct\_ro allow clct-only non-triggering event readout

AdrCC[2] = tmb\_allow\_match\_ro allow alct\*clct-match non-triggering event readout

Version 07/09/2008

Replaced entire ALCT UserPROM JTAG State Machine

New compressed data format: see JTAG PROM-1 section p93

Adr 70: Move dmb\_thresh[2:0] from adr F4[8:6] to adr70[9:7]

Adr 70: Rename dmb\_thresh to dmb\_thresh\_pretrig

Adr 70: Rename hit\_thresh to hit\_thresh\_pretrig

Adr 70: Rename nph\_thresh to hit\_thresh\_postdrift

Adr F0: Rename lyr\_thresh[2:0] to lyr\_thresh\_pretrig[2:0]

Adr F4: Remove dmb\_thresh from F4[8:6]

Adr F4: Add new signal pid\_thresh\_postdrift[3:0] to F4[9:6]

Adr F4: Move adjcfeb\_dist from F4[14:9] to F4[15:10]

Adr F4: Rename pid\_thresh to pid\_thresh\_pretrig

Add adr D8[12] jsm\_tckcnt\_ok JTAG PROM TCKs sent matches TCKs in trailer frame

Add adr D8[13] jsm\_end\_ok JTAG PROM FF end marker found where expected

Add adr D8[14] jsm\_header\_ok JTAG PROM BA begin marker found where expected

Add adr D8[15] jsm\_chain\_ok JTAG PROM Chain Block marker found where expected

Add adr DE[14:13] jtag\_sm\_vec[1:0] JSM JTAG signal state machine vector

Add adr E0[11:8] jsm\_prom\_sm\_vec[3:0] JSM PROM state machine vector

Add adr E0[14:12] jsm\_format\_sm\_vec[3:0] JSM Data format state machine vector

Add adr EA[15] jsm\_tckcnt\_ok JSM tckcnt added to board status

Header20: remove header20\_[12:10] lyr\_thresh[2:0]

Header20 remove header20\_[13] layer\_trig\_en

Header20 add header20\_[13:10] pid\_thresh\_postdrift[3:0]

Header41: add header41\_[13:11] lyr\_thresh\_pretrig[2:0]

Header41 add header41\_[14] layer\_trig\_en

New Counters:

Inserted 2 counters after counter at SubAdr[8]

SubAdr[9]CLCT: CLCT0 passed hit thresh but failed pid thresh after drift

SubAdr[10]CLCT: CLCT0 passed hit thresh but failed pid thresh after drift

Shifts all other counter addresses up by 2, i.e. old counter at SubAdr[9] moved to [11]

Change CLCT Processing Algorithm at bx11 to also require pid ≥ pid\_thresh\_postdrift

Version 06/03/2008

Modifies global\_reset and ttc\_resync behavior

Adds ability to send active feb flag to DMB at tmb alct\*clct matching, retains ability to send at pre-trig

Overlays ALCT rx data with normal scope channels to aid alct debugging

(1) Remove Adr A8[12] alct\_raw\_sync, wasn’t being used

(2) Add temporary alct structure error counters [48]-[52]

(3) Add Adr D0[6] cnt\_clear\_on\_resync clears VME counters [0]-[40] on ttc\_resync, default=0

(4) Add Adr D0[7] hdr\_clear\_on\_resync clears header counters [41]-[47] on ttc\_resync, default=1

(5) Update MPC frame format doc (reflects changes to 5/12/08 firmware)

(6) Added a startup state to the readout state machine to wait 1bx for buf\_q\_empty to update after a reset

(prevents machine from resuming a readout that was in progress at the time of a ttc\_resync)

(7) Add perr\_reset (one-shot) to Adr D0[15], removed ttc\_resync perr reset logic

(8) Block ttc\_resync from clearing resync event counter, requires vme-clear

(9) Adr2A[3] change ccb\_status\_oe default from 1 to 0, turns off backplane drivers to ccb

Added write-only bits to parallel non-decoded ccb commands:

Adr2A [12] vme\_evcntres Event counter reset || ccb\_evcntres

Adr2A[13] vme\_bcntres Bunch crossing reset || ccb\_bcntres

Adr2A14] vme\_bx0 Bx0 signal || ccb\_bx0

(10) Adr28[12] now contains global\_reset\_en=1 to enable resets on DLL lock-lost

(11) Header08[14] now contains clock\_lock\_lost

(12) AdrAC[14]=active\_feb\_src, 0=pretrig, 1=at tmb matching

(13) AdrB0[7:3]=clctf[4:0] active cfeb list at tmb matching

(14) Header23[4:0] active feb list is stored either at pretrig time or tmb match, depending active\_feb\_src

(15) Header23[14] now contains active\_feb\_src bit

(16) Header29[14] now contains hs\_layer\_trig (moved from header23[14])

(17) AdrCE[15]=scp\_ch\_overlay, 0=normal scope channels, 1=use debugging channel overlay

Current overlay assignments:

scp\_ch[71:0] = normal

scp\_ch[128:72] = scp\_alct\_rx[55:0]

assign scp\_alct\_rx[0] = alct\_active\_feb\_flag;

assign scp\_alct\_rx[1] = alct\_first\_valid;

assign scp\_alct\_rx[2] = alct\_first\_amu;

assign scp\_alct\_rx[4:3] = alct\_first\_quality[1:0];

assign scp\_alct\_rx[11:5] = alct\_first\_key[6:0];

assign scp\_alct\_rx[12] = alct\_second\_valid;

assign scp\_alct\_rx[13] = alct\_second\_amu;

assign scp\_alct\_rx[15:14] = alct\_second\_quality[1:0];

assign scp\_alct\_rx[22:16] = alct\_second\_key[6:0];

assign scp\_alct\_rx[27:23] = alct\_bxn[4:0];

assign scp\_alct\_rx[28] = #alct\_wr\_fifo;

assign scp\_alct\_rx[29] = alct\_first\_frame;

assign scp\_alct\_rx[43:30] = alct\_daq\_data[13:0];

assign scp\_alct\_rx[44] = alct\_lct\_special;

assign scp\_alct\_rx[45] = alct\_ddu\_special;

assign scp\_alct\_rx[46] = alct\_last\_frame;

assign scp\_alct\_rx[48:47] = alct\_seq\_status[1:0];

assign scp\_alct\_rx[50:49] = alct\_seu\_status[1:0];

assign scp\_alct\_rx[54:51] = alct\_reserved\_out[3:0];

assign scp\_alct\_rx[55] = alct\_cfg\_done;

Version 05/23/2008

(1) Adr B0[15:14] Add clock\_lock\_lost and sync\_er

Version 05/12/2008

(1) mpc alct\_bx0 and clct\_bx0 signals now bypass mpc\_tx\_delay

(2) Note: Adr86[13] default=0 uses ttc\_bx0, set it to 1 to use local bxn counter instead

Adr86[14] default=0 enables bx0 to mpc continuously, 1 blanks mpc frames unless triggering

(3) Adr CA[8] default changed to 1 to enable using reserved[3] signal from alct as alct\_bx0

(4) Adr90[15:14] now contains bx0 injector one-shots

Version 05/01/2008

(1) All scope channels replaced, see Scope Channel Assignments p50

(2) Header11 CLCT counter was behind by 1 event, fixed.

(3) Header22 Trigger source for alct\*clct matching is set even if match mode is off, fixed.

(4) Header28/29/30 ALCT data was latched n-bx early, leaving empty frames, fixed.

Version 04/29/2008

(1) ALCT signal reserved\_out[3] (alct-to-tmb) is now alct\_bx0

(2) Adr 68[02] renamed match\_pat\_trig\_en to alct\_match\_trig\_en

(3) Adr AC[5] hdr\_wr\_continuous should be set to 0 unless using l1a\_allow\_notmb=1 mode

(4) Adr AC[14] removed allow\_pretrig\_noflush bit

(5) Adr AE[11:0] sequencer state shortened from [14:0]

(6) Adr B2[7:4] Renamed clct\_width to clct\_window

(7) Adr BA[15:8] Now contains rpc bxn differences moved from Adr C4

(8) Adr C4 renamed to ADR\_RPC\_TBINS

Adr C4 added rpc tbins, tbins before pre-trigger, and rpc\_decouple [=0 to copy cfeb tbins]

(9) Adr CA[] new name ADR\_BX0\_DELAY, all new signals for bx0\_delay and bx0 source

(10) Adr D0[8] now contains counter lower-half / upper-half mux bit cnt\_adr\_lsb

Adr D0[14:9] now contains counter sub-address cnt\_adr[5:0]

Adr D0 Event counters replaced with new names and new sub-address channel numbers

(11) Adr F0[15:8] = clct\_throttle[7:0], default=0

(12) Adr F4[0]=clct\_blanking=1 (new default), prevented from setting to 0unless l1a\_allow\_notmb=1 or

tmb\_alct\_only=1

(13) Header21[14:11] Renamed clct\_width to clct\_window

(14) Header36 replaced to display rpc\_tbins and rpc\_pretrig, affects event-size calculation software,

rpc\_exists[1:0] deleted.

(15) Header41 now contains the enabled TMB matching modes

Version 02/5/2008

Added parity checking to cfeb and rpc raw hits RAMs for SEU detection

Added parity error bits to header27

Add drift\_delay to header29

Add alct pretrig window position to header28

Version 01/24/2008

Replaced entire L1A logic.

Replaced 8-buffer system with 2048 buffers.

Replaced readout stack with event queue.

Replaced lct\_quality.

Several VME addresses have changed:

(1) Adr AC[4] is now wr\_buf\_autoclr (formerly clct\_turbo).

Adr AC[5] 1=allow continuous header buffer writing for invalid triggers

Previously an unused bit. Default remains 0 until new trigger logic is ready.

(2) New buffer status signals now occupy Adrs 9E,A0,A2,A4,A6.

ADR\_BUF\_STAT0=9E

ADR\_BUF\_STAT1=A0

ADR\_BUF\_STAT2=A2

ADR\_BUF\_STAT3=A4

ADR\_BUF\_STAT4=A6

Old Adr A2 (alctfifo1) moved to A8 (old A8 was empty)

Old Adr A4 (alctfifo2) moved to AA (old AA was empty)

Old Adr A6[5:0] adjcfeb\_dist[5:0] moved to F4[14:9]

(3) Adr 72[13] is now fifo\_no\_raw\_hits [1=do not wait to store raw hits. A no\_daq mode.]

(4) Adr 74[15:13] is now l1a\_internal\_dly[2:0] (mostly for use by the simulator)

(5) Adr AE[14:11] signal names changed for buffer status

(6) Adrs B0, 78, 7A contain new CLCT internal format

(7) Header04[13] is now buf\_q\_ovf\_err, formerly stack\_ovf\_latch

Header05[14] is now buf\_stalled, formerly buf\_full

Header37,38,39, 40 changed for buffer status [some assignments are probably temporary]

Header25,26,27 contain new CLCT internal format

(8) Scope channels replaced

(9) Counters 1A, 1C, 1E changed, now count debug signal presence instead of time-outs

Version 10/11/2007

(1) CLCT raw hits CRC now stops at the frame before the DE0F marker due to DDUs failure to include the marker.

(2) ALCT raw hits CRC check stops at the frame before the DE0D marker, same reason.

Version 9/14/2007

(1) Header bug fixes in readout counter and lct-duplication flags

(2) New no-alct VME counter, channel 32/33, shifts subsequent channel numbers up 2

(3) ALCT DDR transmitter constraints minimize routing delays between alct\_rx\_clock and main clock.

Version 9/10/2007

(1) New raw hits readout header+trailer format replaces all previous header field assignments.

(2) New VME counters, channels 32 to 4C.

Version 7/10/2007

(1) Increase tmb.v-sequencer.v handshake time-out from 8bx to 15bx to prevent late alct\*clct matches

from being counted as discarded events when using higher than normal clct\_width values.

(2) Modify pre-trigger state machine to wait for alct\*clct matching (or clct-only) before re-arming for the next pre-trigger event to prevent writing current event to wrong header buffer when using higher than normal clct\_width values.

(3) Modify pre-trigger state machine to wait for active\_feb signal to return to 0 before the next pre-trigger event to avoid re-triggering on same event when using longer than normal triad\_persistence.

Version 7/05/2007

(1) Pattern-finder key layer shifted from ly3 back to ly2.

Ly3 pattern templates were flipped top-to-bottom to shift key layer to ly2, and flipped left-to-right to preserve bend direction.

(2) Adr A6 adjcfeb\_dist[5:0] is now 6-bits instead of 5 to allow dist=32 to span a full cfeb, default value remains 5hs.

(3) Adr F4 dmb\_thresh[3:0] default is now 4 to reduce spurious active feb signals to DMB

(4) CLCT Processing Algorithm description updated for current patterns

Version 6/21/2007

(1) Adr D4 bit 11 now contains wr\_usr\_jtag\_dis.

When wr\_usr\_jtag\_dis=1, write access to register adr\_usr\_jtag is blocked.

This allows parallel writes to jtag chains for selected alcts.

Adr 10 bit 14 indicates the state of wr\_usr\_jtag\_dis.

(2) Adrs A0, A8, AA, CA, CC are now obsolete.

Their FFs have been removed, and they read back 0000h.

(3) Adr A6 now contains adjcfeb[4:0] with a default value of 5 hstrips.

This replaces the function of mask registers A6, A8, and AA.

If there is n hstrip key on hs 0,1,2,3,4 on CFEBn, with hits ≥ hit\_thresh\_pretrig, then CFEBn-1 will be marked in the active\_feb list for DMB readout.

If there is a hstrip key on hs 31,30,29,28,27 on CFEBn, with hits ≥ hit\_thresh\_pretrig, then CFEBn+1 will be marked in the active\_feb list for DMB readout.

(4) Adr 6C, layer\_trig\_dly has been removed.

(5) Header05[12] now contains trigger source vector bit [8] (layer trigger)

Header05[13] hsds bit removed.

(6) Header16[14:11] now contains pid\_thresh[3:0] instead of ds\_thresh[2:0].

(7) References to hs\_thresh[2:0] have been changed to hit\_thresh\_pretrig[2:0].

References to ds\_thresh[2:0] have been removed.

(8) Adr 70, ds\_thresh[2:0] has been removed.

(9) Pattern ID numbers have been shifted from 0-to-8 to 2-to-10.

Pattern ID=1 now indicates a layer-trigger event.

Pattern ID=0 now indicates no pattern matches found.

(10) Adr F4, clct\_blanking=1 is the new default value

1. For TMB 2005 operation with up to 5 CFEBs. [↑](#footnote-ref-1)
2. For TMB 2013 operation with 7 DCFEBs. [↑](#footnote-ref-2)
3. NB: All external triggers (including scintillator and ALCT active FEB) create a dummy CLCT to force the TMB to read out raw hits. ALCT triggers can produce an LCT match if the ALCT active FEB is followed by an ALCT valid pattern flag. [↑](#footnote-ref-3)
4. Reserved cable input signals connect to ALCT FPGA user input pins [↑](#footnote-ref-4)
5. Copied from CFEB design: http://www.physics.ohio-state.edu/~gujh/works/cmpdata.html [↑](#footnote-ref-5)