Christof Schlaak

PhD Student

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cschlaak

I am a fourth year PhD student in Computer Science at the Institute for Computing Systems Architecture (ICSA) at the University of Edinburgh. I am working on a functional language for high-level synthesis of hardware accelerators. Microsoft Research has awarded me a PhD scholarship to carry out my studies.
I am generally interested in hardware design, compiler construction, rewrite-based optimization and functional languages.
Before my PhD studies, I completed my bachelor and master studies in computer science and worked as a researcher for two years.

Education

since 2018 **PhD Studies**, *University of Edinburgh*, Edinburgh, Scotland, United Kingdom
In my PhD studies, I want to automatically generate optimized FPGA hardware designs. Starting from a hardware-agnostic description in a high-level functional data parallel language, these applications are then compiled to platform-specific VHDL code. In this process, rewrite rules explore the design space and optimize the design's performance. This research is supervised by Christophe Dubach from McGill University and Aaron Smith (MSR).

2014–2016 **Master of Science in Computer Science**, *University of Oldenburg*, Oldenburg, Germany
My master studies had a focus on embedded systems, covering the following subjects: System level design for embedded systems (with SystemC), low energy system design, and testing technologies for embedded systems. I designed hardware in VHDL for FPGAs in a practical training and employed FPGAs in my master's thesis. Translated title of the master's thesis: 'Measurement based execution time and power analyses of synchronous dataflow graphs on FPGA based MPSoCs'. Another class taught me about fuzzy control and artificial neural networks. I developed a wearable computer based on Arduinos and an android app connected via bluetooth.

2011–2014 **Bachelor of Science in Computer Science**, *University of Oldenburg*, Oldenburg, Germany
Besides covering the basics of computer science, my bachelor studies were specialised on Embedded Systems and Microrobotics (ESMR) with courses about embedded systems, real-time operating systems, HW/SW system design, digital signal and image processing, electrical engineering, control engineering, microrobotics, and microsystems engineering. Translated title of the bachelor's thesis: 'Code generator for automatically configuring an execution time analysis framework for digital signal processing applications'.

Experience

2022–2023 **Web Chair**, *McGill University*, Montreal, Canada
I am the web chair of the International Symposium on Code Generation and Optimization (CGO'23).

2019–2020 **Teaching Assistant**, *University of Edinburgh*, Edinburgh, Scotland, United Kingdom
In the course 'Compiling Techniques', I supported students develop their C compilers.

2016–2018 **Researcher**, *OFFIS – Institute for Information Technology*, Oldenburg, Germany

Full-time work at OFFIS in the department Transportation, in the group Safety & Security Oriented Design Methods & Processes. I contributed to several international projects about intelligent strategies for testing and simulation with use-cases from the automotive domain. By designing simulation architectures and developing prototypes for these research projects, I improved my skills in C/C++, python, MATLAB/Simulink and many other tools. Furthermore, I gained experience in project management related tasks and in working together in a team.

2011–2016 **Tutor**, *University of Oldenburg*, Oldenburg, Germany

During my studies at the university I also worked as a tutor, teaching other students (one course per semester) in imperative and object-oriented programming with Java.

Awards

2018 **Microsoft Research Scholarship**, *University of Edinburgh*, Edinburgh, Scotland, United Kingdom

Microsoft Research has awarded me a research scholarship to carry out my PhD studies.

2017 **Excellent Graduation Work**, *University of Oldenburg*, Oldenburg, Germany

My master's thesis from 2016 was awarded 'Excellent Graduation Work'.

2014 **Federal State Scholarship**, *University of Oldenburg*, Oldenburg, Germany

I received a Federal State Scholarship in Lower Saxony for outstanding achievements in my bachelor studies.

Talks

Jun 2022 **Memory-Aware Functional IR for Higher-Level Synthesis of Accelerators** (Talk), *Conference on High-performance Embedded Architecture and Compilation (HiPEAC 2022)*, Budapest, Hungary

Jun 2022 **Optimizing Data Reshaping Operations in Functional IRs for High-Level Synthesis** (Talk), *23rd ACM SIGPLAN/SIGBED International Conference on Languages, Compilers, and Tools for Embedded Systems (LCTES 2022)*, San Diego, CA, United States

Jun 2022 **Optimizing Data Reshaping Operations in Functional IRs for High-Level Synthesis** (Talk), *Popco Seminar*, McGill University, Montreal, Canada

Apr 2022 **Functional Languages for High-Level Synthesis** (Invited Lecture), *Computer Architecture course (ECSE 425, Winter 2022) of Prof. Amin Emad*, McGill University, Montreal, Canada

Dec 2019 **High-level Synthesis of Neural Networks for FPGAs with Lift** (Poster), *Google's 7th Compiler and Programming Language Summit 2019*, Munich, Germany

Sep 2019 **Synthesising Neural Networks on FPGAs with Lift** (Talk), *Facebook AI Systems Faculty Summit 2019*, Facebook HQ, Menlo Park, CA, United States

Jul 2019 **High-level Synthesis of Neural Networks for FPGAs with Lift** (Poster), *Fifteenth International Summer School on Advanced Computer Architecture and Compilation for High-Performance and Embedded Systems (ACACES 2019)*, Fiuggi, Italy

Apr 2019 **High-level Synthesis of Neural Networks for FPGAs with Lift** (Lightning Talk and Poster), *HiPEAC Computer Systems Week (CSW Spring 2019)*, Edinburgh, Scotland, United Kingdom

Publications

2022 **C. Schlaak**, T. Juang and C. Dubach, *'Memory-Aware Functional IR for Higher-Level Synthesis of Accelerators'*, in ACM Transactions on Architecture and Code Optimization (TACO), Vol. 19, No. 2, Article 16

2018 B. Bauer, J.S. Becker, T. Peikenkamp, **C. Schlaak** and I. Stierand, *'Design Validation for Embedded Multi-core Systems in the Context of ISO 26262'*, in Workshop on Software Engineering for Applied Embedded RealTime Systems (SEERTS)

2017 **C. Schlaak**, M. Fakih and R. Stemmer, *'Power and Execution Time Measurement Methodology for SDF Applications on FPGA-based MPSoCs'*, in Proceedings of the Workshop on High Performance Energy Efficient Embedded Systems (HIP3ES). Collocated with HiPEAC 2017 Conference