U01: Basic Computing Elements of a Hypothetical Machine Architecture

CSci 430: Operating Systems

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Summer 2025

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Basic Elements of a Computing System

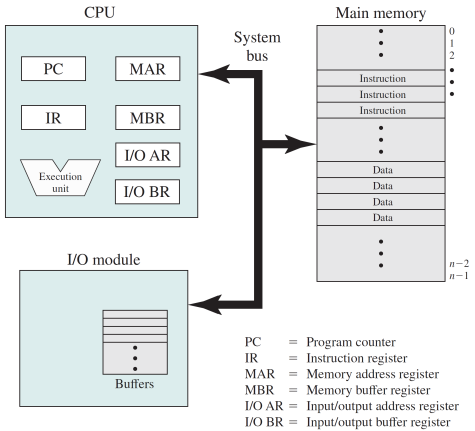

Figure 1: Basic components of a stored-program computer (Von Neumann architecture). (Stallings, 2018, pg.31)

Four elements of a computing system:

1. **Processor**: Controls the operation of the computer and performs data processing. **CPU** central processing unit.
2. **Main Memory**: Stores data and code. Typically volatile memory. **real memory** or **primary memory**.
3. **I/O Modules**: Move data between the computer and its external environment. Communication devices like NICs, or secondary storage like hard disks.
4. **System Bus**: Provides communication path between processors, main memory and I/O modules.

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Instruction Execution (The Fetch/Execute Cycle)

Instruction processing consists of two steps:

1. **Fetch next instruction**: The processor reads (**fetches**) one instruction from memory.
2. **Execute instruction**: The processor decodes the instruction and its arguments and **executes** the indicated operation.

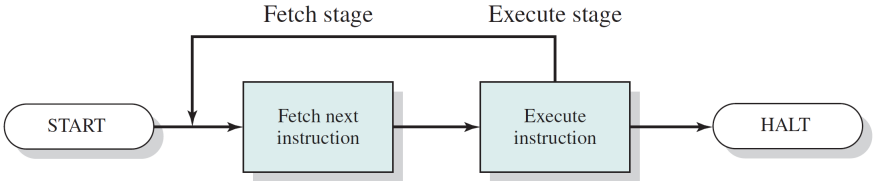

Figure 2: Basic fetch/execute instruction cycle for a hypothetical computer architecture. (Stallings, 2018, pg.33)

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Characteristics of a Hypothetical Machine Architecture

(a) Instruction format

(b) Integer format

Program counter (PC) = Address of instruction
Instruction register (IR) = Instruction being executed
Accumulator (AC) = Temporary storage

(c) Internal CPU registers

0001 = Load AC from memory
0010 = Store AC to memory
0101 = Add to AC from memory

(d) Partial list of opcodes

Figure 3: Example of a simple hypothetical machine architecture. (Stallings, 2018, pg.34)

- Instructions and data are both 16-bits (16-bit architecture).
- Instruction format (a) has 4 bit opcode, allows $2^4 = 16$ different opcodes.
- `PC` register holds next memory address to **fetch** into `IR`
- Opcode defines the operation to **execute**.
  - `AC` register holds one operand
  - Remaining 12 bits $2^{12} = 4096$ (4K) are 2nd operand memory address
- Machine only supports **signed integer** operations (b)
  - Uses simple sign/magnitude format, 1 sign bit and 15 bits for magnitude

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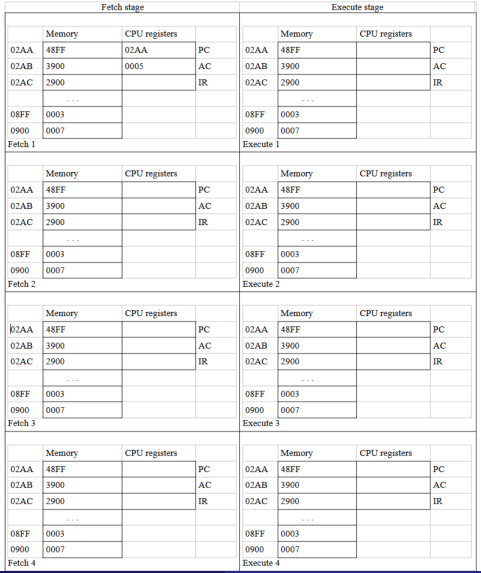
Hypothetical Machine Example Problems 1



Fetch stage

	Memory	CPU registers	
02AA	48FF	02AA	PC
02AB	3900	0005	AC
02AC	2900		IR
	...		
08FF	0003		
0900	0007		

Fetch 1

	Memory	CPU registers	
02AA	48FF		PC
02AB	3900		AC
02AC	2900		IR
	...		
08FF	0003		
0900	0007		

Fetch 2

	Memory	CPU registers	
02AA	48FF		PC
02AB	3900		AC
02AC	2900		IR
	...		
08FF	0003		
0900	0007		

Fetch 3

	Memory	CPU registers	
02AA	48FF		PC
02AB	3900		AC
02AC	2900		IR
	...		
08FF	0003		
0900	0007		

Fetch 4

Execute stage

	Memory	CPU registers	
02AA	48FF		PC
02AB	3900		AC
02AC	2900		IR
	...		
08FF	0003		
0900	0007		

Execute 1

	Memory	CPU registers	
02AA	48FF		PC
02AB	3900		AC
02AC	2900		IR
	...		
08FF	0003		
0900	0007		

Execute 2

	Memory	CPU registers	
02AA	48FF		PC
02AB	3900		AC
02AC	2900		IR
	...		
08FF	0003		
0900	0007		

Execute 3

	Memory	CPU registers	
02AA	48FF		PC
02AB	3900		AC
02AC	2900		IR
	...		
08FF	0003		
0900	0007		

Execute 4

Hex	Bin	Opcode
1	0001	LOAD
2	0010	STOR
3	0011	MUL
4	0100	SUB
5	0101	ADD
6	0110	JMP
7	0111	JMPZ
8	1000	JMPN

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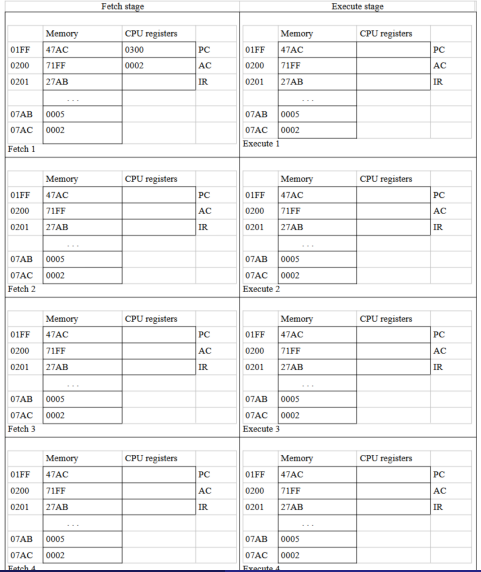
Hypothetical Machine Example Problems 2



Hex	Bin	Opcode
1	0001	LOAD
2	0010	STOR
3	0011	MUL
4	0100	SUB
5	0101	ADD
6	0110	JMP
7	0111	JMPZ
8	1000	JMPN

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Hypothetical Machine Example Problems 3

Fetch stage				Execute stage			
	Memory	CPU registers			Memory	CPU registers	
01AB	5941	01AB	PC	01AB	5941		PC
01AC	2940	8003	AC	01AC	2940		AC
01AD	61AB		IR	01AD	61AB		IR
	...				...		
0940	0000			0940	0000		
0941	0002			0941	0002		
Fetch 1				Execute 1			
	Memory	CPU registers			Memory	CPU registers	
01AB	5941		PC	01AB	5941		PC
01AC	2940		AC	01AC	2940		AC
01AD	61AB		IR	01AD	61AB		IR
	...				...		
0940	0000			0940	0000		
0941	0002			0941	0002		
Fetch 2				Execute 2			
	Memory	CPU registers			Memory	CPU registers	
01AB	5941		PC	01AB	5941		PC
01AC	2940		AC	01AC	2940		AC
01AD	61AB		IR	01AD	61AB		IR
	...				...		
0940	0000			0940	0000		
0941	0002			0941	0002		
Fetch 3				Execute 3			
	Memory	CPU registers			Memory	CPU registers	
01AB	5941		PC	01AB	5941		PC
01AC	2940		AC	01AC	2940		AC
01AD	61AB		IR	01AD	61AB		IR
	...				...		
0940	0000			0940	0000		
0941	0002			0941	0002		
Fetch 4				Execute 4			

Hex	Bin	Opcode
1	0001	LOAD
2	0010	STOR
3	0011	MUL
4	0100	SUB
5	0101	ADD
6	0110	JMP
7	0111	JMPZ
8	1000	JMPN

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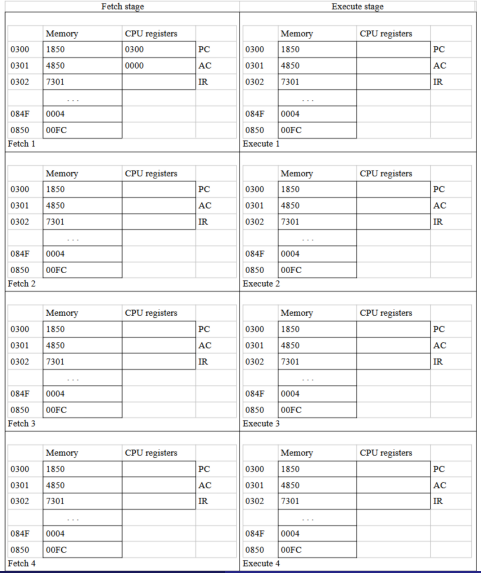
Hypothetical Machine Example Problems 4



Fetch stage

	Memory	CPU registers	
0300	1850	0300	PC
0301	4850	0000	AC
0302	7301		IR
	...		
084F	0004		
0850	00FC		

Fetch 1

	Memory	CPU registers	
0300	1850		PC
0301	4850		AC
0302	7301		IR
	...		
084F	0004		
0850	00FC		

Fetch 2

	Memory	CPU registers	
0300	1850		PC
0301	4850		AC
0302	7301		IR
	...		
084F	0004		
0850	00FC		

Fetch 3

	Memory	CPU registers	
0300	1850		PC
0301	4850		AC
0302	7301		IR
	...		
084F	0004		
0850	00FC		

Fetch 4

Execute stage

	Memory	CPU registers	
0300	1850		PC
0301	4850		AC
0302	7301		IR
	...		
084F	0004		
0850	00FC		

Execute 1

	Memory	CPU registers	
0300	1850		PC
0301	4850		AC
0302	7301		IR
	...		
084F	0004		
0850	00FC		

Execute 2

	Memory	CPU registers	
0300	1850		PC
0301	4850		AC
0302	7301		IR
	...		
084F	0004		
0850	00FC		

Execute 3

	Memory	CPU registers	
0300	1850		PC
0301	4850		AC
0302	7301		IR
	...		
084F	0004		
0850	00FC		

Execute 4

Hex	Bin	Opcode
1	0001	LOAD
2	0010	STOR
3	0011	MUL
4	0100	SUB
5	0101	ADD
6	0110	JMP
7	0111	JMPZ
8	1000	JMPN

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Bibliography

Stallings, W. (2018). *Operating systems: Internals and design principles* (ninth). Pearson Education.

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