Using ADC on AlphBot

Embedded Real-Time Systems (ERTS) Lab
Indian Institute of Technology, Bombay

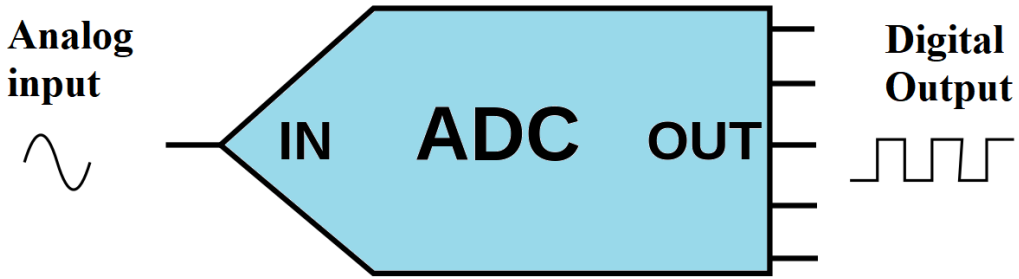
Agenda for Discussion

1. Analog to Digital Conversion
   - What is an ADC
   - Need for ADC
   - ADC of ATmega328p
2. Coding ADC
   - ADC Initialization
   - ADCSRA
   - ADCSRB
   - ADMUX
   - Algorithm for ADC

What is an ADC

What is an ADC

- Converts a signal from analog (continuous) to digital (discrete) form



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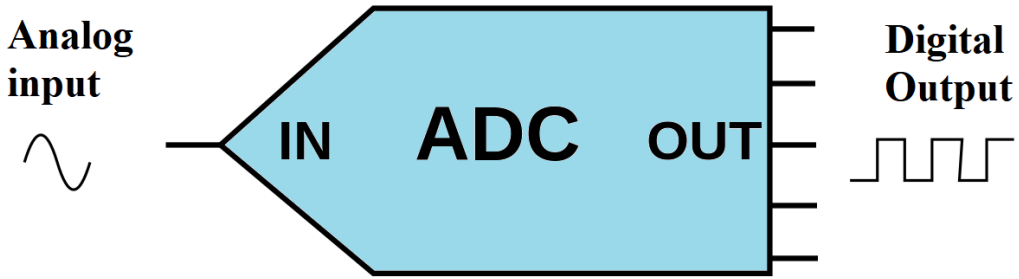

- It samples the input signal periodically

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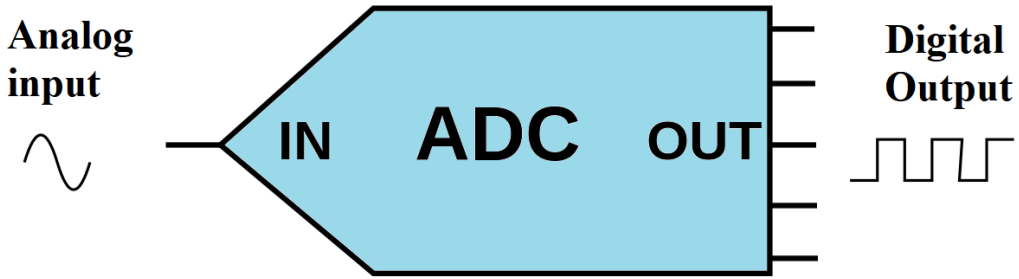

- It samples the input signal periodically
- Conversion involves quantization of the input signal and encoding.

Need for ADC

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- IR Proximity sensors

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- Temperature sensor

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- Temperature sensor
- White line sensors

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- Battery voltage sensor

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- etc..

In-Built ADC of ATmega328p

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- Minimum voltage change (Vref / 2^n)

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- Selectable 1.1V ADC Reference Voltage

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- Free Running or Single Conversion Mode

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In-Built ADC of ATmega328p

- 10-bit Resolution
- Minimum voltage change (Vref / 2^n)
- 65 to 260 μs Conversion Time
- 6 Multiplexed Single Ended Input Channels
- Optional Left Adjustment for ADC Result Readout
- 0 - VCC ADC Input Voltage Range
- Temperature sensor input channel
- Selectable 1.1V ADC Reference Voltage
- Free Running or Single Conversion Mode
- Interrupt on ADC Conversion Complete
- ADC pins are available on PortC

ADC Initialization

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- To Program ADC, we have to initialize some register before use it.

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2. ADCSRB - ADC Control and Status Register B
3. ADMUX - ADC Multiplexer Selection Register

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These registers are:

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4. DIDR0 - Digital Input Disable Register 0

ADC Initialization

- To Program ADC, we have to initialize some register before use it.

  These registers are:

  1. ADCSRA - ADC Control and Status Register A
  2. ADCSRB - ADC Control and Status Register B
  3. ADMUX - ADC Multiplexer Selection Register
  4. DIDR0 - Digital Input Disable Register 0

- All these Registers are 8 Bit

ADCSRA- ADC Control and Status Register A

This register is Used to control ADC operation

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Bit	Symbol	Description	Bit Value

ADCSRA- ADC Control and Status Register A

This register is Used to control ADC operation

Bit	Symbol	Description	Bit Value
7	ADEN	ADC Enable	

ADCSRA- ADC Control and Status Register A

This register is Used to control ADC operation

Bit	Symbol	Description	Bit Value
7	ADEN	ADC Enable	1

ADCSRA- ADC Control and Status Register A

This register is Used to control ADC operation

Bit	Symbol	Description	Bit Value
7	ADEN	ADC Enable	1
6	ADSC	ADC Start Conversion	

ADCSRA- ADC Control and Status Register A

This register is Used to control ADC operation

Bit	Symbol	Description	Bit Value
7	ADEN	ADC Enable	1
6	ADSC	ADC Start Conversion	0

ADCSRA- ADC Control and Status Register A

This register is Used to control ADC operation

Bit	Symbol	Description	Bit Value
7	ADEN	ADC Enable	1
6	ADSC	ADC Start Conversion	0
5	ADATE	ADC Auto Trigger Enable	

ADCSRA- ADC Control and Status Register A

This register is Used to control ADC operation

Bit	Symbol	Description	Bit Value
7	ADEN	ADC Enable	1
6	ADSC	ADC Start Conversion	0
5	ADATE	ADC Auto Trigger Enable	0

ADCSRA- ADC Control and Status Register A

This register is Used to control ADC operation

Bit	Symbol	Description	Bit Value
7	ADEN	ADC Enable	1
6	ADSC	ADC Start Conversion	0
5	ADATE	ADC Auto Trigger Enable	0
4	ADIF	ADC Interrupt Flag	

ADCSRA- ADC Control and Status Register A

This register is Used to control ADC operation

Bit	Symbol	Description	Bit Value
7	ADEN	ADC Enable	1
6	ADSC	ADC Start Conversion	0
5	ADATE	ADC Auto Trigger Enable	0
4	ADIF	ADC Interrupt Flag	0

ADCSRA- ADC Control and Status Register A

This register is Used to control ADC operation

Bit	Symbol	Description	Bit Value
7	ADEN	ADC Enable	1
6	ADSC	ADC Start Conversion	0
5	ADATE	ADC Auto Trigger Enable	0
4	ADIF	ADC Interrupt Flag	0
3	ADIE	ADC Interrupt Enable	

ADCSRA- ADC Control and Status Register A

This register is Used to control ADC operation

Bit	Symbol	Description	Bit Value
7	ADEN	ADC Enable	1
6	ADSC	ADC Start Conversion	0
5	ADATE	ADC Auto Trigger Enable	0
4	ADIF	ADC Interrupt Flag	0
3	ADIE	ADC Interrupt Enable	0

ADCSRA- ADC Control and Status Register A

This register is Used to control ADC operation

Bit	Symbol	Description	Bit Value
7	ADEN	ADC Enable	1
6	ADSC	ADC Start Conversion	0
5	ADATE	ADC Auto Trigger Enable	0
4	ADIF	ADC Interrupt Flag	0
3	ADIE	ADC Interrupt Enable	0
2	ADPS2	ADC Prescaler Select Bits	

ADCSRA- ADC Control and Status Register A

This register is Used to control ADC operation

Bit	Symbol	Description	Bit Value
7	ADEN	ADC Enable	1
6	ADSC	ADC Start Conversion	0
5	ADATE	ADC Auto Trigger Enable	0
4	ADIF	ADC Interrupt Flag	0
3	ADIE	ADC Interrupt Enable	0
2	ADPS2	ADC Prescaler Select Bits	1

ADCSRA- ADC Control and Status Register A

This register is Used to control ADC operation

Bit	Symbol	Description	Bit Value
7	ADEN	ADC Enable	1
6	ADSC	ADC Start Conversion	0
5	ADATE	ADC Auto Trigger Enable	0
4	ADIF	ADC Interrupt Flag	0
3	ADIE	ADC Interrupt Enable	0
2	ADPS2	ADC Prescaler Select Bits	1
1	ADPS1	ADC Prescaler Select Bits	

ADCSRA- ADC Control and Status Register A

This register is Used to control ADC operation

Bit	Symbol	Description	Bit Value
7	ADEN	ADC Enable	1
6	ADSC	ADC Start Conversion	0
5	ADATE	ADC Auto Trigger Enable	0
4	ADIF	ADC Interrupt Flag	0
3	ADIE	ADC Interrupt Enable	0
2	ADPS2	ADC Prescaler Select Bits	1
1	ADPS1	ADC Prescaler Select Bits	1

ADCSRA- ADC Control and Status Register A

This register is Used to control ADC operation

Bit	Symbol	Description	Bit Value
7	ADEN	ADC Enable	1
6	ADSC	ADC Start Conversion	0
5	ADATE	ADC Auto Trigger Enable	0
4	ADIF	ADC Interrupt Flag	0
3	ADIE	ADC Interrupt Enable	0
2	ADPS2	ADC Prescaler Select Bits	1
1	ADPS1	ADC Prescaler Select Bits	1
0	ADPS0	ADC Prescaler Select Bits	

ADCSRA- ADC Control and Status Register A

This register is Used to control ADC operation

Bit	Symbol	Description	Bit Value
7	ADEN	ADC Enable	1
6	ADSC	ADC Start Conversion	0
5	ADATE	ADC Auto Trigger Enable	0
4	ADIF	ADC Interrupt Flag	0
3	ADIE	ADC Interrupt Enable	0
2	ADPS2	ADC Prescaler Select Bits	1
1	ADPS1	ADC Prescaler Select Bits	1
0	ADPS0	ADC Prescaler Select Bits	0

ADCSRA- ADC Control and Status Register A

This register is Used to control ADC operation

Bit	Symbol	Description	Bit Value
7	ADEN	ADC Enable	1
6	ADSC	ADC Start Conversion	0
5	ADATE	ADC Auto Trigger Enable	0
4	ADIF	ADC Interrupt Flag	0
3	ADIE	ADC Interrupt Enable	0
2	ADPS2	ADC Prescaler Select Bits	1
1	ADPS1	ADC Prescaler Select Bits	1
0	ADPS0	ADC Prescaler Select Bits	0

ADCSRA- ADC Control and Status Register A

This register is Used to control ADC operation

Bit	Symbol	Description	Bit Value
7	ADEN	ADC Enable	1
6	ADSC	ADC Start Conversion	0
5	ADATE	ADC Auto Trigger Enable	0
4	ADIF	ADC Interrupt Flag	0
3	ADIE	ADC Interrupt Enable	0
2	ADPS2	ADC Prescaler Select Bits	1
1	ADPS1	ADC Prescaler Select Bits	1
0	ADPS0	ADC Prescaler Select Bits	0

ADCSRA = 0x86

ADCSRA- ADC Control and Status Register A

This register is Used to control ADC operation

Bit	Symbol	Description	Bit Value
7	ADEN	ADC Enable	1
6	ADSC	ADC Start Conversion	0
5	ADATE	ADC Auto Trigger Enable	0
4	ADIF	ADC Interrupt Flag	0
3	ADIE	ADC Interrupt Enable	0
2	ADPS2	ADC Prescaler Select Bits	1
1	ADPS1	ADC Prescaler Select Bits	1
0	ADPS0	ADC Prescaler Select Bits	0

ADCSRA = 0x86

ADC Prescaler Selection Bit

ADC Prescaler Selection Bit

Table 26-5. ADC Prescaler Selections

ADPS2	ADPS1	ADPS0	Division Factor
0	0	0	2
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

ADC clock frequency = (F_CPU / Division Factor)
= 16000000 / 64
= 250 kHz

ADCSRB- ADC Control and Status Register B

This register is Used to control ADC operation

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This register is Used to control ADC operation

Bit	Symbol	Description	Bit Value

ADCSRB- ADC Control and Status Register B

This register is Used to control ADC operation

Bit	Symbol	Description	Bit Value
7	-	Reserved Bit	

ADCSRB- ADC Control and Status Register B

This register is Used to control ADC operation

Bit	Symbol	Description	Bit Value
7	-	Reserved Bit	-

ADCSRB- ADC Control and Status Register B

This register is Used to control ADC operation

Bit	Symbol	Description	Bit Value
7	-	Reserved Bit	-
6	ACME	Analog Comparator Multiplexer Enable	

ADCSRB- ADC Control and Status Register B

This register is Used to control ADC operation

Bit	Symbol	Description	Bit Value
7	-	Reserved Bit	-
6	ACME	Analog Comparator Multiplexer Enable	0

ADCSRB- ADC Control and Status Register B

This register is Used to control ADC operation

Bit	Symbol	Description	Bit Value
7	-	Reserved Bit	-
6	ACME	Analog Comparator Multiplexer Enable	0
5	-	Reserved Bit	-
4	-	Reserved Bit	-

ADCSRB- ADC Control and Status Register B

This register is Used to control ADC operation

Bit	Symbol	Description	Bit Value
7	-	Reserved Bit	-
6	ACME	Analog Comparator Multiplexer Enable	0
5	-	Reserved Bit	-
4	-	Reserved Bit	-
3	-	Reserved Bit	

ADCSRB- ADC Control and Status Register B

This register is Used to control ADC operation

Bit	Symbol	Description	Bit Value
7	-	Reserved Bit	-
6	ACME	Analog Comparator Multiplexer Enable	0
5	-	Reserved Bit	-
4	-	Reserved Bit	-
3	-	Reserved Bit	-

ADCSRB- ADC Control and Status Register B

This register is Used to control ADC operation

Bit	Symbol	Description	Bit Value
7	-	Reserved Bit	-
6	ACME	Analog Comparator Multiplexer Enable	0
5	-	Reserved Bit	-
4	-	Reserved Bit	-
3	-	Reserved Bit	-
2	ADTS2	ADC Auto Trigger Source Bits	0
1	ADTS1	ADC Auto Trigger Source Bits	0
0	ADTS0	ADC Auto Trigger Source Bits	0

ADCSRB- ADC Control and Status Register B

This register is Used to control ADC operation

Bit	Symbol	Description	Bit Value
7	-	Reserved Bit	-
6	ACME	Analog Comparator Multiplexer Enable	0
5	-	Reserved Bit	-
4	-	Reserved Bit	-
3	-	Reserved Bit	-
2	ADTS2	ADC Auto Trigger Source Bits	0
1	ADTS1	ADC Auto Trigger Source Bits	0
0	ADTS0	ADC Auto Trigger Source Bits	0

ADCSRB- ADC Control and Status Register B

This register is Used to control ADC operation

Bit	Symbol	Description	Bit Value
7	-	Reserved Bit	-
6	ACME	Analog Comparator Multiplexer Enable	0
5	-	Reserved Bit	-
4	-	Reserved Bit	-
3	-	Reserved Bit	-
2	ADTS2	ADC Auto Trigger Source Bits	0
1	ADTS1	ADC Auto Trigger Source Bits	0
0	ADTS0	ADC Auto Trigger Source Bits	0

ADCSRB = 0x00

ADCSRB- ADC Control and Status Register B

This register is Used to control ADC operation

Bit	Symbol	Description	Bit Value
7	-	Reserved Bit	-
6	ACME	Analog Comparator Multiplexer Enable	0
5	-	Reserved Bit	-
4	-	Reserved Bit	-
3	-	Reserved Bit	-
2	ADTS2	ADC Auto Trigger Source Bits	0
1	ADTS1	ADC Auto Trigger Source Bits	0
0	ADTS0	ADC Auto Trigger Source Bits	0

ADCSRB = 0x00

ADMUX - ADC Multiplexer Selection Register

This register is Used to select ADC channel

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Bit	Symbol	Description	Bit Value

ADMUX - ADC Multiplexer Selection Register

This register is Used to select ADC channel

Bit	Symbol	Description	Bit Value
7	REFS1	Reference Selection Bit	

ADMUX - ADC Multiplexer Selection Register

This register is Used to select ADC channel

Bit	Symbol	Description	Bit Value
7	REFS1	Reference Selection Bit	0
6	REFS0	Reference Selection Bit	1

ADMUX - ADC Multiplexer Selection Register

This register is Used to select ADC channel

Bit	Symbol	Description	Bit Value
7	REFS1	Reference Selection Bit	0
6	REFS0	Reference Selection Bit	1
5	ADLAR	ADC Left Adjust Result	

ADMUX - ADC Multiplexer Selection Register

This register is Used to select ADC channel

Bit	Symbol	Description	Bit Value
7	REFS1	Reference Selection Bit	0
6	REFS0	Reference Selection Bit	1
5	ADLAR	ADC Left Adjust Result	1

ADMUX - ADC Multiplexer Selection Register

This register is Used to select ADC channel

Bit	Symbol	Description	Bit Value
7	REFS1	Reference Selection Bit	0
6	REFS0	Reference Selection Bit	1
5	ADLAR	ADC Left Adjust Result	1
4	-	Reserved Bit	

ADMUX - ADC Multiplexer Selection Register

This register is Used to select ADC channel

Bit	Symbol	Description	Bit Value
7	REFS1	Reference Selection Bit	0
6	REFS0	Reference Selection Bit	1
5	ADLAR	ADC Left Adjust Result	1
4	-	Reserved Bit	0
3	MUX3	ADC Channel selection bit-3	0
2	MUX2	ADC Channel selection bit-2	0
1	MUX1	ADC Channel selection bit-1	0
0	MUX0	ADC Channel selection bit-0	0

ADMUX - ADC Multiplexer Selection Register

This register is Used to select ADC channel

Bit	Symbol	Description	Bit Value
7	REFS1	Reference Selection Bit	0
6	REFS0	Reference Selection Bit	1
5	ADLAR	ADC Left Adjust Result	1
4	-	Reserved Bit	0
3	MUX3	ADC Channel selection bit-3	0
2	MUX2	ADC Channel selection bit-2	0
1	MUX1	ADC Channel selection bit-1	0
0	MUX0	ADC Channel selection bit-0	0

ADMUX - ADC Multiplexer Selection Register

This register is Used to select ADC channel

Bit	Symbol	Description	Bit Value
7	REFS1	Reference Selection Bit	0
6	REFS0	Reference Selection Bit	1
5	ADLAR	ADC Left Adjust Result	1
4	-	Reserved Bit	0
3	MUX3	ADC Channel selection bit-3	0
2	MUX2	ADC Channel selection bit-2	0
1	MUX1	ADC Channel selection bit-1	0
0	MUX0	ADC Channel selection bit-0	0

ADMUX = 0x30

ADMUX - ADC Multiplexer Selection Register

This register is Used to select ADC channel

Bit	Symbol	Description	Bit Value
7	REFS1	Reference Selection Bit	0
6	REFS0	Reference Selection Bit	1
5	ADLAR	ADC Left Adjust Result	1
4	-	Reserved Bit	0
3	MUX3	ADC Channel selection bit-3	0
2	MUX2	ADC Channel selection bit-2	0
1	MUX1	ADC Channel selection bit-1	0
0	MUX0	ADC Channel selection bit-0	0

ADMUX = 0x30

ADC Reference Voltage Selection Bit

ADC Reference Voltage Selection Bit

REFS1	REFS0	Voltage Reference Selection
0	0	AREF, internal V_{REF} turned off
0	1	AV_{CC} with external capacitor at AREF pin
1	0	Reserved
1	1	Internal 1.1V voltage reference with external capacitor at AREF pin

ADC Left Adjustment Bit

ADC Left Adjustment Bit

The ADC Data Register – ADCL and ADCH

ADLAR = 0

Bit	15	14	13	12	11	10	9	8	
	–	–	–	–	–	–	ADC9	ADC8	ADCH
	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0	ADCL
	7	6	5	4	3	2	1	0	
Read/Write	R	R	R	R	R	R	R	R	
	R	R	R	R	R	R	R	R	
Initial Value	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	

ADLAR = 1

Bit	15	14	13	12	11	10	9	8	
	ADC9	ADC8	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADCH
	ADC1	ADC0	–	–	–	–	–	–	ADCL
	7	6	5	4	3	2	1	0	
Read/Write	R	R	R	R	R	R	R	R	
	R	R	R	R	R	R	R	R	
Initial Value	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	

MUX3:0 Channel Selection

MUX3:0 Channel Selection

MUX3:0	ADC Channel
0000	ADC0
0001	ADC1
0010	ADC2
0011	ADC3
0100	ADC4
0101	ADC5
0110	ADC6
0111	ADC7

MUX3:0 Channel Selection

MUX3:0	ADC Channel
0000	ADC0
0001	ADC1
0010	ADC2
0011	ADC3
0100	ADC4
0101	ADC5
0110	ADC6
0111	ADC7

Algorithm for ADC

Algorithm for ADC

1. Configure the PORT as Input and deactivate the pull-up resistors

Algorithm for ADC

1. Configure the PORT as Input and deactivate the pull-up resistors
2. Initialize the ADC registers

Algorithm for ADC

1. Configure the PORT as Input and deactivate the pull-up resistors
2. Initialize the ADC registers
3. Set/reset the appropriate Channel Selection bits: MUX[3:0]

Algorithm for ADC

1. Configure the PORT as Input and deactivate the pull-up resistors
2. Initialize the ADC registers
3. Set/reset the appropriate Channel Selection bits: MUX[3:0]
4. Start ADC conversion by setting the ADSC bit in ADCSRA register

Algorithm for ADC

1. Configure the PORT as Input and deactivate the pull-up resistors
2. Initialize the ADC registers
3. Set/reset the appropriate Channel Selection bits: MUX[3:0]
4. Start ADC conversion by setting the ADSC bit in ADCSRA register
5. Use polling method to check:

Algorithm for ADC

1. Configure the PORT as Input and deactivate the pull-up resistors
2. Initialize the ADC registers
3. Set/reset the appropriate Channel Selection bits: MUX[3:0]
4. Start ADC conversion by setting the ADSC bit in ADCSRA register
5. Use polling method to check:
    1. ADIF bit - it updates from 0 to 1 once ADC conversion complete
    OR

Algorithm for ADC

1. Configure the PORT as Input and deactivate the pull-up resistors
2. Initialize the ADC registers
3. Set/reset the appropriate Channel Selection bits: MUX[3:0]
4. Start ADC conversion by setting the ADSC bit in ADCSRA register
5. Use polling method to check:
    1. ADIF bit - it updates from 0 to 1 once ADC conversion complete
    OR
    2. ADSC bit - it updates from 1 to 0 once ADC conversion completes

Algorithm for ADC

1. Configure the PORT as Input and deactivate the pull-up resistors
2. Initialize the ADC registers
3. Set/reset the appropriate Channel Selection bits: MUX[3:0]
4. Start ADC conversion by setting the ADSC bit in ADCSRA register
5. Use polling method to check:
    1. ADIF bit - it updates from 0 to 1 once ADC conversion complete
    OR
    2. ADSC bit - it updates from 1 to 0 once ADC conversion completes
6. Read the converted data from ADC data registers

Algorithm for ADC

1. Configure the PORT as Input and deactivate the pull-up resistors
2. Initialize the ADC registers
3. Set/reset the appropriate Channel Selection bits: MUX[3:0]
4. Start ADC conversion by setting the ADSC bit in ADCSRA register
5. Use polling method to check:
    1. ADIF bit - it updates from 0 to 1 once ADC conversion complete
    OR
    2. ADSC bit - it updates from 1 to 0 once ADC conversion completes
6. Read the converted data from ADC data registers
7. Reset the ADIF bit, MUX[3:0] bits to their default values used during the initialization of ADC. Note: To clear ADIF bit, one must write logical one to the bit

Algorithm for ADC

1. Configure the PORT as Input and deactivate the pull-up resistors
2. Initialize the ADC registers
3. Set/reset the appropriate Channel Selection bits: MUX[3:0]
4. Start ADC conversion by setting the ADSC bit in ADCSRA register
5. Use polling method to check:
    1. ADIF bit - it updates from 0 to 1 once ADC conversion complete
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6. Read the converted data from ADC data registers
7. Reset the ADIF bit, MUX[3:0] bits to their default values used during the initialization of ADC. Note: To clear ADIF bit, one must write logical one to the bit
8. Repeat the steps from 3, for next ADC conversion

Algorithm for ADC

1. Configure the PORT as Input and deactivate the pull-up resistors
2. Initialize the ADC registers
3. Set/reset the appropriate Channel Selection bits: MUX[3:0]
4. Start ADC conversion by setting the ADSC bit in ADCSRA register
5. Use polling method to check:
    1. ADIF bit - it updates from 0 to 1 once ADC conversion complete
    OR
    2. ADSC bit - it updates from 1 to 0 once ADC conversion completes
6. Read the converted data from ADC data registers
7. Reset the ADIF bit, MUX[3:0] bits to their default values used during the initialization of ADC. Note: To clear ADIF bit, one must write logical one to the bit
8. Repeat the steps from 3, for next ADC conversion

Thank You!

Post your queries on: support@e-yantra.org