KIET GROUP OF INSTITUTIONS

LAB MANUAL

COMPUTER ORGANIZATION AND ARCHITECTURE (KCS 352)

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BATCH: 01

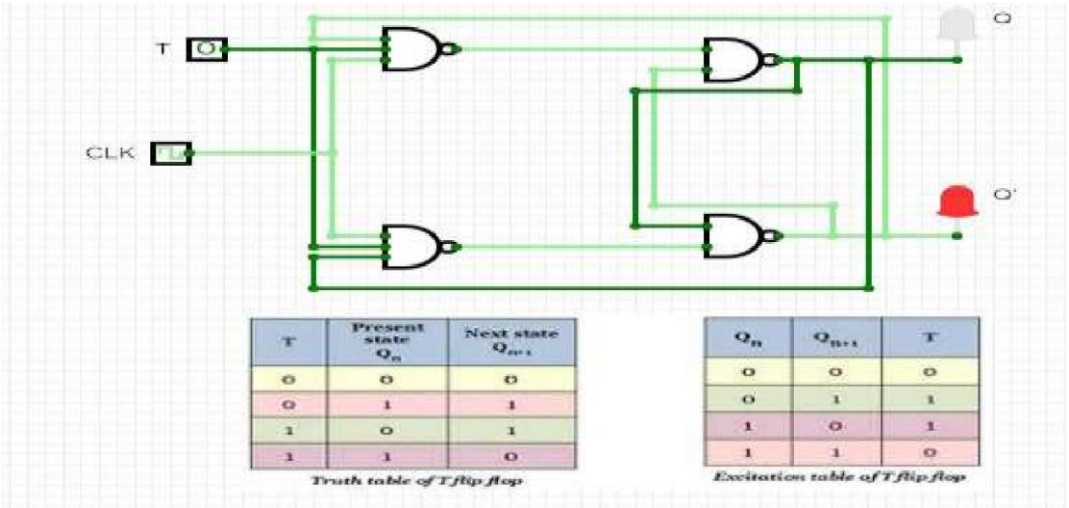
Objective: Verify the excitation tables of various FLIP-FLOPS.

Theory:

In electronics, a flip-flop or latch is a circuit that has two stable states and can be used to store state information – a bistable multivibrator. The circuit can be made to change state by signals applied to one or more control inputs and will have one or two outputs.

T- FLIP FLOP

The T flip-flop is also called toggle flip-flop. It is **a change of the JK flipflop**. The T flip flop is received by relating both inputs of a JK flip-flop. The T flipflop is received by relating the inputs 'J' and 'K'. When T = 0, both AND gates are disabled.



T	Present state Q_n	Next state Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

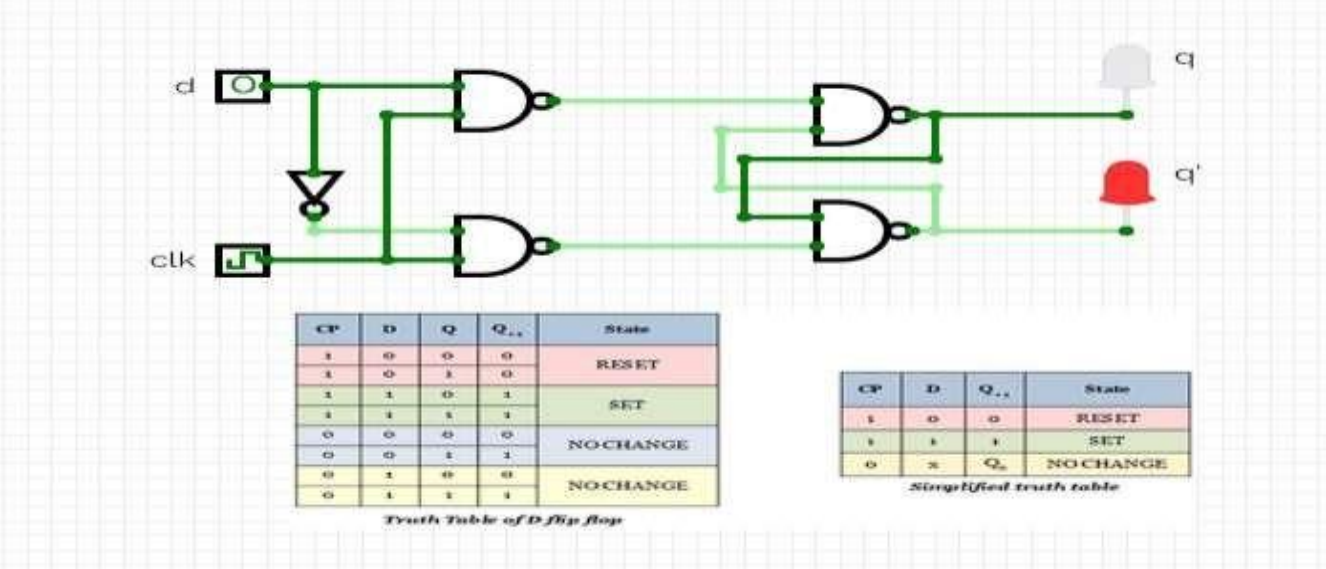
Truth table of T flip flop

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Excitation table of T flip flop

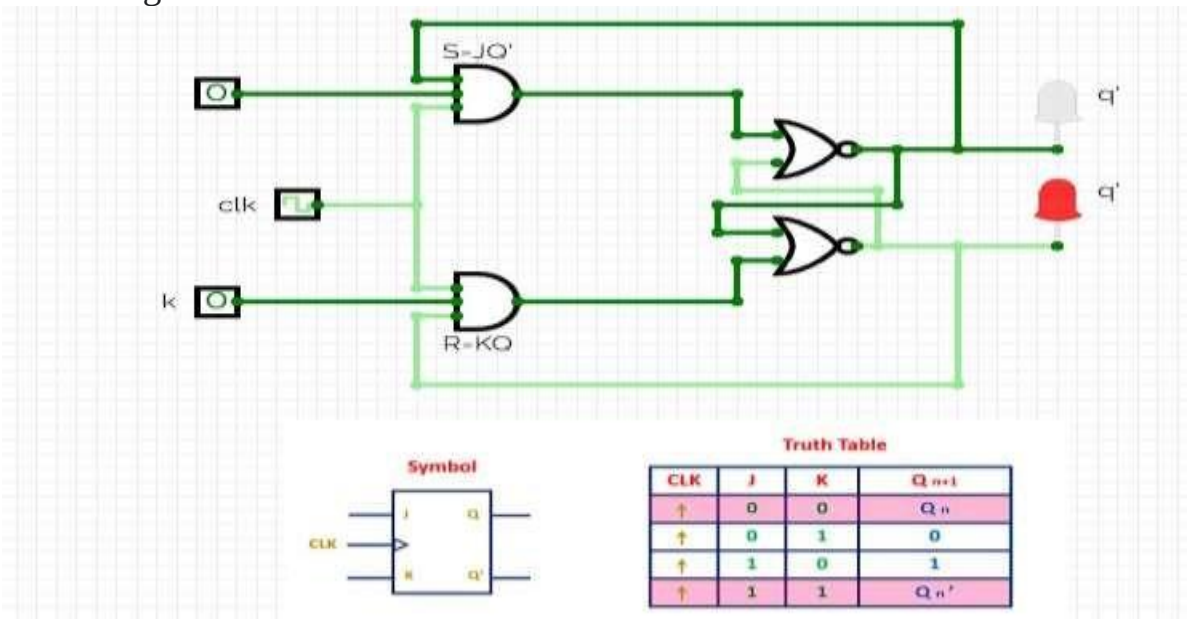
D-FLIP FLOP

A D (or Delay) Flip Flop (Figure 1) is **a digital electronic circuit used to delay the change of state of its output signal (Q) until the next rising edge of a clock timing input signal occurs**.



JK FLIP FLOP

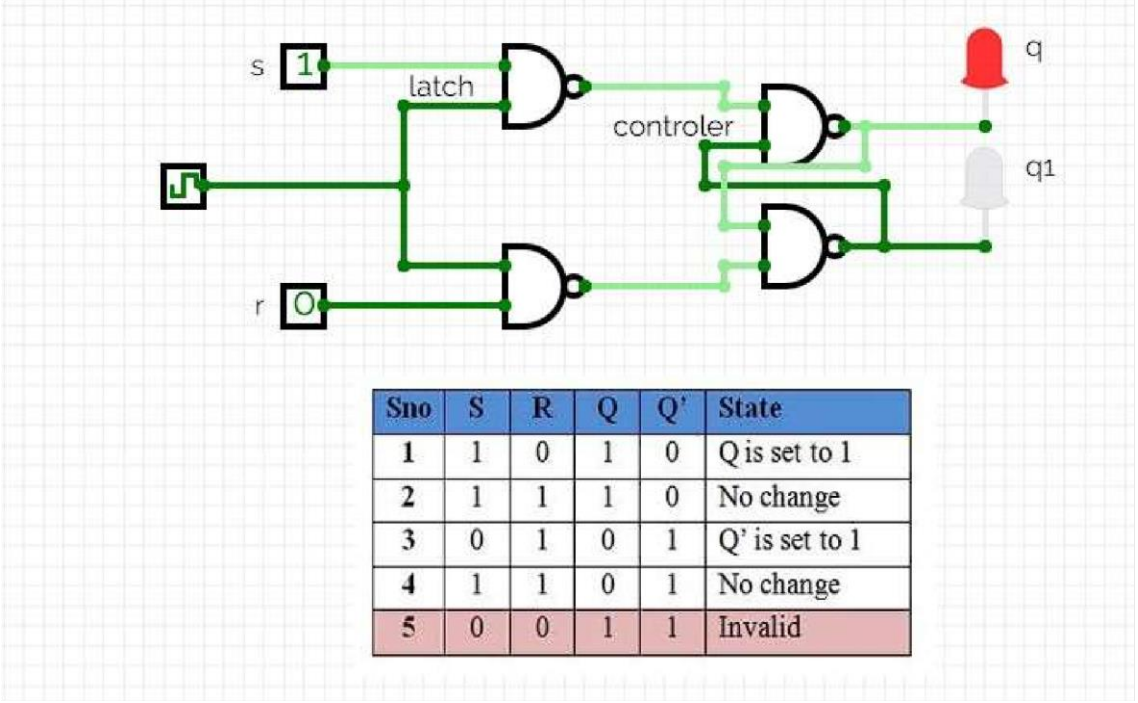
A J-K flip-flop is nothing more than **an S-R flip-flop with an added layer of feedback**. This feedback selectively enables one of the two set/reset inputs so that they cannot both carry an active signal to the multivibrator circuit, thus eliminating the invalid condition.



SR-FLIP FLOP

SR flip-flop is **a gated set-reset flip-flop**. The S and R inputs control the state of the flip-flop when the clock pulse goes from LOW to HIGH. The flip-flop will

not change until the clock pulse is on a rising edge. When both S and R are simultaneously HIGH, it is uncertain whether the outputs will be HIGH or LOW.



Sno	S	R	Q	Q'	State
1	1	0	1	0	Q is set to 1
2	1	1	1	0	No change
3	0	1	0	1	Q' is set to 1
4	1	1	0	1	No change
5	0	0	1	1	Invalid