Chapter - 4

FET BIASING

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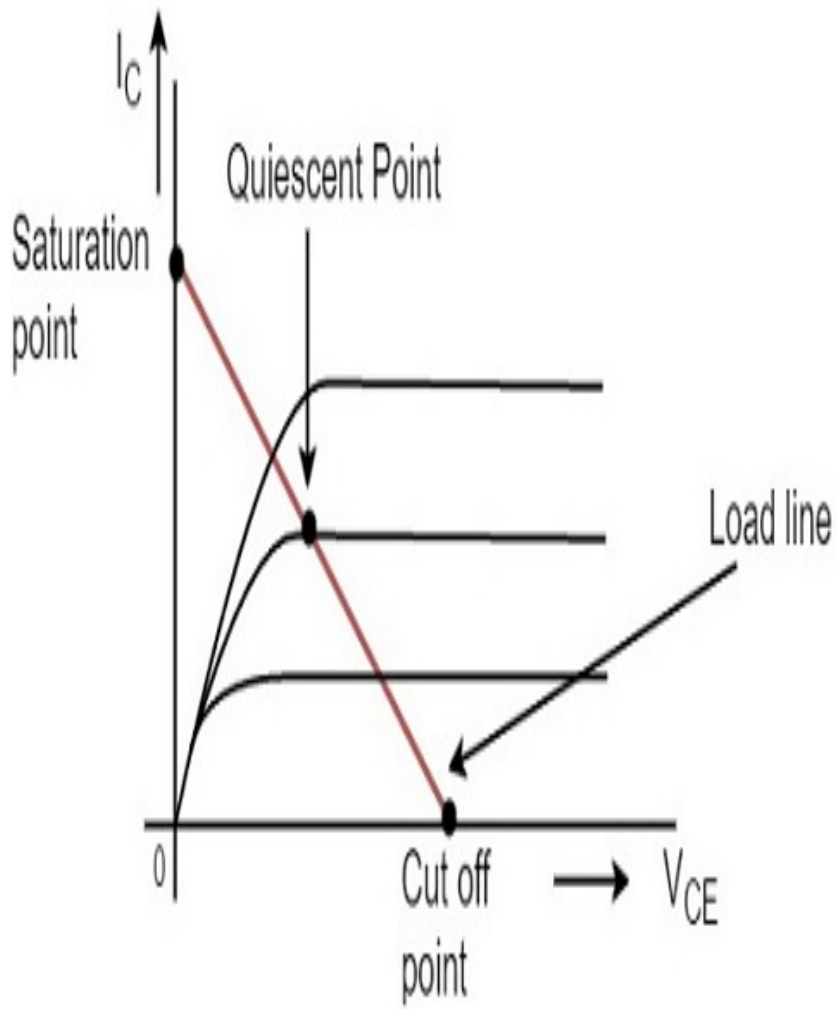
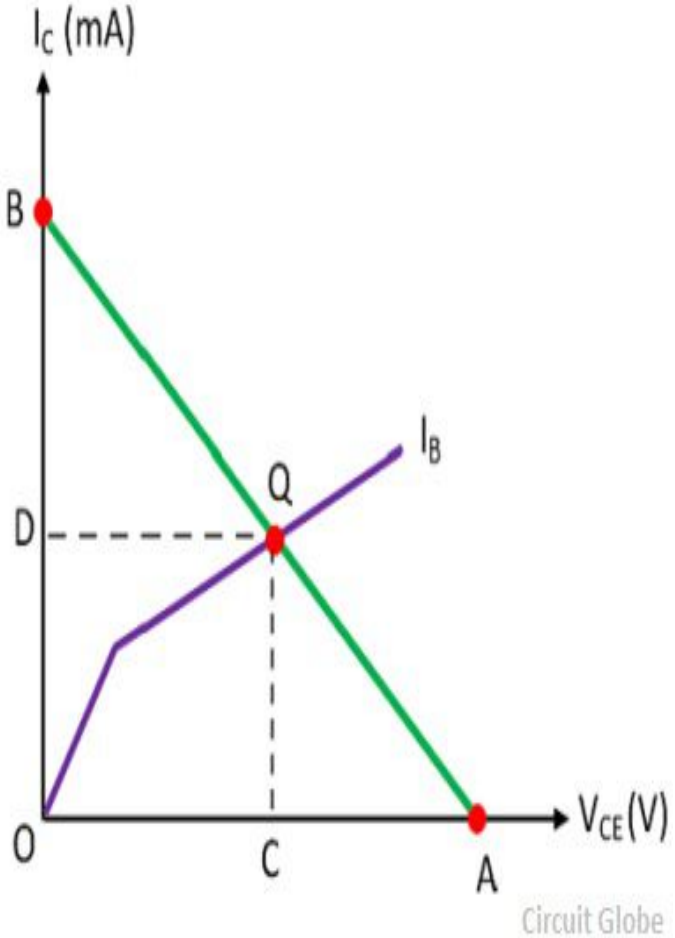
When a line is drawn joining the saturation and cut of points, such a line can be called as Load line. This line, when drawn over the output characteristic curve, makes contact at a point called as Operating point.



a **load line** is a **line** drawn on the characteristic curve, a graph of the current vs. the voltage in a nonlinear device like a diode or transistor. It represents the constraint put on the voltage and current in the nonlinear device by the external circuit.



Introduction of Biasing

The analysis or design of a transistor amplifier requires knowledge of both the dc and ac response of the system. In fact, the amplifier increases the strength of a weak signal by transferring the energy from the applied DC source to the weak input ac signal The analysis or design of any electronic amplifier therefore has two components:

- The dc portion and
- The ac portion During the design stage, the choice of parameters for the required dc levels will affect the ac response.

Biasing: Application of dc voltages to establish a fixed level of current and voltage.

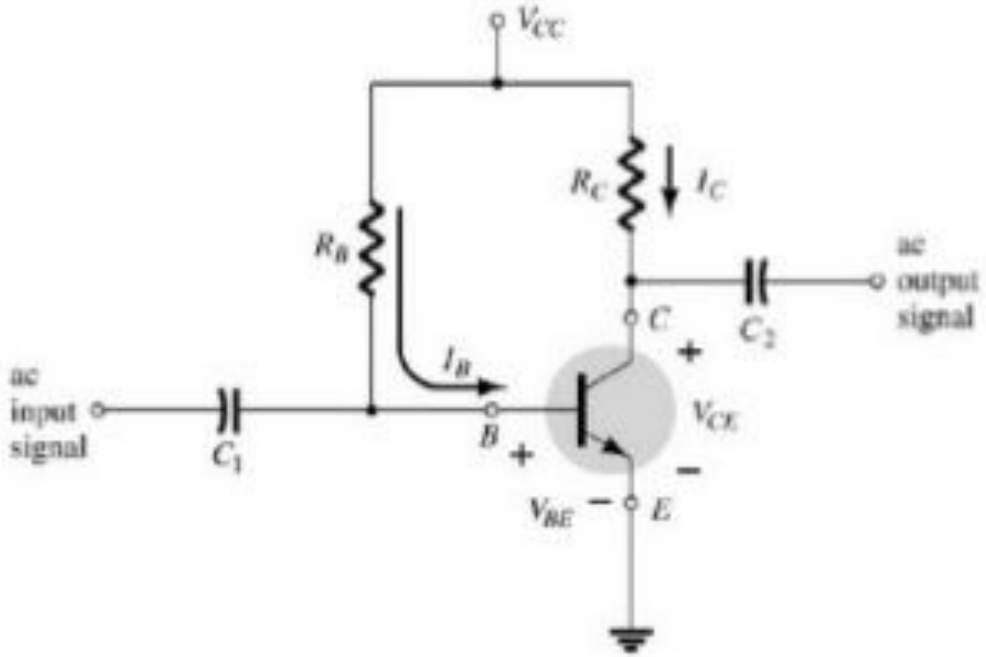
Purpose of DC biasing circuit:

- To turn the device “ON”
- To place it in operation in the region of its characteristic where the device operates most linearly .
- Proper biasing circuit which it operate in linear region and circuit have centered Q-point or midpoint biased
- Improper biasing cause Improper biasing cause
- Distortion in the output signal
- Produce limited or clipped at output signal

Types of DC Biasing Circuits

- Fixed-bias circuit
- Emitter-stabilized bias circuit
- Collector-emitter loop
- Voltage divider bias circuit
- DC bias with voltage feedback

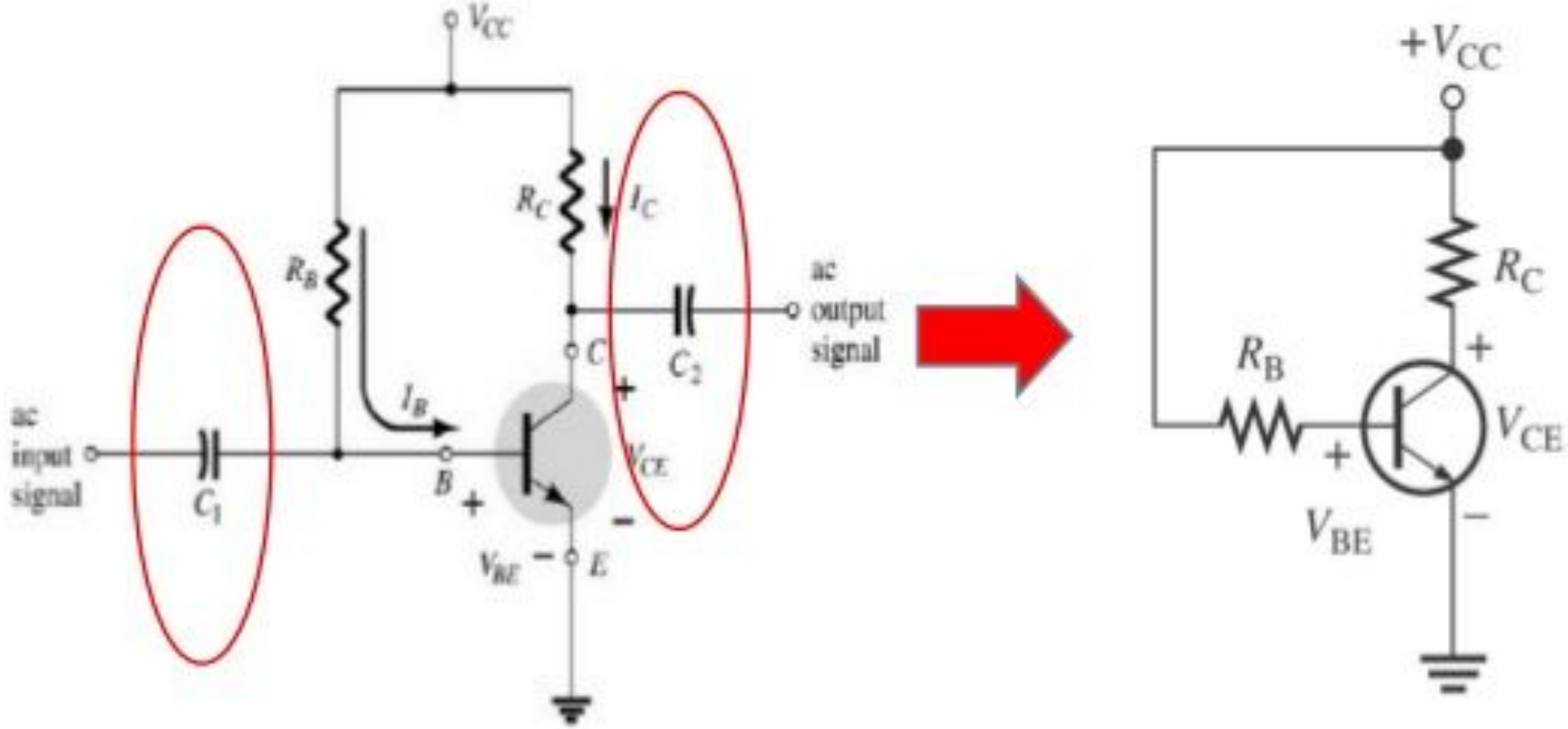
Fixed Base Bias Circuit



- This is common emitter (CE) configuration
- 1st step: Locate capacitors and replace them with an open circuit
- 2nd step: Locate 2 main loops which;
  - BE loop
  - CE loop

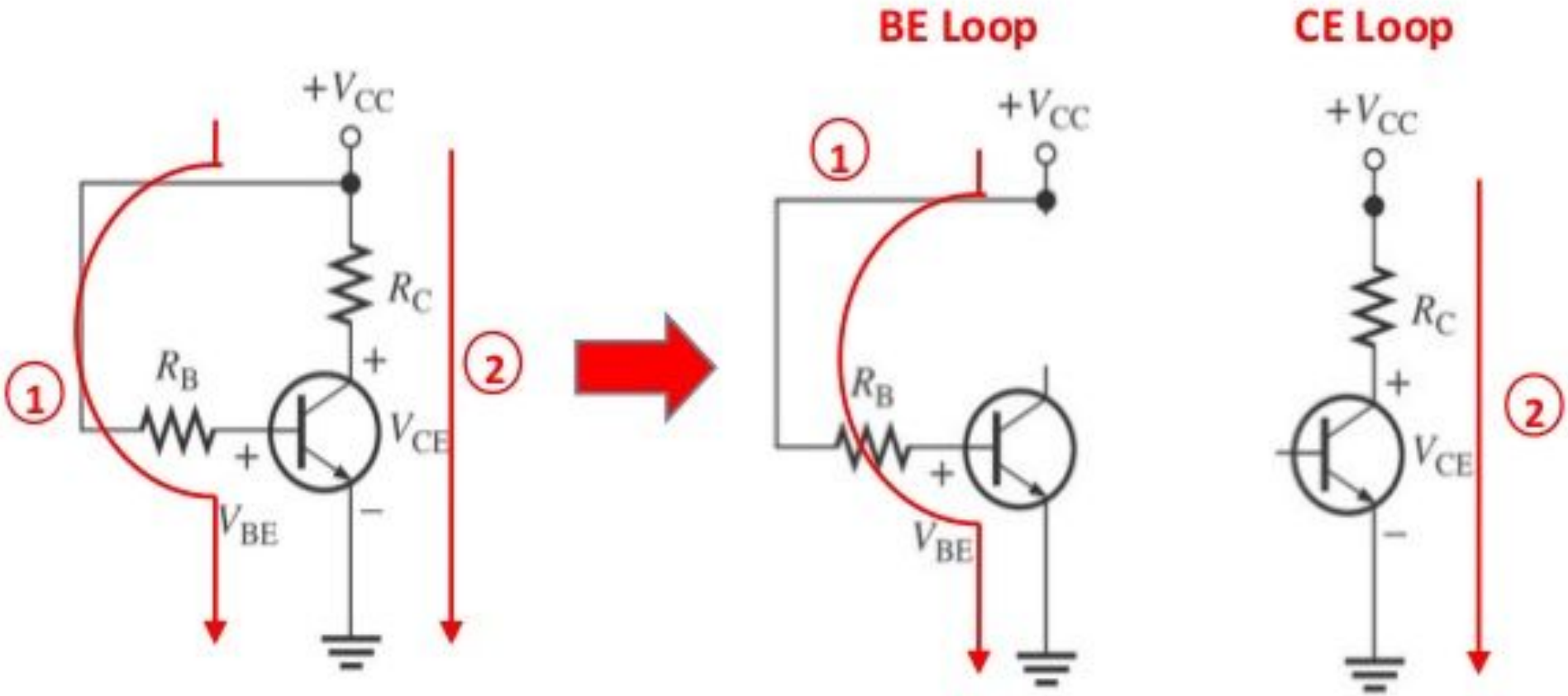
Fixed Base Bias Circuit

- 1st step: Locate capacitors and replace them with an open circuit

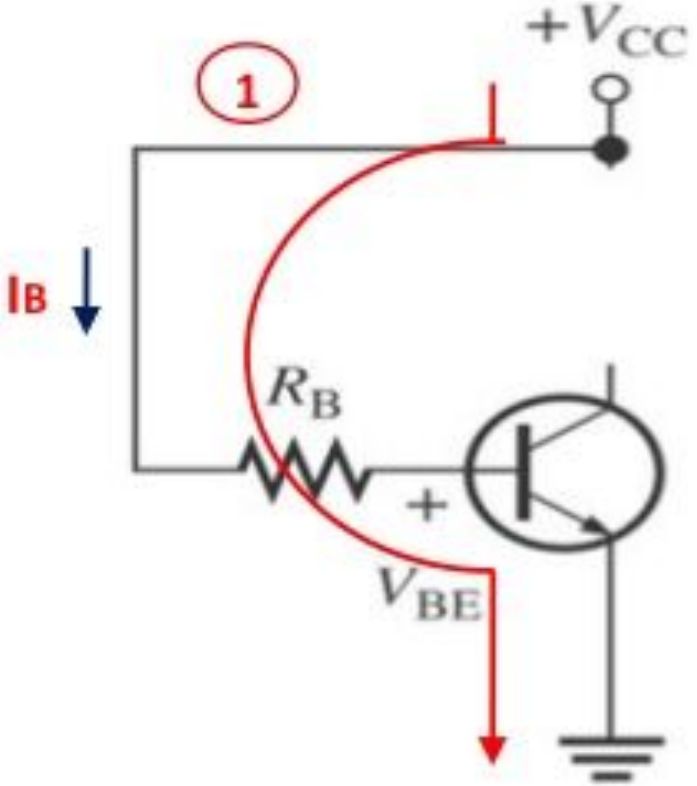


Fixed Base Bias Circuit

- 2nd step: Locate 2 main loops.



Fixed Base Bias Circuit

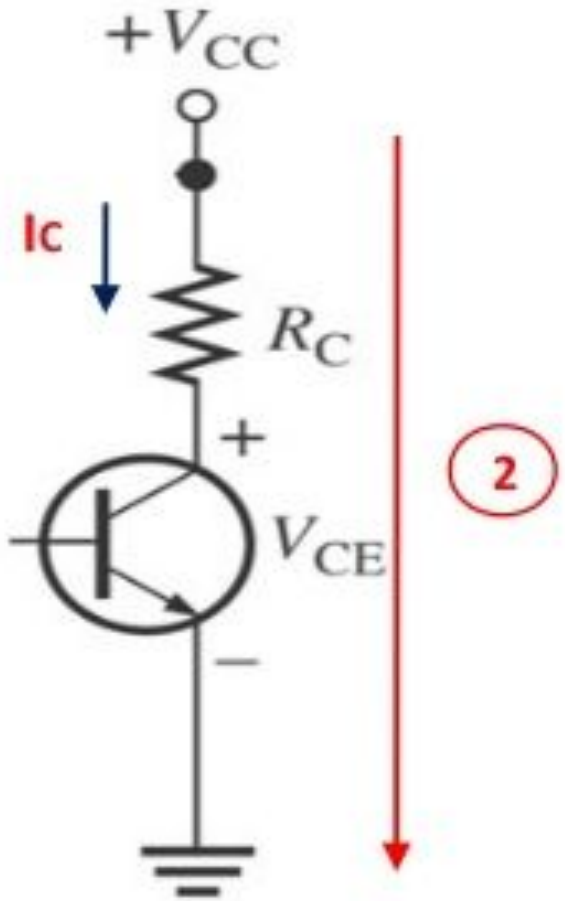


- BE Loop Analysis
- $V_{CC} - I_B R_B - V_{BE} = 0$

Therefore,

$I_B = (V_{CC} - V_{BE})/R_B$

Fixed Base Bias Circuit



CE Loop Analysis

$V_{CC} - I_C R_C - V_{CE} = 0$

$V_{CE} = V_{CC} - I_C R_C$

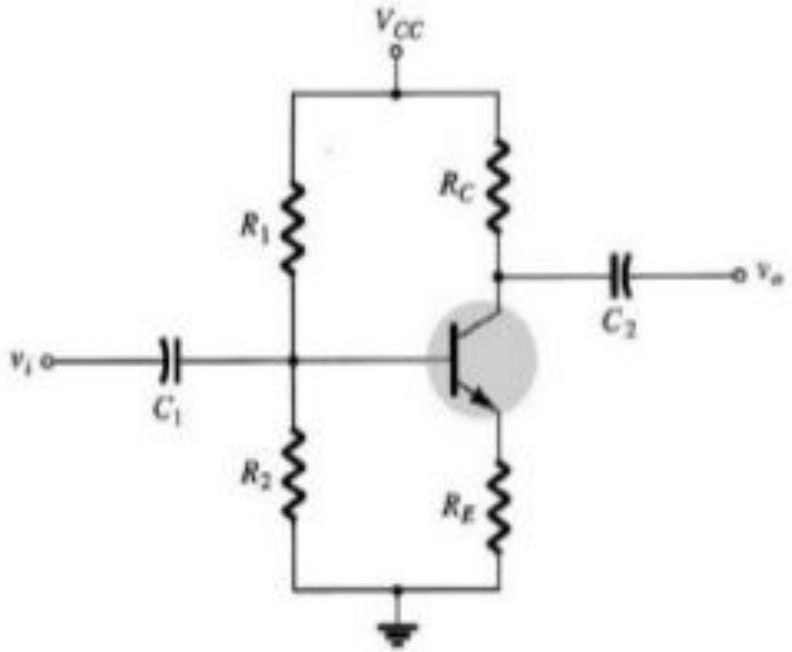
But $I_C = \beta I_B$

$V_{CE} = \beta_{DC}((V_{CC} - V_{BE})/R_B)$

Fixed Base Bias Circuit

- DISADVANTAGE
  - Unstable – because it is too dependent on β and produce width change of Q-point
  - For improved bias stability , add emitter resistor to dc bias.

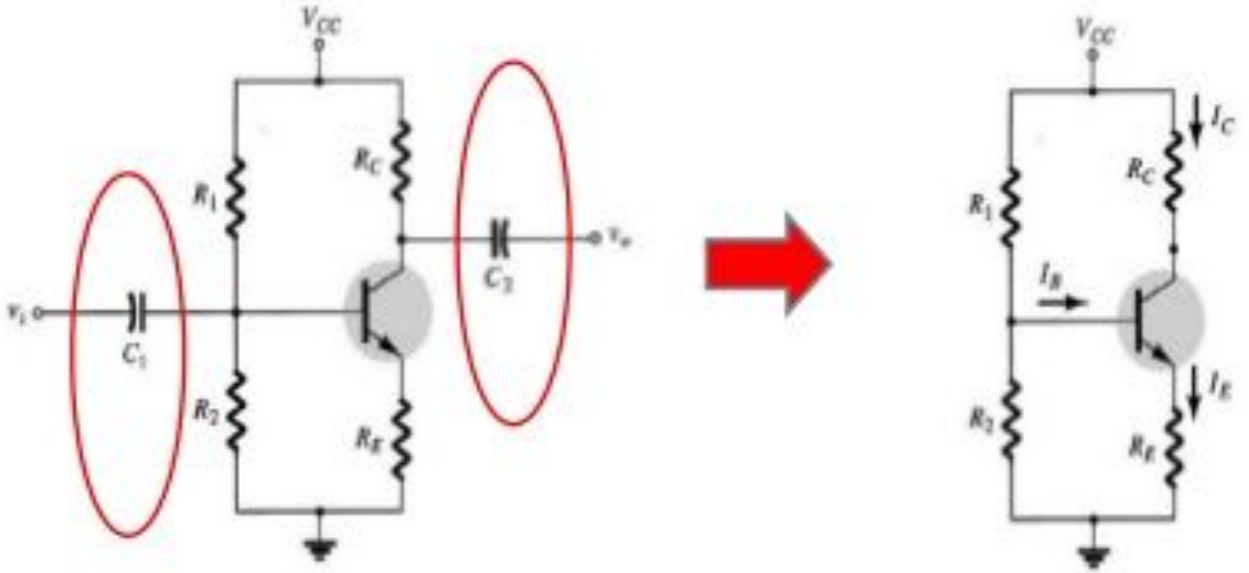
Voltage Divider Bias Circuit



- Provides good Q-point stability with a single polarity supply voltage
- 1st step: Locate capacitors and replace them with an open circuit
- 2nd step: Simplified circuit using Thevenin Theorem
- 3rd step: Locate 2 main loops which;
  - BE loop
  - CE loop

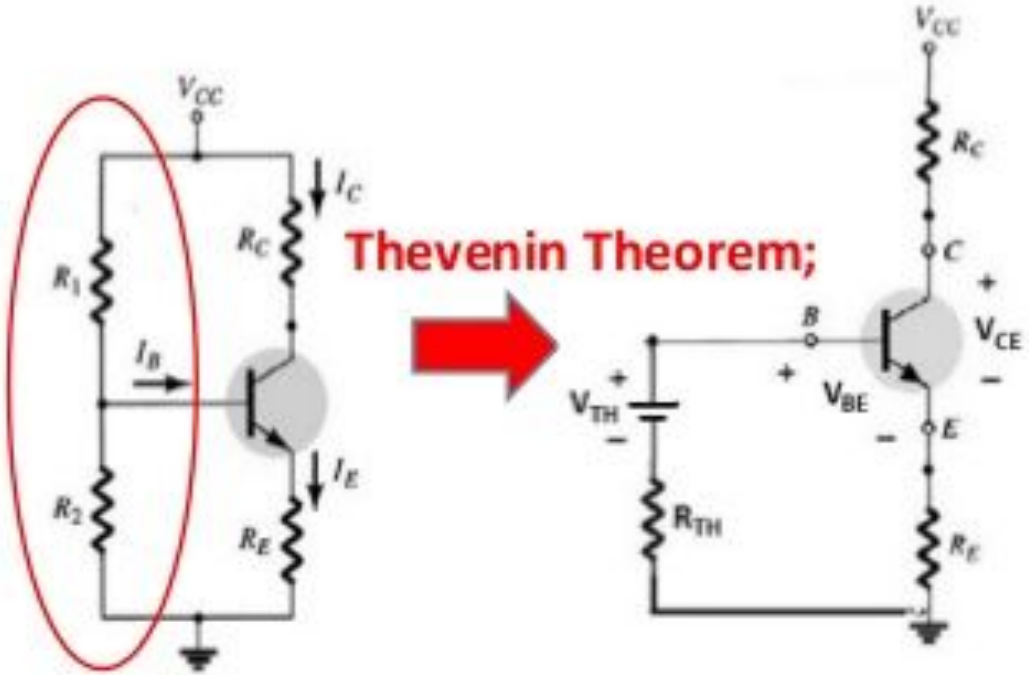
Voltage Divider Bias Circuit

- 1st step: Locate capacitors and replace them with an open circuit



Voltage Divider Bias Circuit

- 2nd step: : Simplified circuit using **Thevenin Theorem**



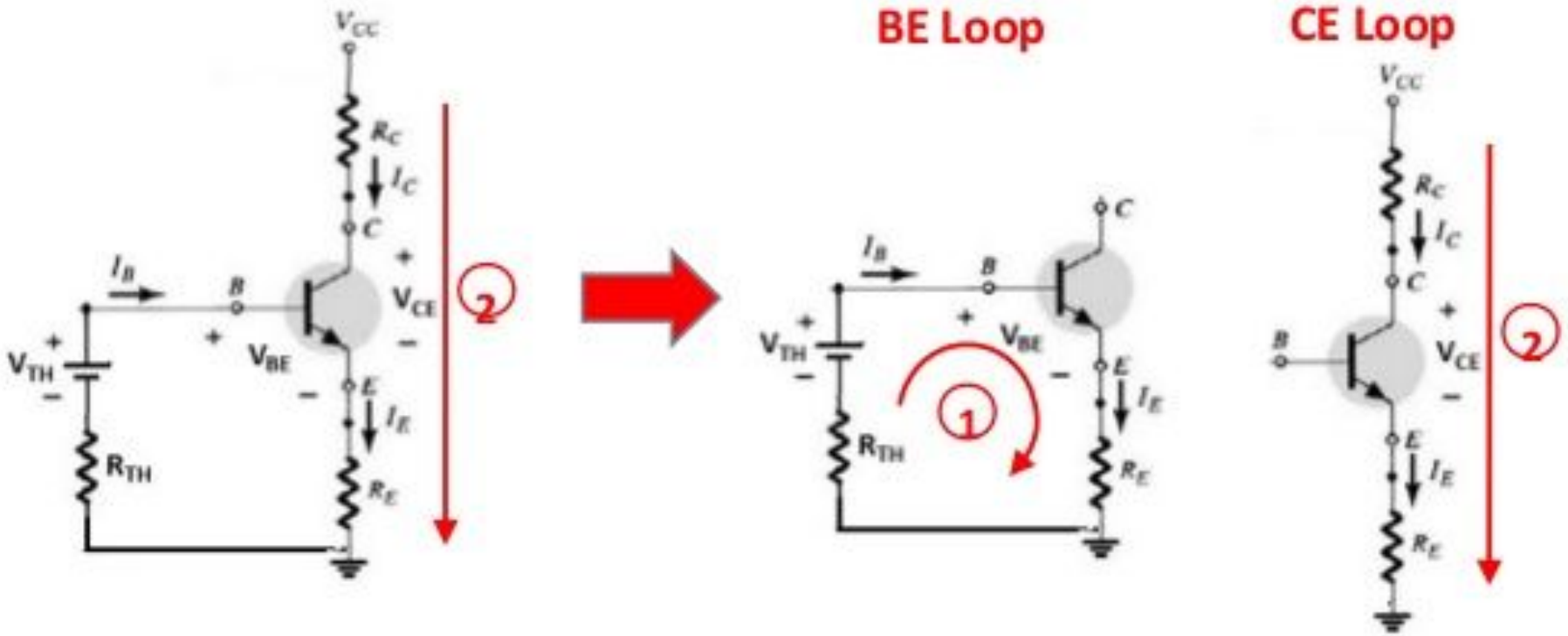
From Thevenin Theorem;

$$R_{TH} = R_1 // R_2 = \frac{R_1 \times R_2}{R_1 + R_2}$$

$$V_{TH} = \frac{R_2}{R_1 + R_2} V_{CC}$$

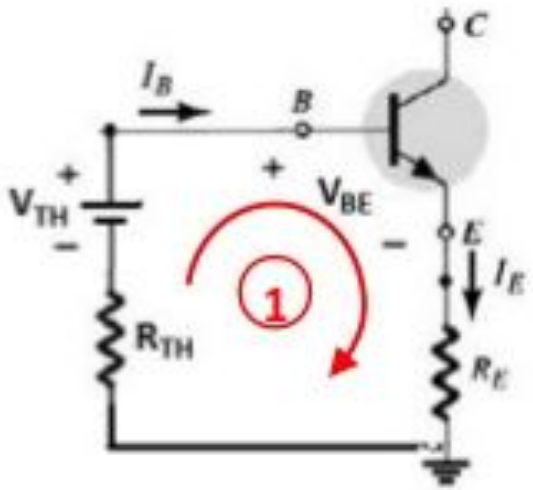
Voltage Divider Bias Circuit

- 3rd step: : Locate 2 main loops.



Voltage Divider Bias Circuit

- BE Loop Analysis



$$V_{TH} - I_B R_{TH} - V_{BE} - I_E R_E = 0$$

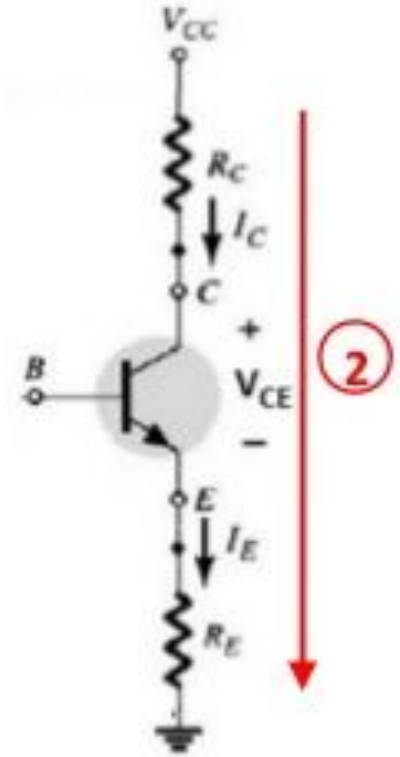
Recall; $I_E = (\beta + 1) I_B$

Substitute for I_E

$$V_{TH} - I_B R_{TH} - V_{BE} - (\beta + 1) I_B R_E = 0$$

$$\therefore I_B = \frac{V_{TH} - V_{BE}}{R_{RTH} + (\beta + 1) R_E}$$

Voltage Divider Bias Circuit



- CE Loop Analysis

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

Assume;

$$I_E \approx I_C$$

Therefore;

$$\therefore V_{CE} = V_{CC} - I_C (R_C + R_E)$$