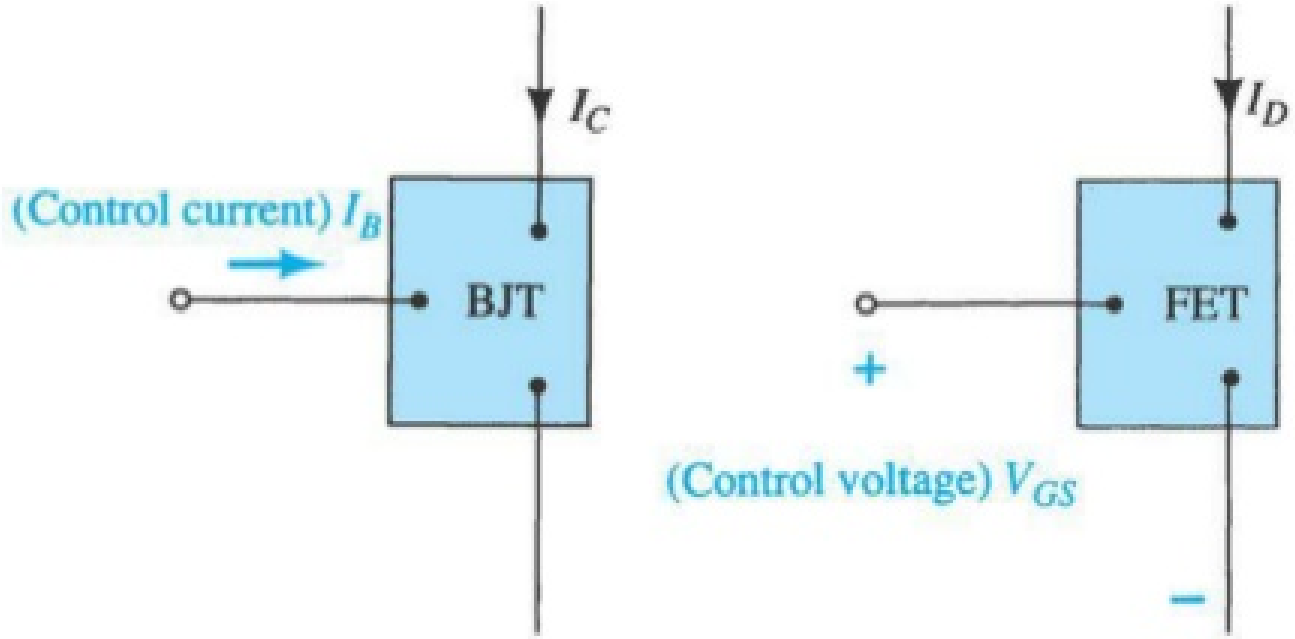
FET
(FIELD EFFECT TRANSISTOR)

Engr. Jess Rangcasajo
jessrangcasajo@gmail.com
ECE 321 Instructor

Field Effect Transistor

Field effect Transistor is a semiconductor device which depends for its operation on the control of current by an electric Field

FET'S VS. BJT'S



Similarities:

- Amplifiers
- Switching Device
- Impedance Matching Circuits

Field Effect Transistor

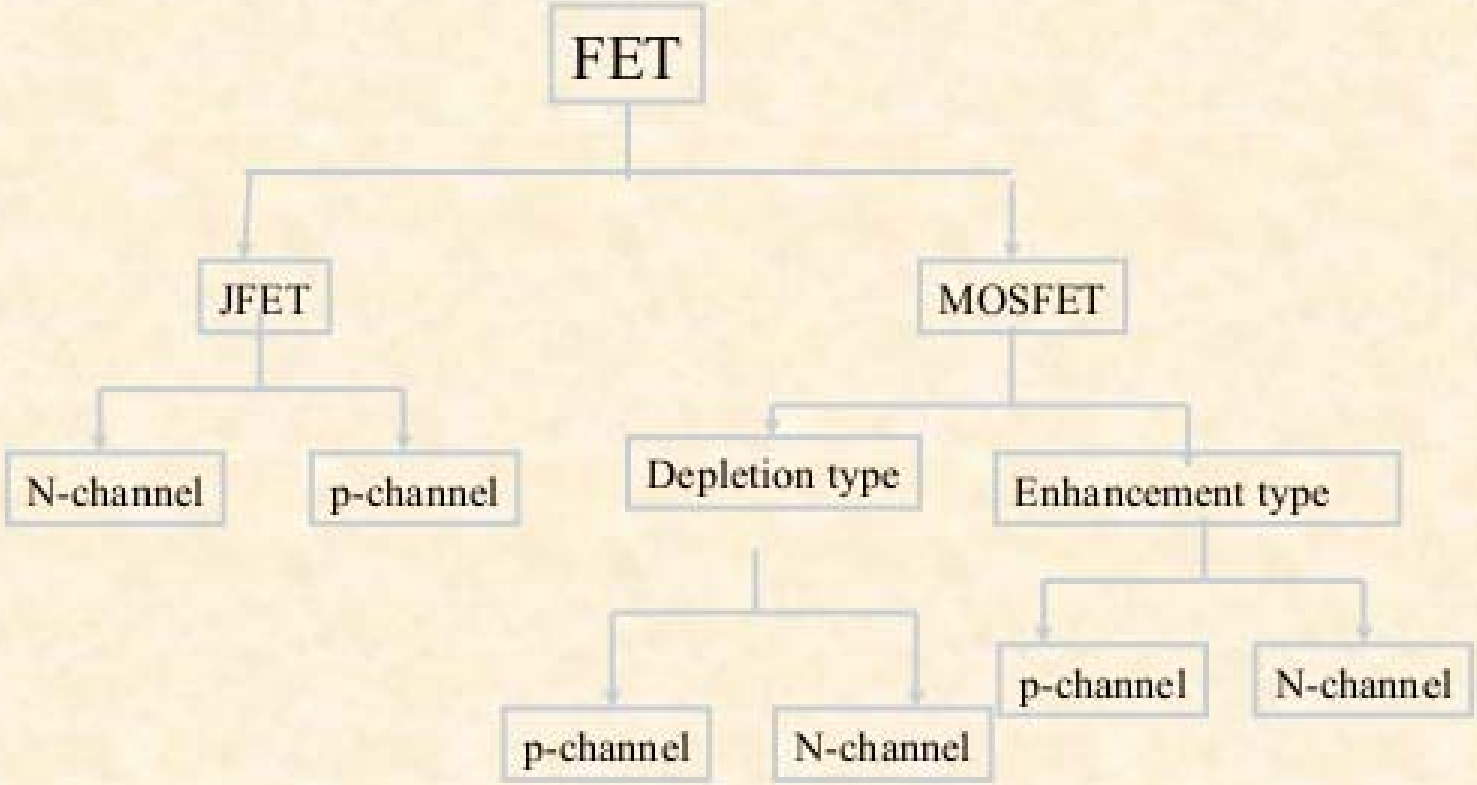
FET has several advantages over BJT

1. Current flow is due to majority carriers only
2. Immune to radiation
3. High input resistance
4. Less noisy than BJT
5. No offset voltages at zero drain current
6. High thermal stability

FET and BJT

FET	BJT
1. Uni polar device	1. Bipolar device
2. Voltage controlled Device	2.Current controlled device
3. High input impedance (in Mega ohms)	3.Low input impedance
4. Better thermal stability	4.Low thermal stabilty
5. High switching speeds	5.Lower switching speeds
6. Less Noisy	6.More noisy
7. Easy to fabricate	7.Diffuicult to fabricate on IC

Classification of Field Effect Transistors



TYPES OF FET

1. JFET (Junction FET)
2. MESFET (metal-semiconductor FET)
3. MOSFET (metal-oxide-semiconductor FET)
   a. D-MOSFET (Depletion)
   b. E-MOSFET (Enhancement)

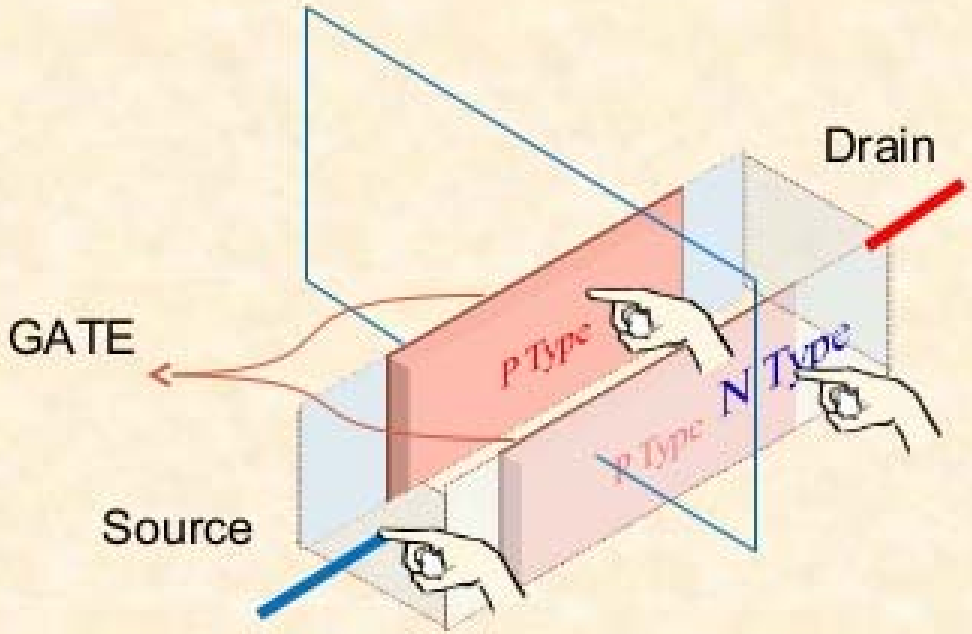
Construction of FET

Source : The source is the terminal through which majority carriers enter the Silicon Bar

Drain : Terminal through which Majoroty carriers leave the bar

Gate: controls Drain current and is always reverse biased

Construction



The two ends of the bar are known as Source and Drain

Fig 3. Construction of N Channel FET

Principle

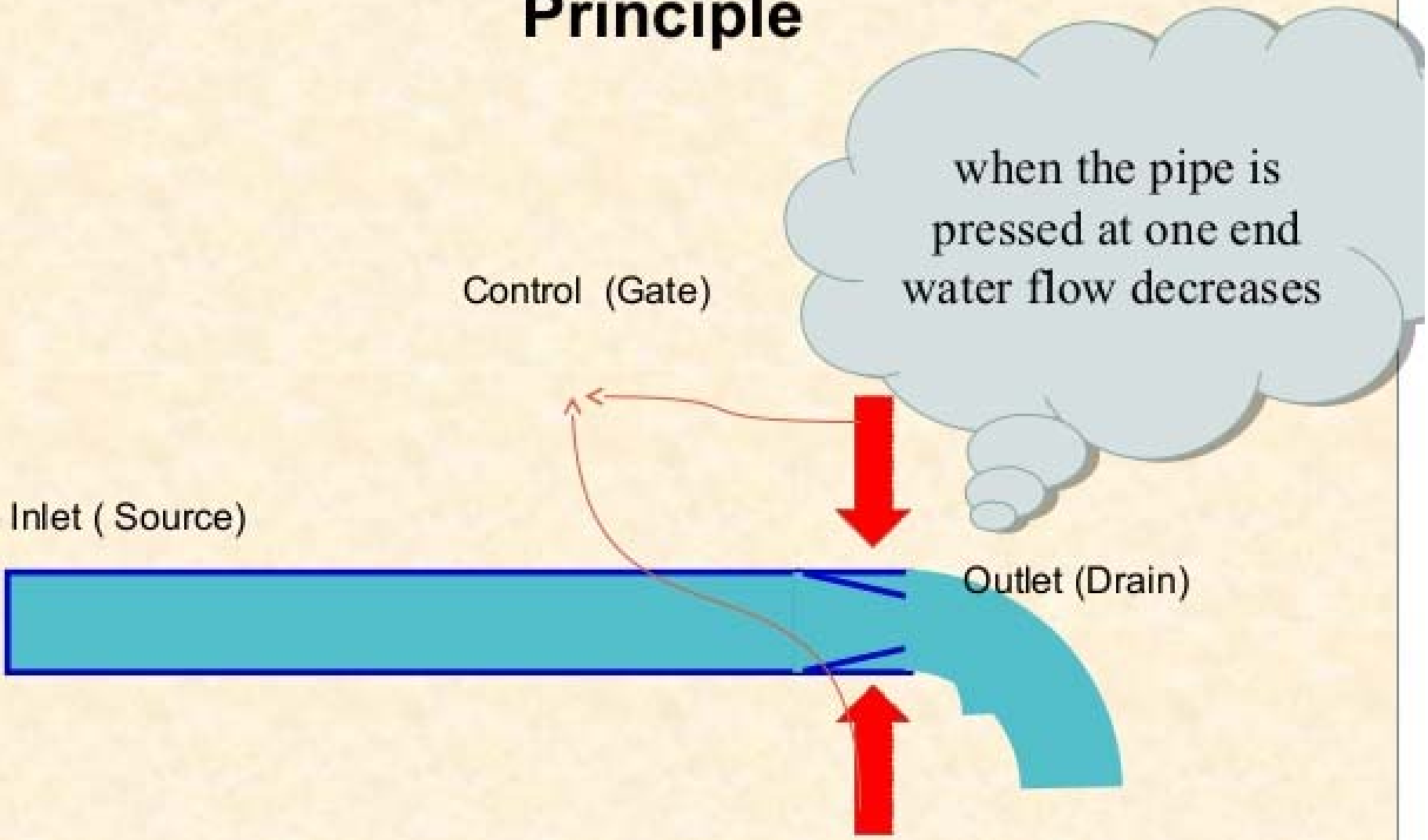
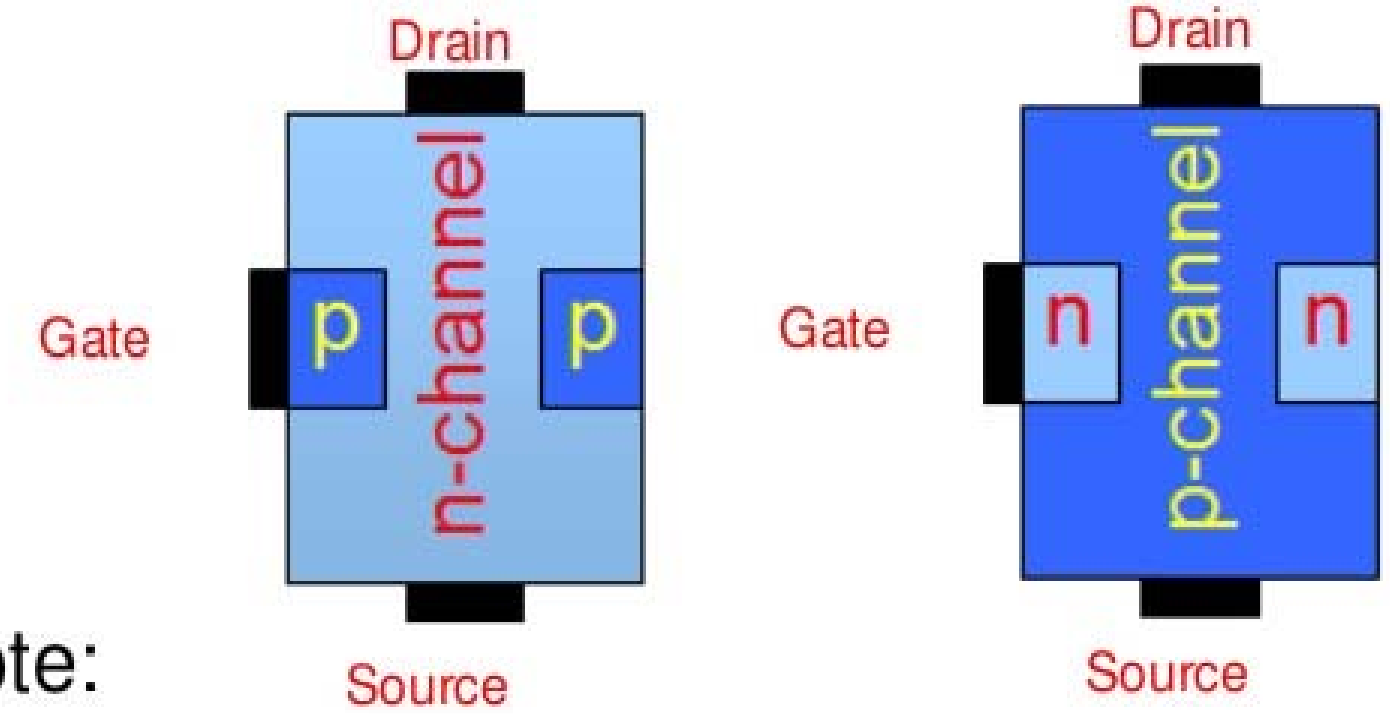


Fig2. water Pipe analogy

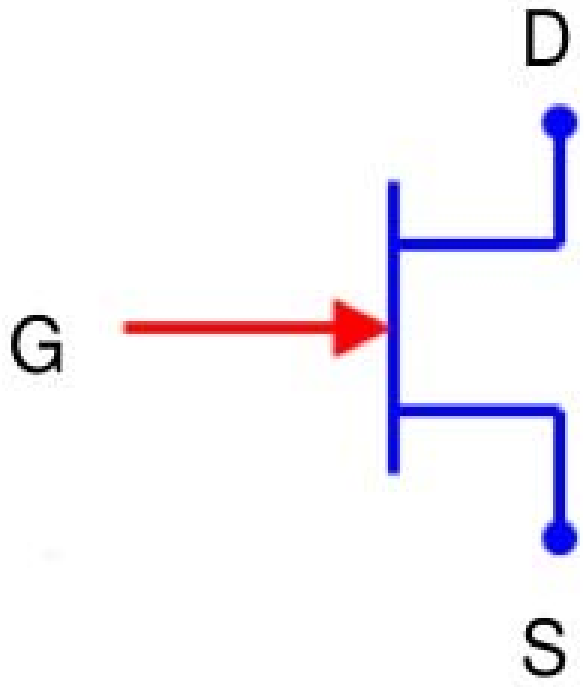
Two types of JFET

1. n-channel
2. p-channel

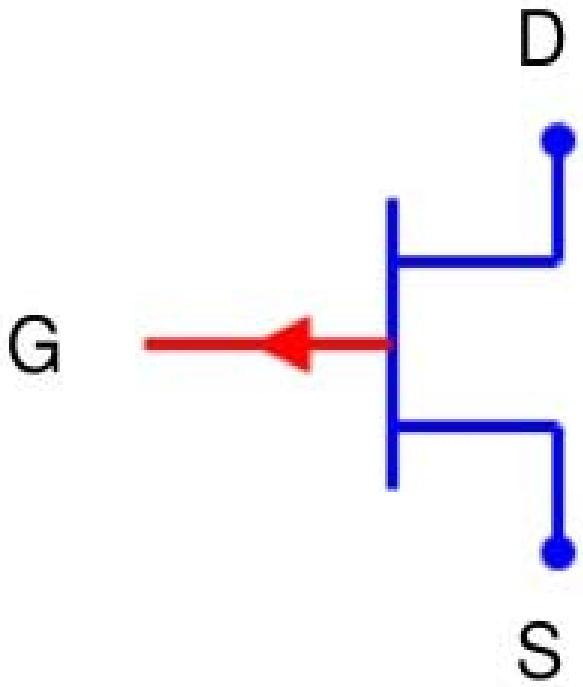


Note:

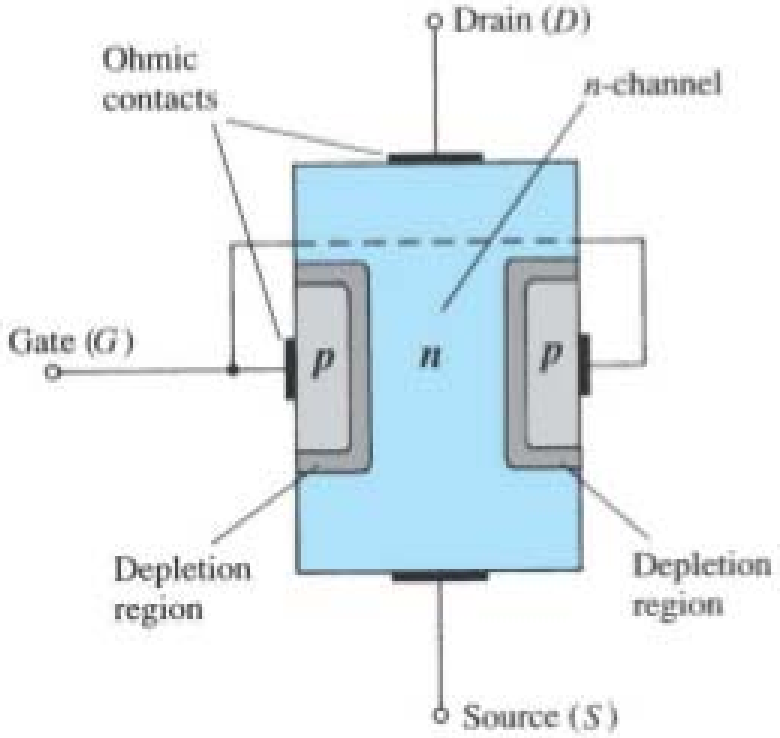
- n-channel is more widely used.

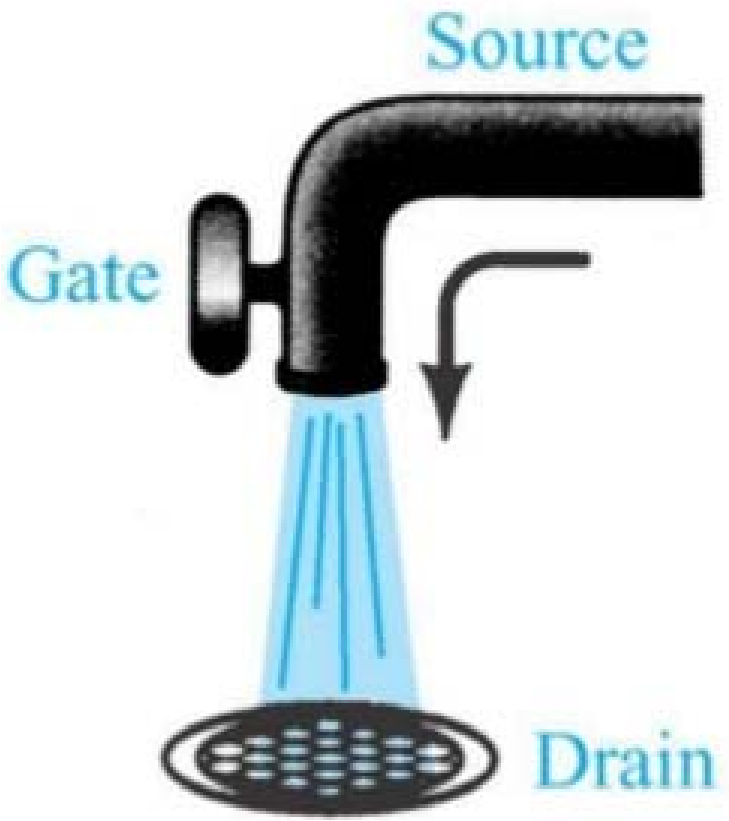


n-channel



p-channel





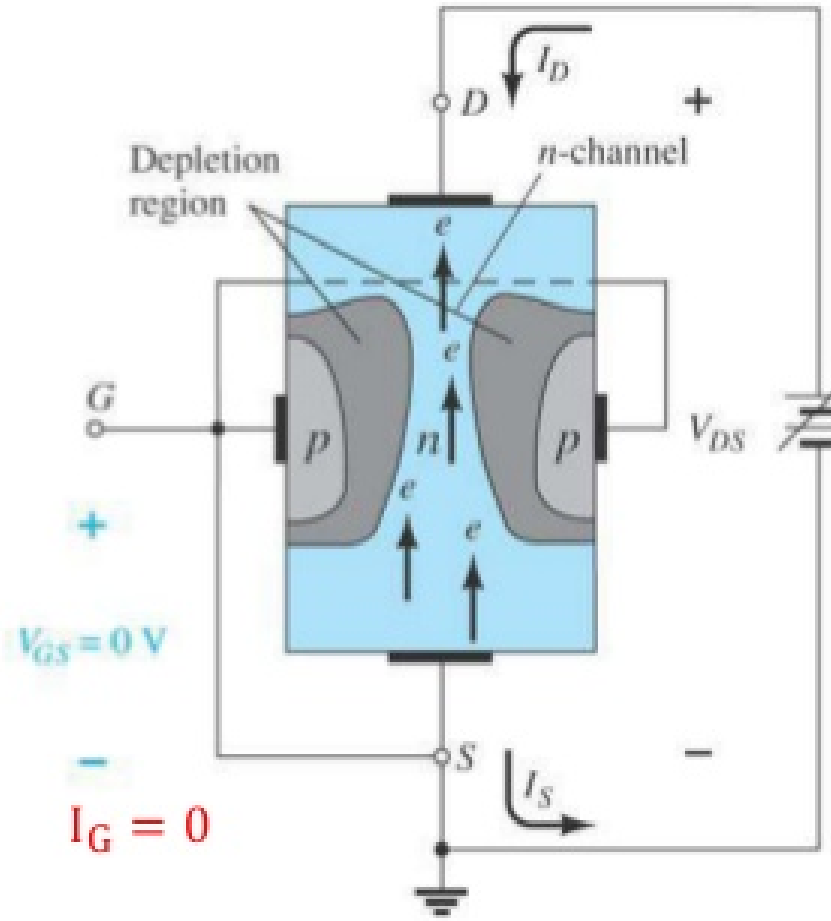
- **Drain (D) and Source (S) are connected to the n-channel**
- **Gate (G) is connected to the p-type material**

- JFET is always operated with the gate-source PN junction **reversed biased**.

- Reverse biasing of the gate source junction with the negative voltage produces a depletion region along the PN junction which extends into the n-channel and thus increases its resistance by restricting the channel width as shown in the preceding figure.

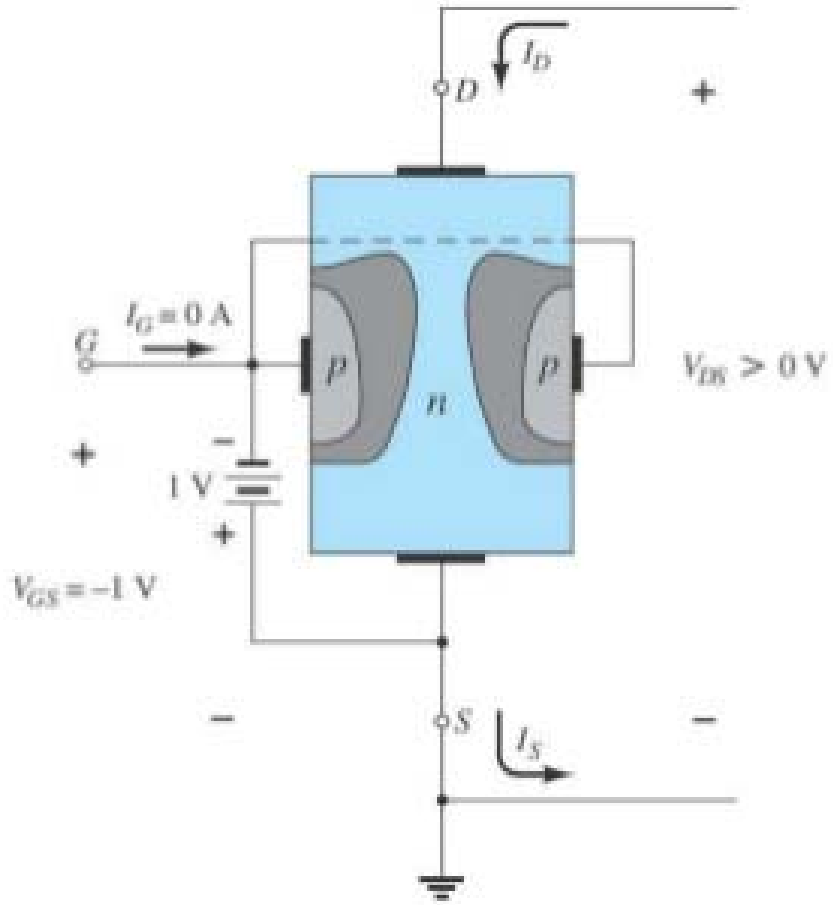
$V_{GS} = 0, V_{DS}$ SOME POSITIVE VALUE

When $V_{GS} = 0$ and V_{DS} is increased from 0 to a more positive voltage.



- The depletion region between p-gate and n-channel increases
- Increasing the depletion region, decreases the size of the n-channel which increases the resistance of the n-channel.
- Even though the n-channel resistance is increasing, the current (ID) from source to drain through the n-channel is increasing. This is because VDS is increasing.

Recall from DIODE discussion:
- The greater the applied reverse bias, the wider is the depletion region.

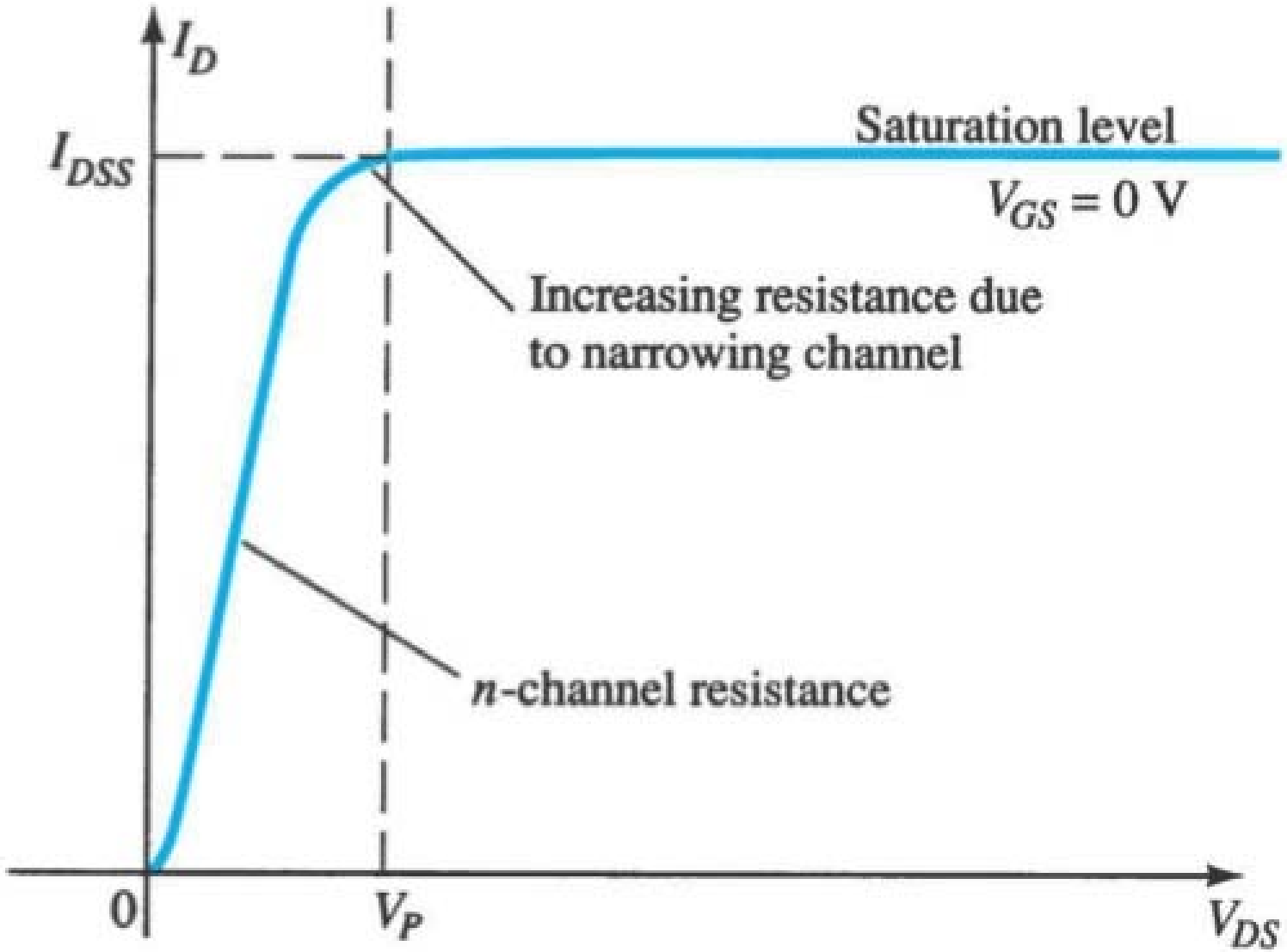


$V_{GS} \geq 0$

- Voltage from gate to source is controlling voltage of the JFET.
- As V_{GS} becomes more negative, the depletion region increases.
- The more negative V_{GS}, the resulting level for I_D is reduced.
- Eventually, when $V_{GS} = V_p$ [$V_p = V_{GS}$ **(off)**], I_D is 0 mA. (the device is "**turned off**".

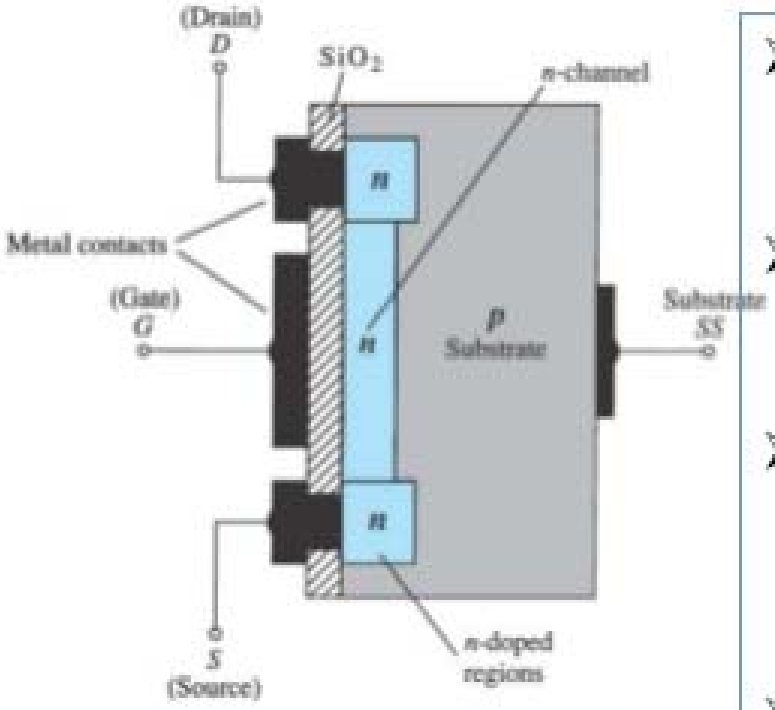
•The level of V_{GS} that results in I_D=0 mA is defined by V_{GS}=V_P, with V_P being a negative voltage for n-channel devices and a positive voltage for p-channel JFETs.

Application of a negative voltage to the gate of a JFET.



I_D versus V_{DS} for $V_{GS} = 0$ V

DEPLETION-TYPE MOSFET CONSTRUCTION

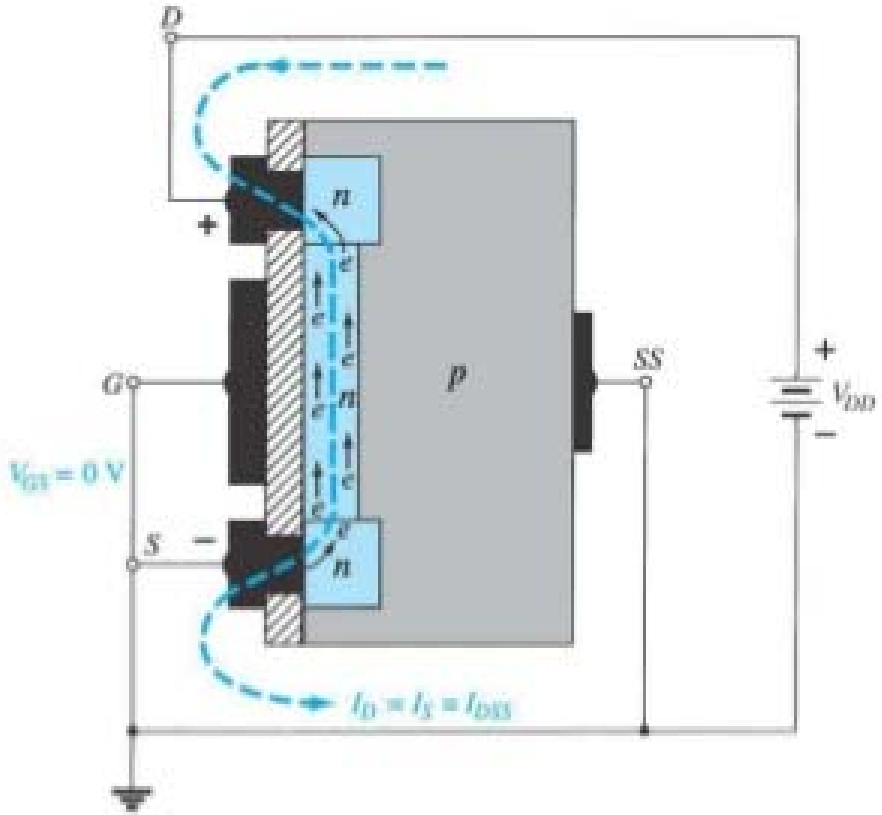


n-Channel depletion-type MOSFET

- The Drain (D) and Source (S) connect to the to n-doped regions.
- These n-doped regions are connected via an n-channel.
- This n-channel is connected to the Gate (G) via a thin insulating layer of SiO2.
- The n-doped material lies on a p-doped substrate that may have an additional terminal connection called Substrate (SS).

Dielectric insulator

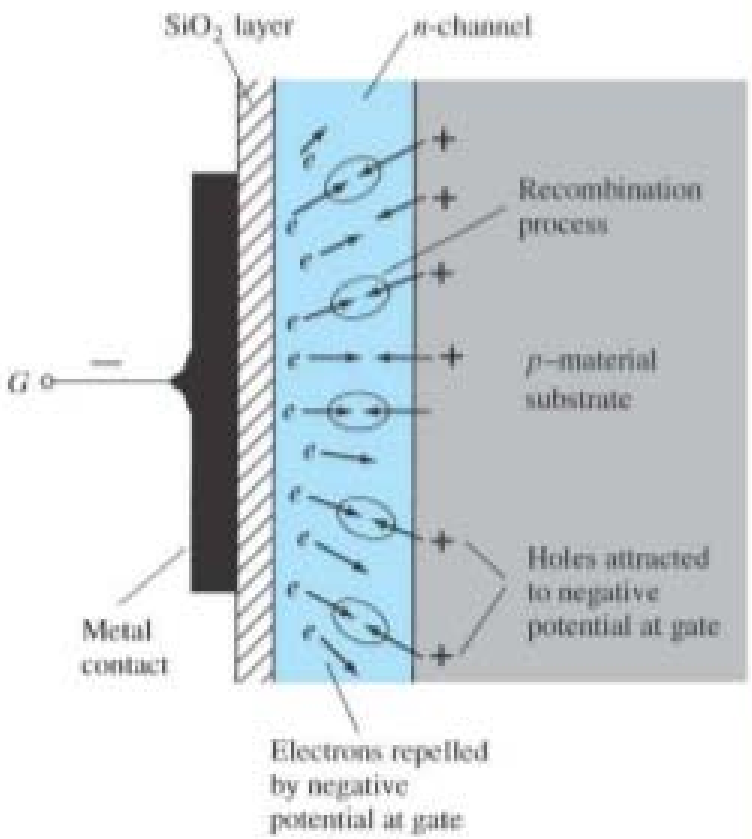
DEPLETION-TYPE MOSFET :BASIC OPERATION AND CHARACTERISTICS



n-Channel depletion-type MOSFET with $V_{GS} = 0$ V and applied voltage V_{DD}.

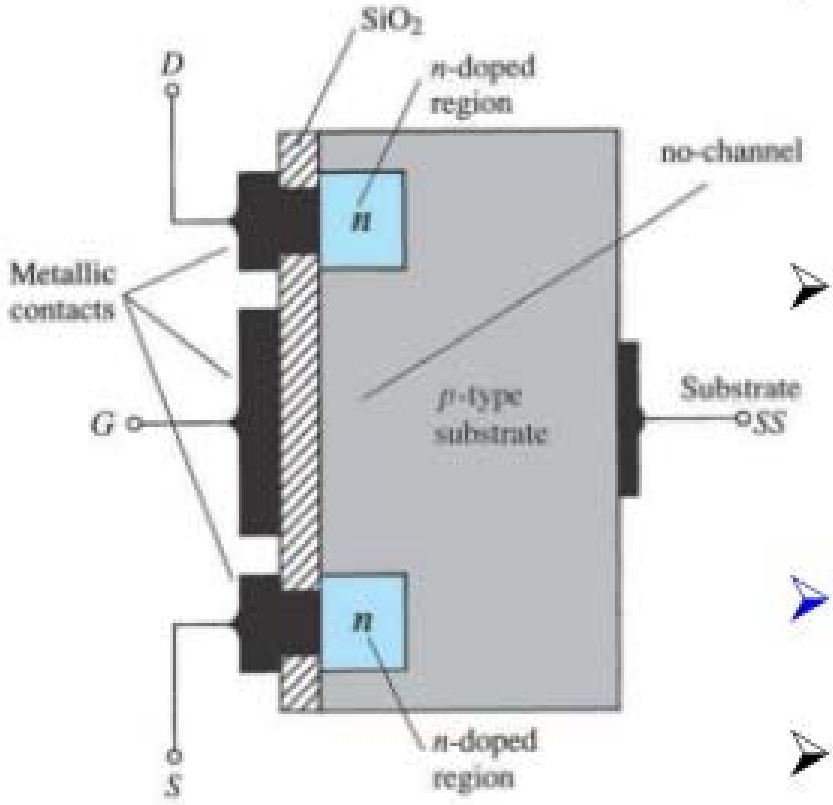
- ✓ $V_{GS} = 0$ and V_{DS} is applied across the drain to source terminals.
- ✓ This results to attraction of free electrons of the n-channel to the drain, and hence current flows.

Continuation….

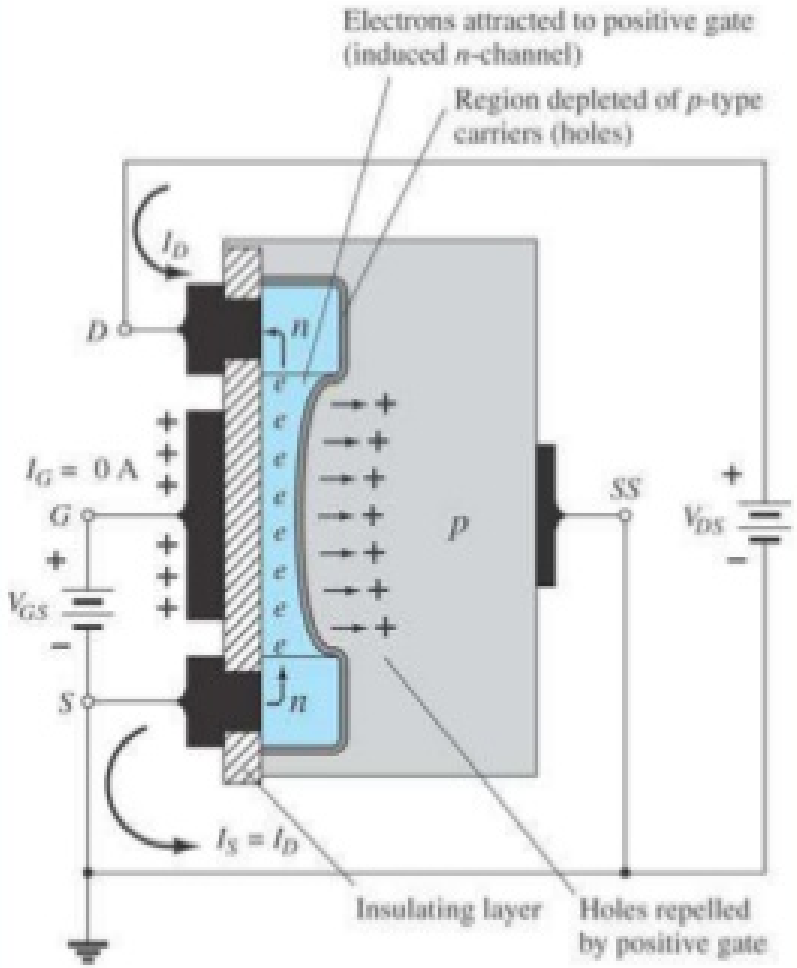


- V_{GS} is set at a negative voltage such as -1 V
- The negative potential at the gate pressure electrons toward the p-type substrate and attract the holes for the p-type substrate.
- This will reduce the number of free electrons in the n-channel available for conduction.
- The more negative the V_{GS} , the resulting level of drain current I_D is reduced.
- When V_{GS} is reduced to V_P (pinch off voltage), then $I_D = 0mA$.

ENHANCEMENT-TYPE MOSFET CONSTRUCTION



- The Drain (D) and Source (S) connect to the to n-doped regions.
- The Gate (G) connects to the p-doped substrate via a thin insulating layer of SiO2
- **There is no channel**
- The n-doped material lies on a p-doped substrate that may have an additional terminal connection



- For $V_{GS} = 0, I_D = 0$(no channel)
- For V_{DS} some positive voltage and $V_{GS} = 0$, two reversed biased n-junctions and no significant flow between drain and source.

- For $V_{GS} > 0$ and $V_{GS} > 0$, the positive voltage at gate pressure holes to enter deeper regions of the p-substrate, and the electrons in p-substrate and the electrons in p-substrate will be attracted to the positive gate.
- The level of V_{GS} that results in the significant increase in drain current in called:
  THRESHOLD VOLTAGE (Vt)
- For $V_{GS} < V_T$, $I_D = 0ma$

THANK YOU!