Module : 5

Microprocessor is an integrated chip with central processing unit.

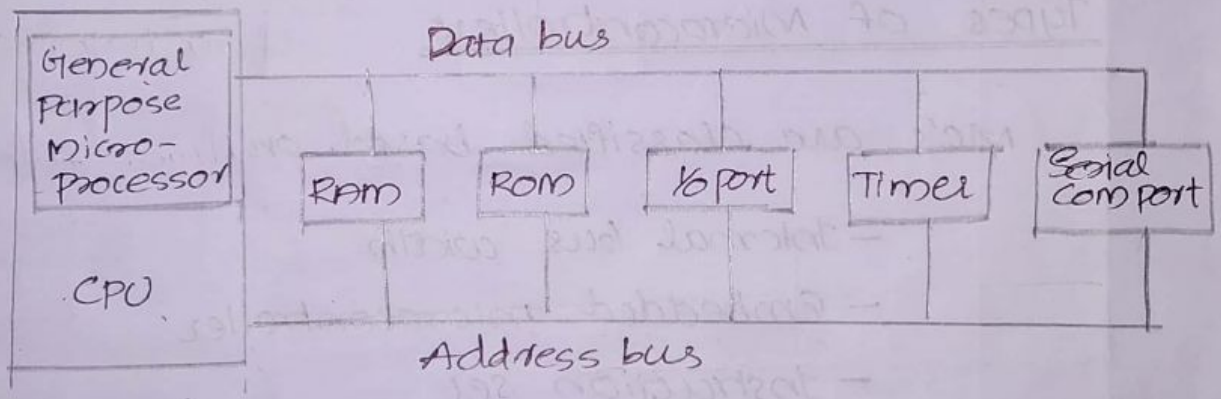
- It contains no RAM, ROM, IO ports on the chip.

Eg: Intel x86 family, Motorola 680x0, Intel 4004.

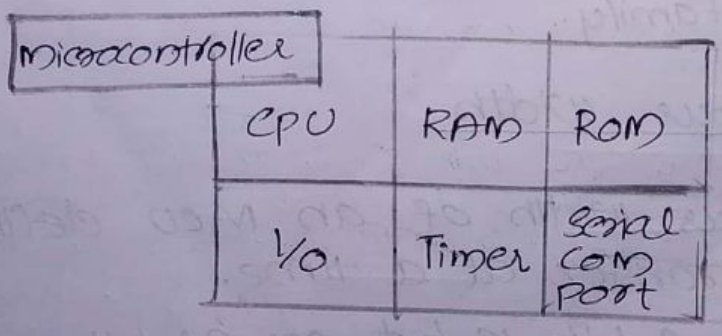
Microcontroller is a microcomputer with few application specific devices on a single chip or VLSI core.

Eg: TMS 1000 Gary Boone & Michael Cochran of Texas Instruments

4 bit MC Intel 8051 (8 bit MC)



Microprocessor based system



Microcontroller

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• Microprocessor is heart of computer	• Microcontroller is heart of embedded systems.
• Memory, IO components to be externally connected	• Built on chip
• cost is high	• cost is less
• Power consumption is high	• power consumption is less
• Follows Von-Neumann architecture (both Instructions & data are in the same location)	• Follows ~~hard~~ harward architecture
• Less registers, More memory operations.	• Many registers.
• Application: Used in Pc	• Used in specific applications. Remote, fax,

Types of Microcontrollers

MC's are classified based on:

- Internal bus width
- Embedded microcontroller
- Instruction set
- Memory architecture
- Packaging
- Family.

i) Internal bus width

- Internal bus width of an MCU defines no. of bits it can transfer at a time.
- It can be 8 bit, 16 bit or 32 bit

8 bit MC: Intel 8031, Intel 8051, PIC 1X (Series)

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16 bit MC- Intel 8096, PIC 2x

32 bit MC - Intel 251 family, PIC 3x

ii) Embedded microcontroller

- embedded / extended

iii) Instruction set

- RISC (Reduced instruction set
- CISC (complex instruction set
- CISC with RISC core

iv) Memory architecture

- Von neumann Architecture / Princeton Architecture
- Harvard

v) Packaging

- IC chip
- VLSI core

vi) Family

8051 ——— Intel, philips, ATMEL, Siemens, dallas

Motorola

PIC

Hittachi

Texas

ARM

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CRITERIA FOR CHOOSING A MICROCONTROLLER

1. Perform task efficiently & cost effectively.
   Decide 8 bit, 16 bit, 32 bit microcontroller can best handle the computing needs of task.
   a) Speed
   b) packaging
   c) Power consumption
   d) Amount of RAM, ROM on chip
   e) Number of I/O pins and timer on chip
   f) How easy is to upgrade to higher performance or lower power-consumption versions.
   g) Cost per unit.

2. How easy it is to develop around it.
   - availability of assembler, debugger, code efficient C language compiler, emulator, technical support.

3. Ready availability in needed quantities both now and in future.

SELECTION OF A MC

Features taken into consideration while selecting a MCU

* 8 bit, 16 bit or 32 bit ALU
* power dissipation permissible (max limit) clock speed (lowest limit).
* RISC/CISC/RISC core with CISC instruction set.
* Program storage architecture - Harvard or Princeton and required total external and internal memory upto or more.
* DMA controller requirement.

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* Cache memory management unit requirement.
* Intensive ~~const~~ computations as a fast rate requirement.

Additional

* Cost when single chip /MCU interfaces to circuit with some features externally added.
* Major building H/w blocks their cost and availability.
* Major building blocks of software, cost and availability, and required H/w - S/w tradeoff.
* Ease of integration.
* Availability of design team expertise.
* Availability and cost of development S/w & H/w tools.
* Ease and availability of testing and debugging facilities.
* Ease and reliable availability of MCU, development tools and building blocks for H/w & S/w.

6/08/2019

Characteristics & Resources of a MC

The various on chip resources are :

1. Basic processing unit, internal buses, interrupt handler.
2. On-chip program memory (EEPROM, Flash)
3. On chip RAM
4. Interfacing capability to external program memory.
5. Interfacing capability to external data memory.
6. IO ports.
7. On-chip registers.
8. Special function Registers.
9. UART Universal Asynchronous Receiver Transmitter
10. Serial Asynchronous
11. Timers/Counters.
12. Pulse width Modulator (PWM)
13. On-Chip ADC

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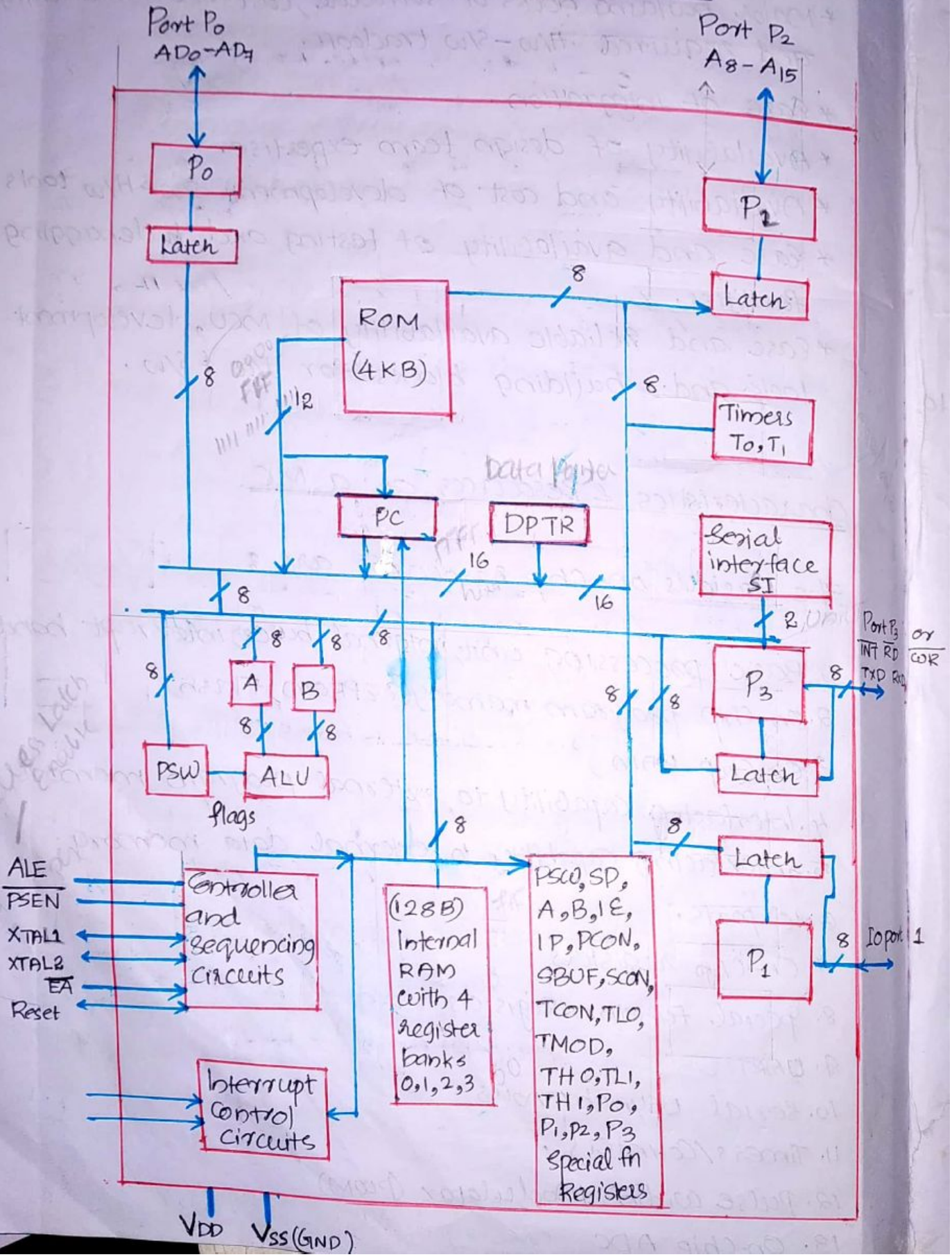
14. Watchdog Timer
15. Bitwise manipulation capability.
16. power down mode
17. Real time clock.

Slides

ARCHITECTURE OF 8051



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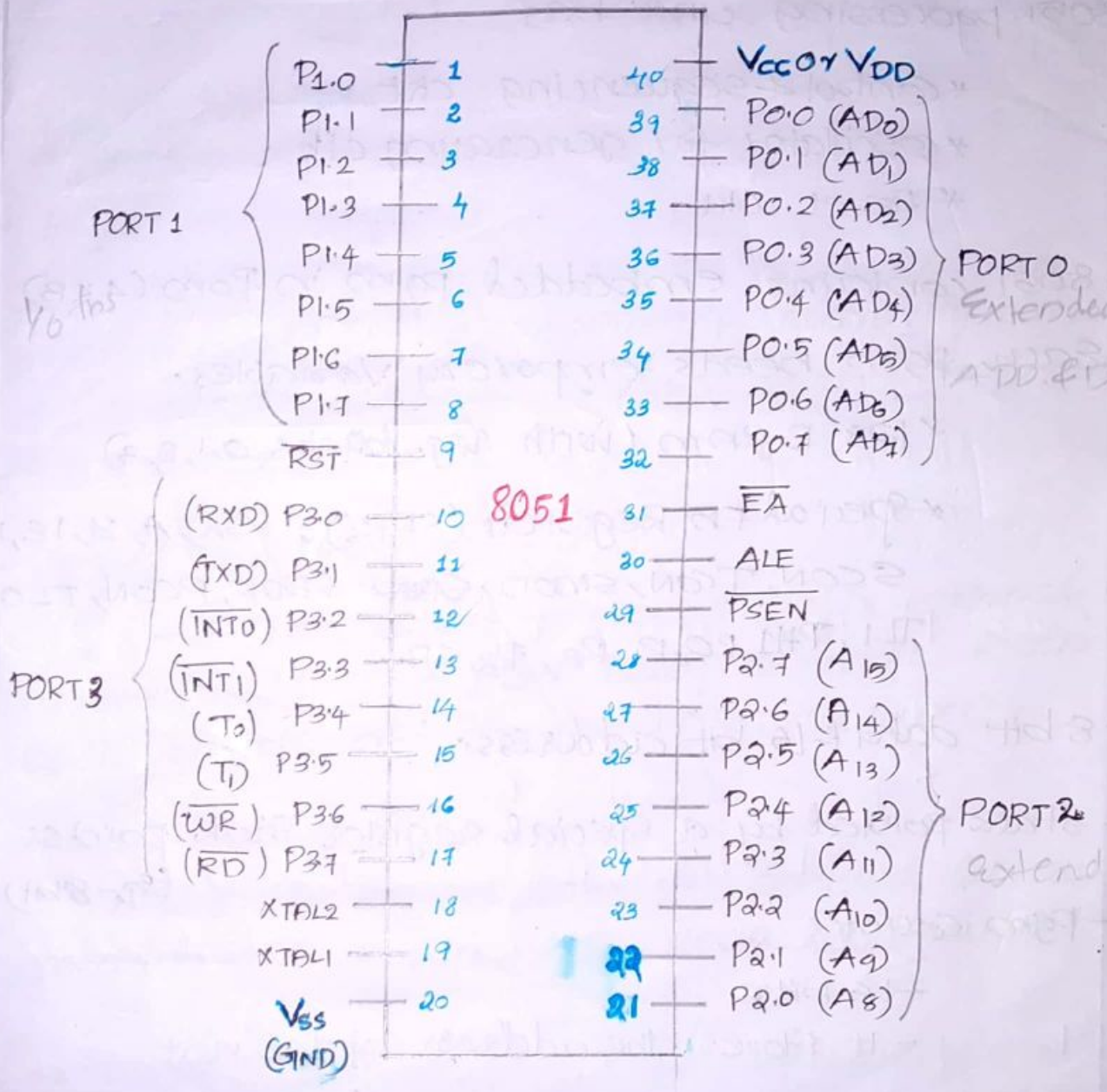
8051 PIN DIAGRAM



Main features of 8051

Feature	8051
* ROM (on-chip pgm space in bytes)	4KB
* RAM (bytes)	128
* Timers	2
* I/O Pins (four ports)	32
* Serial port	1
* Interrupt sources	6

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- 8051 is a DIP IC with 40 pins dedicated for various functions such as I/O, RD, WR, address, data and interrupts.

- 8051 processing unit has

  * Control and sequencing ~~unit~~ ckt.
  * Oscillator for generating clock.
  * Reset ckt.

- 8051 contains embedded pgm in ROM (4 KB)

  * 8051 can work in single mode (internal devices & ckts) and Expanded mode (address and data bus signals)

- Each program needs temporary variables.

  * 128 B RAM (with reg. banks 0, 1, 2, 3)
  * Special function Registers (SFRs):

PSW, A, B, IE, IP, SCON, TCON, SMOD,
~~SFR~~ SBUF, PCON, TL_0, TH_0, TL_1, TH_1, P_0, P_1, P_2, P_3, SP

- Stack pointed by a special register Stack Pointer (SP - 8 bit)

- Program Counter (PC)

  * Lower byte at bus A_0-A_7 / data bus D_0-D_7:

    Expanded mode (port 0: single mode)

  * Higher byte at bus A_8-A_{15}:

    Expanded mode (port 2: single mode)

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- Data Pointer (DPTR)
  * To access data from external memory.
  * Lower byte (DPL) higher byte (DPH)

- 10 devices connection through ports: Port 0, 1, 2, 3

- Interrupts
  * Two external pins INT0 and INT1
  * Interrupt control circuit.
  * Two SFRs IP (Interrupt priority) and IE (Interrupt enable).

- Serial Interface
- Two programmable timers/event counters for real

USE of Subunits and Signals

PC - program counter

16 bit address pointer PC holds program memory address of instruction currently being fetched. PC consists of 2 bytes PCH (higher) and PCL (lower).

DPTR - Data Pointer

16 bit address pointer, it holds external data memory address of data being currently fetched. DPTR consists of DPH (higher) & DPL (lower).

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A - Accumulator

8 bit register, saves an operand for ALU op's and accumulates final result in A.

B - B register

8 bit register, saves second operand for ALU, accumulates part of result.

ALU - Arithmetic & Logic

Unit performing arithmetic & logic operations.

PSW - Processor status word

8 bit register to save status & status bits.

P0 - Port 0

8 bit port for I/O in single mode & data bus/ lower order address signals AD_0-AD_7 in expanded mode.

P2 - Port 2

8 bit port for I/O in single mode & higher order address signals AD_8-AD_{15} in expanded mode.

P1 - Port 1

8 bit Port for I/O in single mode.

P3 - Port 3

8 bit port for I/O in single mode & used for serial interface (SI) signals, timer T_0 & T_1 inputs, interrupts INT_0 and INT_1 inputs, sending RD & WR signals for memory read & write in expanded mode

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SI - Serial Interface device

Serial IO operations. 2 modes:

- Full duplex (Input and output at an instance) UART
- half duplex (Input and output at an instance) synchronous communication.

2 pins of P3 : RxD , TxD

2 pins of P3 : DATA & CLOCK.

T0 & T1 - Timers T0 and T1

Timing devices ; it has 4 registers TH1, TL1, TH0, TL0.

SFR - special function Registers

SP, PSW, A, B, IE, IP, P0, P1, P2, P3, SCON, TCON, SMOD, SBUF, PCON, TL0, TH0, TL1, TH1

ROM - Read only Program memory

Masked ROM, EPROM, Flash EEPROM of 4kb, internally connects to PC bus of 12 bits; Address is b/w 0x0000 & 0X0FFF.

Internal RAM - Internal Random Access Memory

RAM is 128 Bytes for read and write, indirectly and directly addressable; Address b/w 0x00 & 0x7F

Register Banks - Four set of registers

4 registers banks each of 8 registers; part of internal RAM.

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XTAL1 & XTAL2 - Pins to Crystal

Pins to crystal oscillator ckt; 12 MHz crystal in 8051.

$\overline{EA}$ - External Enable

To enable use of external memory addresses.

RST - Reset pin

Reset ckt input; let processor reset and synchronize with external peripheral devices.

$\overline{INT_0}$, $\overline{INT_1}$ - Interrupt pins

Two External interrupts, ~~Activ~~ Active from low.

V_{cc} (V_{dd}) & V_{ss} (GND) - Voltage Supply Pin & Ground pin

V_{cc} - 5V supply & V_{ss} - Ground connections.

$\overline{PSEN}$ - Program store Enable

Activates for reading external prgm memory byte.

$\overline{RD}$ - Read

Activates for reading a byte from external program memory byte.

$\overline{WR}$ - Read

Activates for writing a byte to external program memory byte.

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Special function Registers in 8051

- The 128 KB internal RAM is divided into:
  - * General purpose registers (used for any purpose)
  - * Bit Addressable registers (Access data by bit wise)
  - * Register Banks

- special Fn registers are used to pgm and control different hardware peripherals like Timers, serial port, I/O ports etc.

8 bits → Filled by register

→ stack

lower 128 B (00H-7FH)
(direct and indirect Addressing)

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Special Function Registers

1. CPU Math Registers – A, B
2. Program status word – PSW
3. Pointer Registers – DPTR (DPH, DPL), SP, PC
4. IO port registers – P0, P1, P2, P3
5. Peripheral Control Registers
   1. PCON (Power Control)
   2. SCON (Serial Control)
   3. TCON (Timer Control) – 4. TMOD
   5. IE (Interrupt Enable)
   6. IP (Interrupt Priority)
6. Peripheral Data Registers
   1. SBUF (Serial Data Buffer)
   2. TL0/TH0 (Timer 0 Low/High)
   3. TL1/TH1 (Timer 1 Low/High)

1. Math Registers

A – Accumulator
B – B register

A

- general purpose register
-

B

- Multiplication & division can be performed only upon nos stored in A & B
- Temporary Storage

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8. Program Status Word – 8 bit register

- The PSW register contains several status bits that reflect the current state of the CPU.

CY	AC	F0	RS1	RS0	OV	F1	P

CY – PSW.7 – Carry Flag

AC – PSW.6 – Auxiliary carry Flag

F0 – PSW.5 – Flag 0 available to the user for General purpose

RS1 – PSW.4 – Register Bank selector bit 1

RS0 – PSW.3 – Register Bank selector bit 0

OV – PSW.2 – overflow flag.

F1 – PSW.1 – User definable flag.

P – PSW.0 – Parity flag. Set/cleared by hardware each instruction cycle to indicate an odd/even number of 1 bits in the accumulator.

With RS1 & RS0 bits we can select the corresponding Reg. bank

RS1	RS0	Register Bank	Address
0	0	0	00H – 07H
0	1	1	08H – 0FH
1	0	2	10H – 17H
1	1	3	18H – 1FH

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19/08/19

3 Pointer Registers

- DPTR, SP, PC
  - SP → 8 bit
    - Points to Stack
    - Stack in bank 1
    - Always initialize with 07H
    - It is the last location.

DPTR (Data Pointer)

- It uses when there is external memory.
  - DPH (Higher)
  - DPL (Lower)

4. IO Port Registers

- P0, P1, P2, P3

- All this ports have 8 bit capacity.
- Reset, All the field values of all ports are 1.
- If there is 1 in port, then the port is input port
- 0 → output port.
- It is bit addressable.

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5. Peripheral Control Registers

- PCON, TCON, SCON, TMOD, IE, IP

PCON (Peripheral/Power Control)

PD & IDL both take 1 then 1st preference goes to PD.

7							0
SMOD	–	–	–	GF1	GF0	PD	IDL

- IDL - Idle mode: Cut the clock to the CPU & provide to the timer.
- PD - Power ~~need~~down mode: It control the power
- GF1 & GF0 : User defined fields.
- The black spaces for future modes, Normaly it gives the value '0'.
- SMOD - Serial mode: Double data rate

If it is 1, then the baud rate in the serial mode becames double.

Baud rate – No. of bits transfer in 1 second.

TCON (Timer Control / counter control Register)

7							0
TF_1	TR_1	TF_0	TR_0	IE_1	IT_1	IE_0	IT_0

- TF_0 & TF_1 - Timer overflow

  TF_0 - Set 1, the overflow in timer T_0

  TF_1 - Set 1, the overflow in timer T_1

- TR_1 - Enables timer T_1
- TR_0 - Enables timer T_0
- IE_1 - Its external interrupt 1 flag, This is set by hardware interrupt & cleared coben that interrupt is processed.
- IE_0 - Its external interrupt 0 flag, this is set by

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hardware interrupt & cleared when that interrupt is processed.

IT1 – Interrupt 1 type control bit set & cleared by S/W
IT0 – Interrupt 0 type control bit set & cleared by S/W.

TMOD (Timer Mode)

Timer 1 | Timer 0

GATE 1	C/T1	M1	M0	GATE 0	C/T0	M1	M0

M1	M0	Mode	Description
0	0	0	13 bit (higher – 8 bit, lower → 5 bit)
0	1	1	16 bit timer / counter (0-64 K)
1	0	2	8 bit Auto Reload timer
1	1	3	split mode it split higher half & lower half

GATE 1 – When gate1 = 1, timer1 operates only if the particular interrupt (INT1) bit is set. ie P3.3 is set.

GATE 0 – When gate0 = 1, timer 0 operates only if the particular interrupt (INT0) bit is set ie, P3.2 is set.

C/T0 & C/T1 – It selects the source of pulse to be counted.

C/T1 = 1, T1 (P3.5) (In counter mode)
= 0, it will be taking from oscillator (in timer mode).

C/T0 = 1, T0 (P3.4) (In counter mode)
= 0, it will be taking from oscillator (in timer mode)

M0 & M1

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SCON (Serial Control)

SM0	SM1	SM2	REN	TB8	RB8	TI	RI

SM1	SM0	Mode	Description
0	0	0	8 bit shift register
0	1	1	8 bit UART
1	0	2	9 bit UART } Their baud rate will
1	1	3	9 bit UART } be different.

* SM0 & SM1 - It indicates serial bit mode select
* SM_2 - If it is 1, it indicates Multi processor communication
  - If it is 0, it indicates single processor communication.
* REN - Reception Enable bit
  when REN = 1, Then the data is enable. It is ready for take the data from serial port.
* TB8: SBUF (8 bit) - Serial buffer
  ↳ It keeps the additional bit in transmission
* 9 bit UART
  8 bit SBUF + 1 bit
  ↓
  TB8 - transmitter
  RB8 - reception
* TI - transmitter interrupt
* RI - receiver interrupt.

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IE (Interrupt Enable)

EA	-	ET_2	ES	ET_1	EX_1	ET_0	EX_0
7							0

- EA = 1, only the interrupt is enabled.
  EA = 0, doesnot consider the other interrupts.
- ET_2 - Interrupt of Timer T_2
- ES - Enable serial port
- EX_1 - Enable interrupt from pin INT_1 (external interrupt)
- ET_1 - Enable Interrupt of Timer T_1
- ET_0 - Enable Interrupt of Timer T_0
- EX_0 - Enable interrupt from pin INT_0.

IP (Interrupt Polarity)

Interrupt polarity. ←

-	-	PT_2	PS	PT_1	PX_1	PT_0	PX_0
7							0

- The polarity from LSB ie, most polarity for the LSB. (PX_0) - INT_0
-

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20/08/19

Memory & IO Addressing

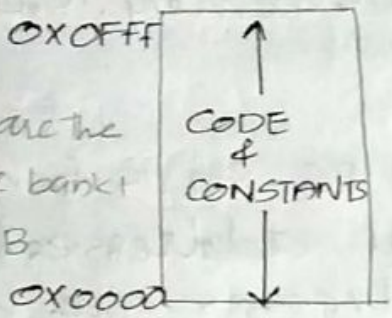
Internal ROM + Internal RAM

0000 - 0FFF 00 - 7F

* general purpose area (Scratchpad area)

Both can extend from 0000 to FFFF

Internal Pgm memory

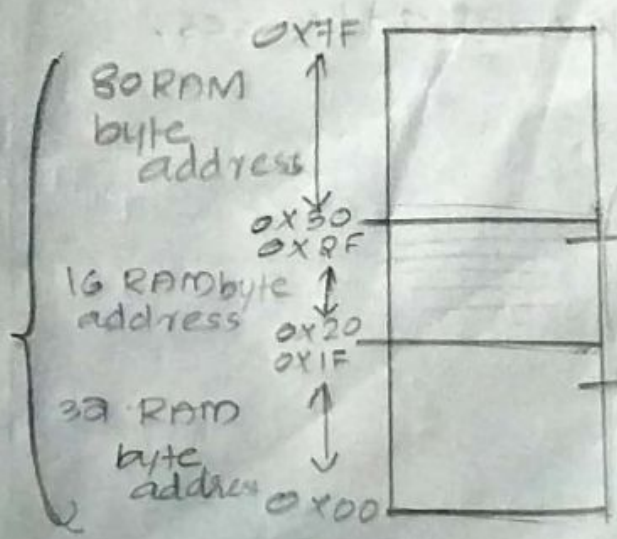


These are the bank of bank1 each of 2kB

When $\overline{EA}$ = 1 during the RESET interval.

When EA=1, Internal ROM is used
EA=0, External ROM

Internal Data Memory



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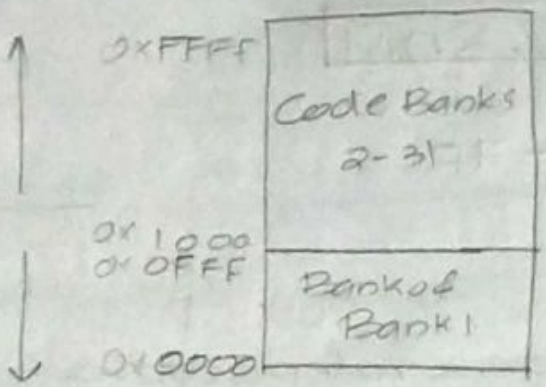
External program Memory



When $\overline{EA}$=0 during RESET

$\overline{EA}$=1,

* First 4KB, taking from internal ROM
balance 60 KB from external ROM.

$\overline{EA}$=0,

* Only consider external memory. ie, 60KB.

Active low

- When $\overline{EA}$ =0 at reset PC starts from 0000H and accesses external addresses from the memory. Memory addresses are b/w 0000H to FFFFH
- When $\overline{EA}$ = 1, at reset, the PC starts from 0000H.

The instructions are accessed from the internal address & then PC is loaded with 1000H from the external addresses.

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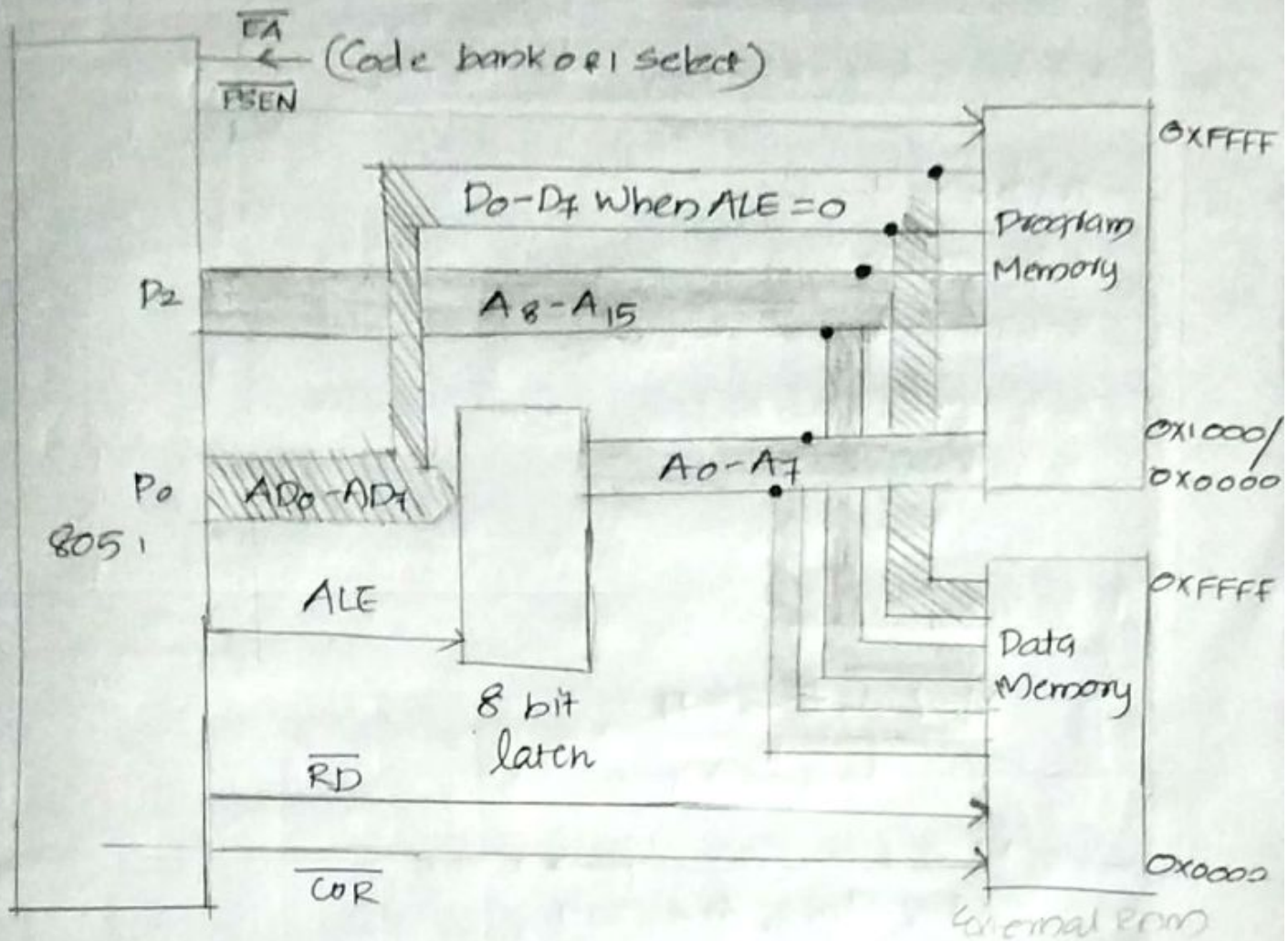
Interfacing of external memory (both pgm & Data Mem)

22/8/19



P0 - Pass lower bit address (AD0-AD7)

P2 - Pass higher bit address (A8-A15)

latch (8 bit) - seperate data & address.

- 1st check EA
- Then enable PSEN (Program Store enable)
- Both EA & PSEN must be enable then Read & write the datas into memory.
- In AD0-AD7,
  - ALE=0, the channel has 8 bit data
  - ALE=1, the channel has 8 bit lower address.

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