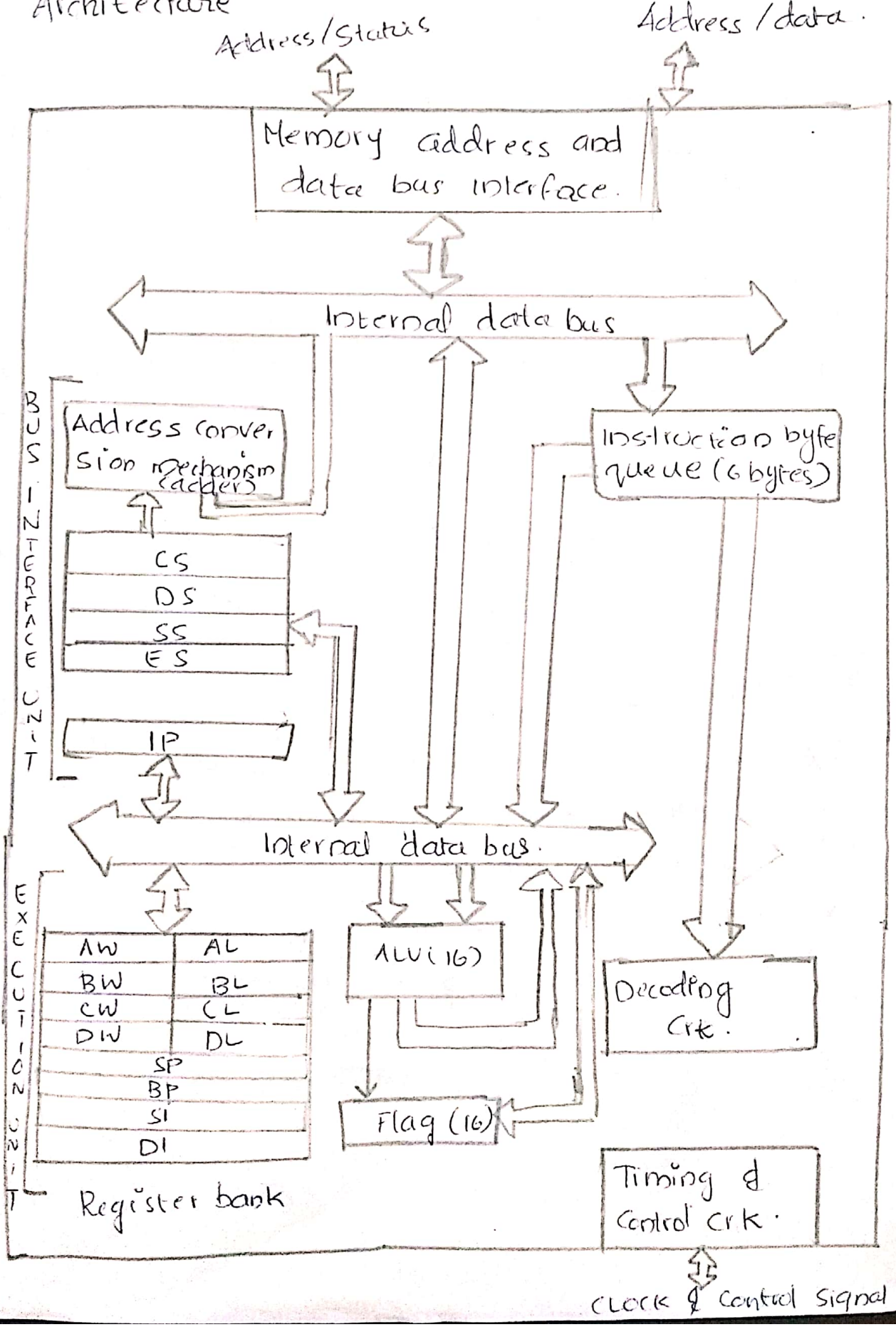
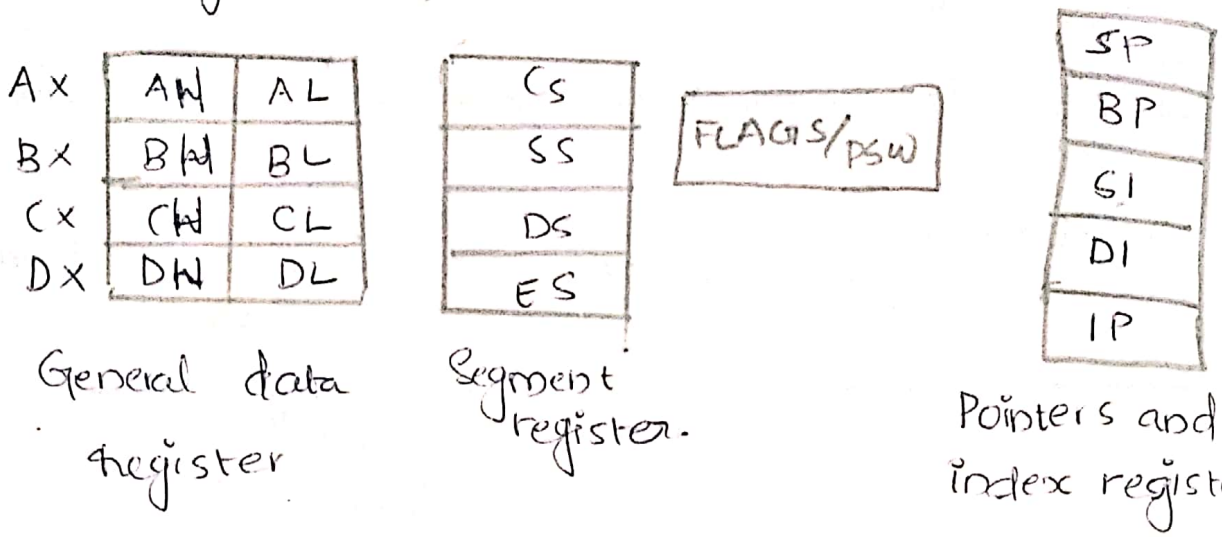
MODULE - 1

8086 MICROPROCESSOR.

Architecture



8086 Register Organisation :-

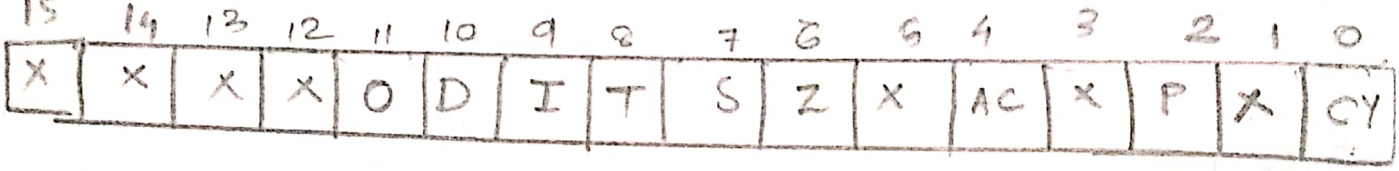


General data register

Segment register.

Pointers and index register

Flag register in 8086



General purpose → General data registers

Special purpose → Segment register / pointers and index registers
Flags/PSW

General purpose Register

AX → Used as a 16 bit Accumulator.

BX → AH → high bit AL → low bits
OFFSET can be stored in this register

CX → Used as a counter
In String loop instruction.

DX → Destination Address Storing register

Flag register

X → for future Use. fields

Z → zero flag.

1) condition codes (CY, P, AC, Z, S, O)
(carry/borrow, parity)

2) Machine control (D, I, T)

→ P is set if the lower byte has even no of ones in Accumulator.

→ AC → Acuilary carry.

→ Z → will be set if the all the bits of Accumulator is zero.

→ Machine control

⇒ D → Direction flag → If it is zero a string will be processed from lower to higher address

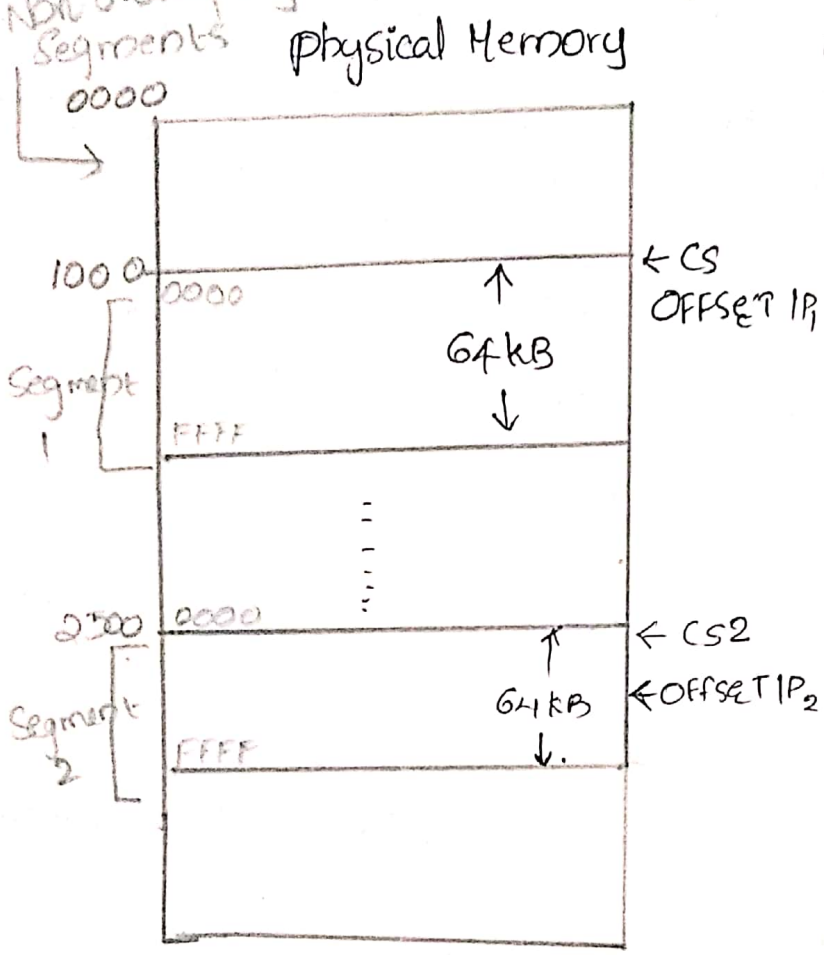
→ If the value is 1 a string will be processed from higher to lower address

⇒ I → Interrupt flag - If it is set (1) the maskable interrupt can be set by the CPU

maskable (Type 2 interrupt)
If it is not set nonmaskable interrupt set by the CPU.

⇒ T → trap → The executable code function in a Single step execution mode. Type 1 interrupt

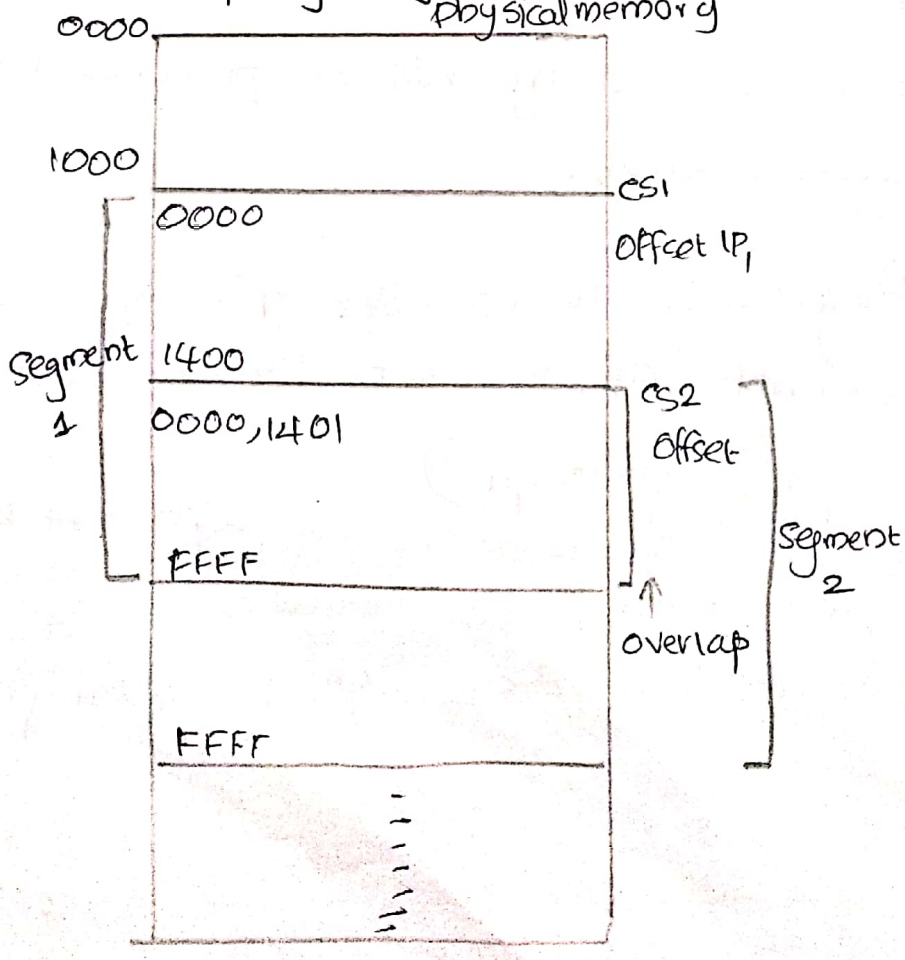
Non overlaping Segments



CS :- code Segment
SS :- stack Segment
DS :- Data Segment
ES :- Extra Segment

1M → divides in to
16 logical segment
1 segment → 64 KB

Overlaping Segments



Pointer
. ~~Index~~ registers

IP → Instruction Pointer

BP → Base pointer / change in offset we use it

SP → Stack pointer

Index register.

SI → Source address

DI → Destination address

→ IP along with CS gives the address

→ Instruction & byte queue.

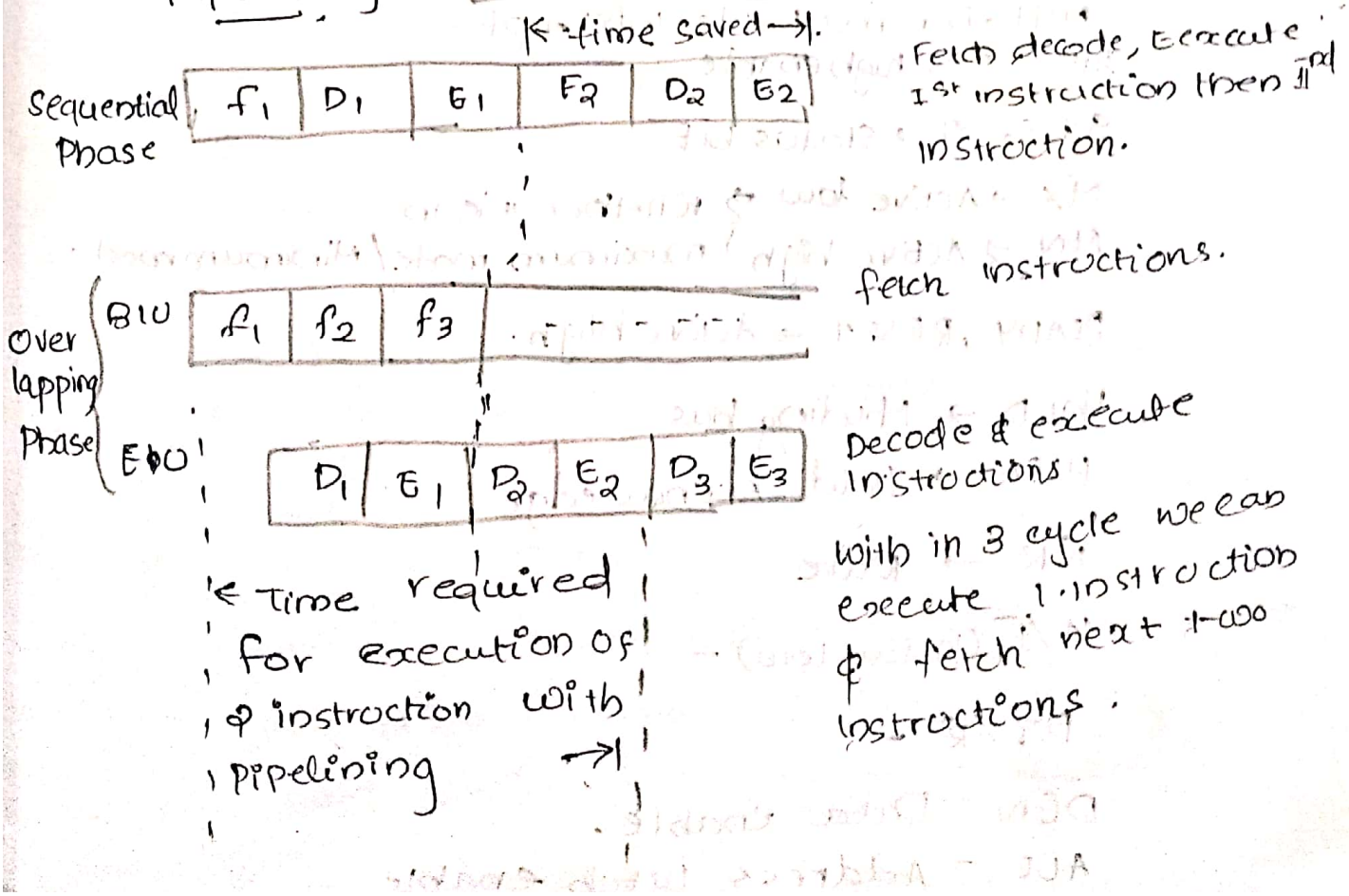
IMP → Pre-fetching →

→ 20 bit generating mechanism in address

Conversion mechanism.

Pipelining

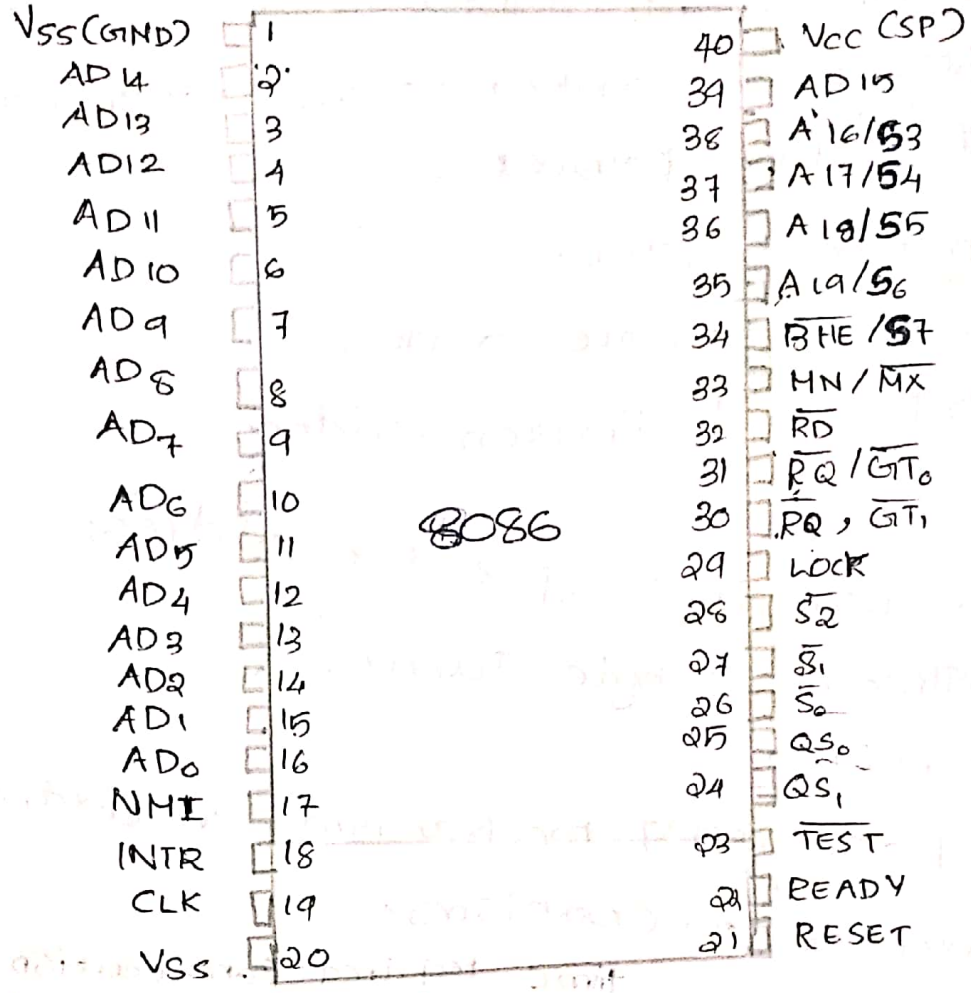
time required for execution of 2 instruction without pipelines



20/8/19.

PIN DIAGRAM. (DIP package)

Maximum mode Minimode



NMI - Non maskable interrupt.

BHE - Bus high enable

S7, S6 etc → Status bit

$\overline{MX}$ → Active low } Whether it is in
MN → Active high } maximum mode / Minimum mode

READY, RESET → Active high.

HOLD → Holding bus

HLDA → Hold Acknowledge

$\overline{WR}$ → Write

M/$\overline{IO}$ (Active low) –

DT/$\overline{R}$ –

$\overline{DEN}$ – Data enable.

ALE – Address latch enable

$\overline{INTA}$ - Interrupt Acknowledge.

→ 20 bit Address and 16 bit data

→ Multiplexing the Address line and Data lines AD_0 (PIN-16) to A_{14} (PIN-2)

→ $S_0 \ldots S_7$ Status bit. / Information about the which segment currently used.

→ Status bit multiplexing with $A_{16}, A_{17}, A_{18}, A_{19}$

→ $\overline{BHE}$ - Used for when the data take from the which partition of the memory

✓ 8086 Microprocessor is 16 bit CPU in 3 clock rates 5, 8, 10 MHz packaged in to a 40 pin DIP. (Dual in line packaging)

→ 8086 signals are classified into 3 groups

1. Signals having common for
2. Signal having funs in minimum (single processor) mode
3. Signal having funs in maximum (multiprocessor) mode

1. Signal description which are common for minimum & maximum mode.

a) $AD_{15} - AD_0$: Time multiplexed memory I/O and Data lines.

Address remains on line during T_1 state while data is available on data bus during T_2, T_3 & T_W (state for waiting time) & T_4 state

2. A_{19} / S_6
A_{18} / S_5
A_{17} / S_4
A_{16} / S_3

- These multiplex address & status lines during T_1 these lines have memory Address.
- During I/O operations these lines have low value(0).
- From state T_2 to T_4 these lines have Status Information.

S_6 → Always low
S_5 → Status of interrupt enable flag Bit
It is updated at the beginning of each clock cyc
S_4/S_3 → Indicate the segment register currently being used

S_4	S_3	Meaning
0	0	Extra segment
0	1	Stack segment
1	0	Code segment / non
1	1	Data segment

- Address bits are seperated from Status bit using ALE.

3. $\overline{BHE}$ / S_7 (Bus high enable / Status)

BHE signal is used to indicate transfer of data over higher order data bus ($D_{15} - D_8$). It is used to derive chip select of odd address memory bank or peripherals.
It is low during T_1 and during T_2, T_3, T_4 It has Status information.

$\overline{BHE}$	A_0	indication (Memory organization).
0	0	Whole word
0	1	upper byte from or to odd address
1	0	lower byte from or to even address
1	1	none

4. ~~(RD)~~ $\overline{RD}$ (Read)

Read signal on low indicates peripheral that process is performing a memory or I/O Operation.

$\overline{RD}$ is active low and shows the state for T_2, T_3, T_W of any read state.

5. Ready :- This active high signal is an ~~acknowledg~~ ~~ment~~ acknowledge that they have completed their data transfer.

6. INTR (Interrupt request) :- This signal is Sample during last clock cycle of each instruction to determine availability of a request. If any interrupt request is pending process enters signal acknowledgement cycle. Can be internaly masked by Reseting Interrupt Enable flag.

7. $\overline{TEST}$:- This I/P is examine by a wait instruction. If TEST goes low execution will continue else processor will remain an Ideal state.

8. NMI (Non maskable interrupt) :- (level triggered) Edge triggered I/P which process Type 2 interrupt.

- A transition from low to high initiates the interrupt respond to the current instruction.
- It is not makable by software

9. RESET :- this I/P causes the processor to terminate current activity & start execution from FFFOH.
   Signal must be active high for atleast 4 clock cycle

10. CLK :- clock I/P provides basic time for process operation or bus control activity.
    It is an asymmetric square wave with 33% of duty cycle

11 VCC :- +5 volt power supply.

12 GND :- Ground internal circuitary

13 MN/$\overline{MX}$:- It indicates whether it is minimum mod/maximum mode 0 - Max, 1 - Min

PINS FOR MINIMUM MODE OPERATION

1. M/I_O :- Specify memory operation.
   M=0 - memory operation
   I_O=1 - I/O operation.

$\overline{INTA}$:- Activ low → interrupt Acknowledgement

ALE :- Check whether it have activate address

DT/$\overline{R}$:- high - transmit data
   low - Receive data

$\overline{DEN}$:- Data enable: Data coolive in data line.

Memory/IO organization page no: 14 :17 21, 22 23.

HOLD/HLDA :- HOLD the bus. HLDA is for bold acknowledgment

$\overline{WR}$:- Indicate write operation.

PINS FOR MAXIMUM MODE OPERATION

1.

$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	Indication
0	0	0	Interrupt Acknowledge
0	0	1	Read I/O port
0	1	0	Write I/O port
0	1	1	Halt
1	0	0	code Access
1	0	1	Read memory
1	1	0	Write memory
1	1	1	passive

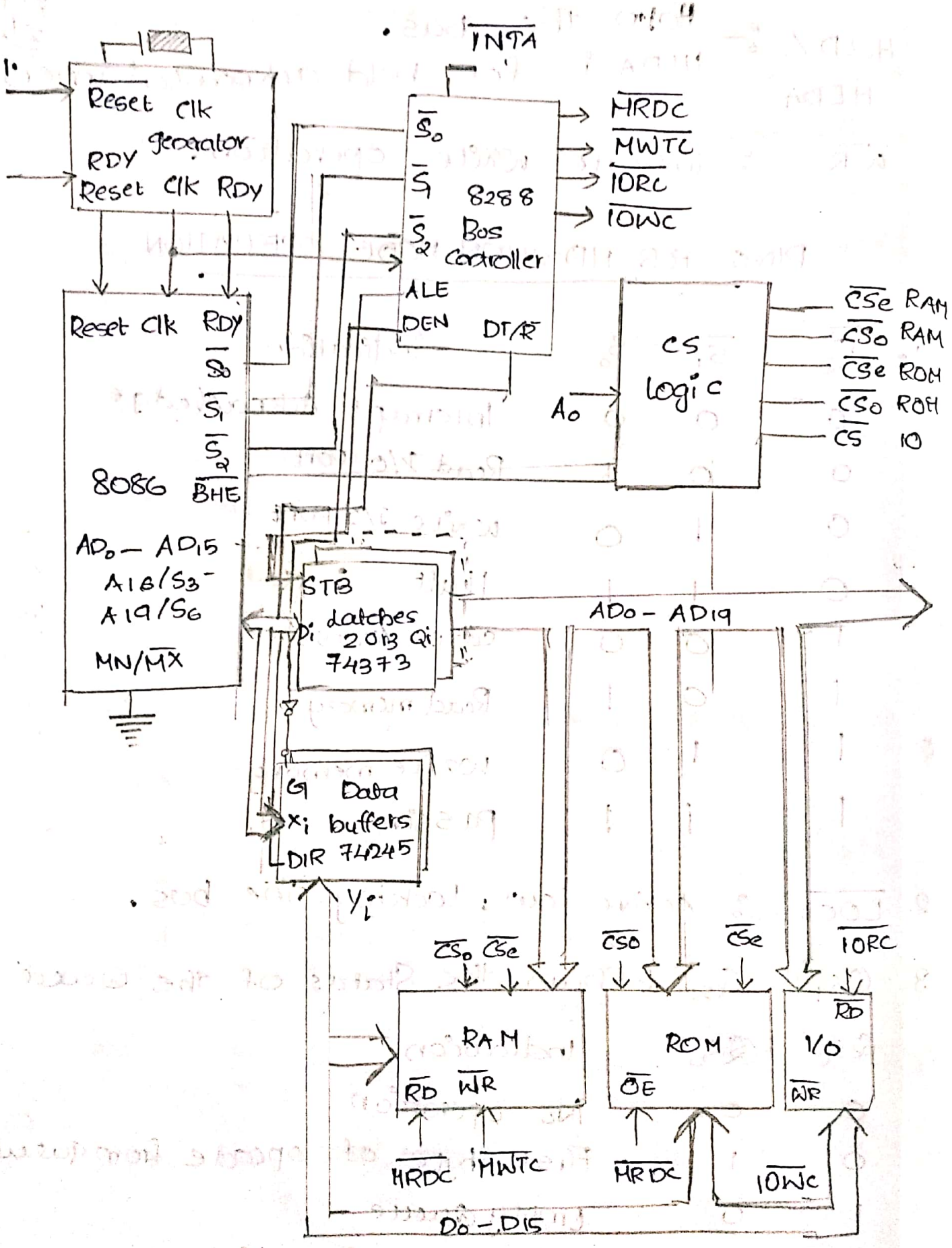
2. $\overline{LOCK}$:- Active low; locking the bus.

3. QS_1 QS_0 :- Shows the Status of the Queue.

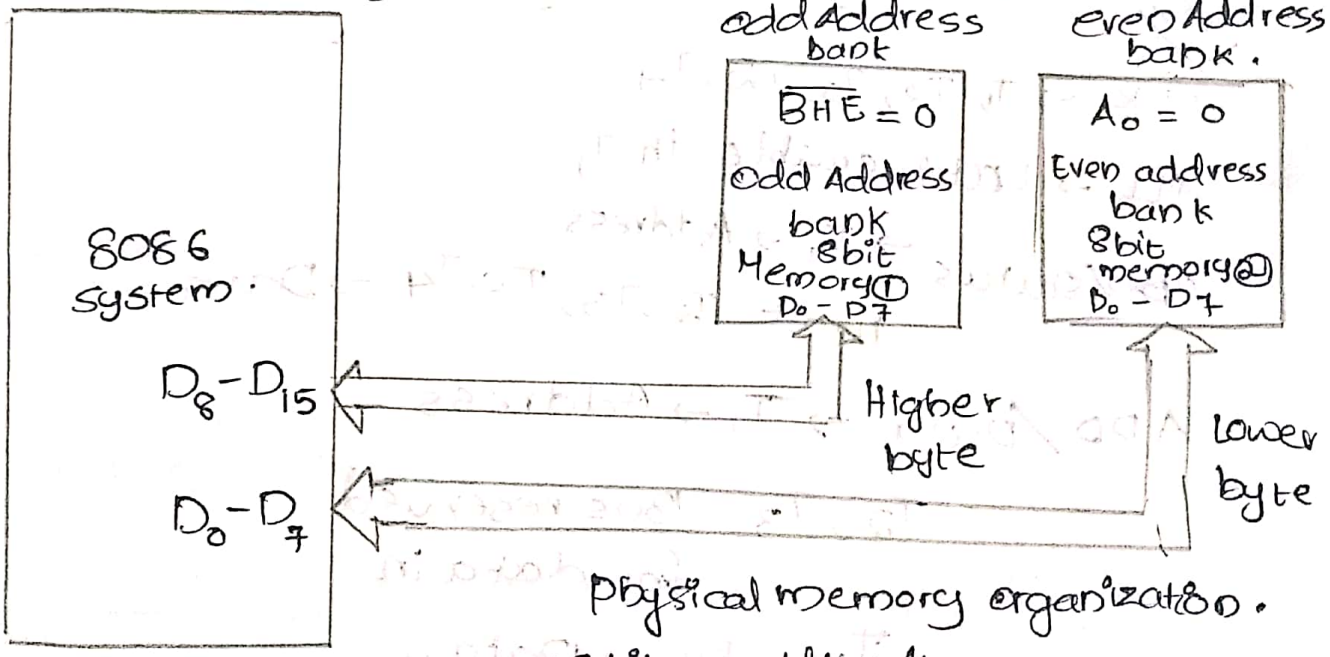
QS_1	QS_0	Indication
0	0	No operation
0	1	First byte of opcode from queue
1	0	Empty Queue
1	1	Subsequent byte from Queue

4. $\overline{RQ}$ / $\overline{GT_0}$ (- having high priority).

$\overline{RQ}$ / $\overline{GT_1}$:- Bus Request & Bus grand



2. 8086 have 1mb memory. It partition in to two 512 kB, 512 kB.



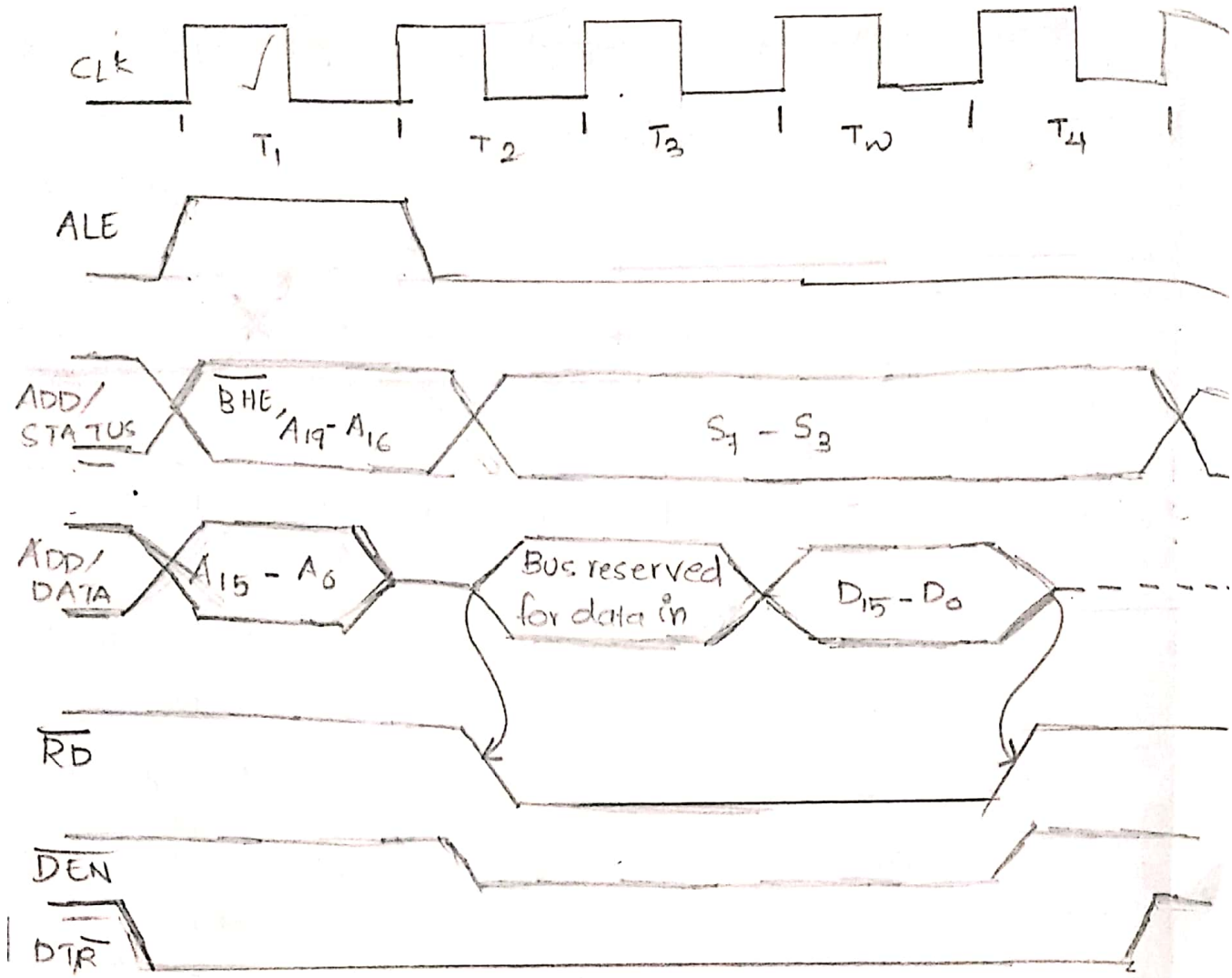
Physical memory organization.

16 bit split in to two → 8 bit in odd bank
→ 8 bit in even bank

Read entire word if ~~word~~ starting is even address in one memory cycle. bank

Start from odd bank then we need two memory cycle. $\overline{BHE}$ & A_0 controls the odd & even bank.

1) Minimum Mode



Note: Read cycle Timing Diagram for minimum mode

CLK → T1, T2, T3, TW, T4

ALE → Latch enable in T1

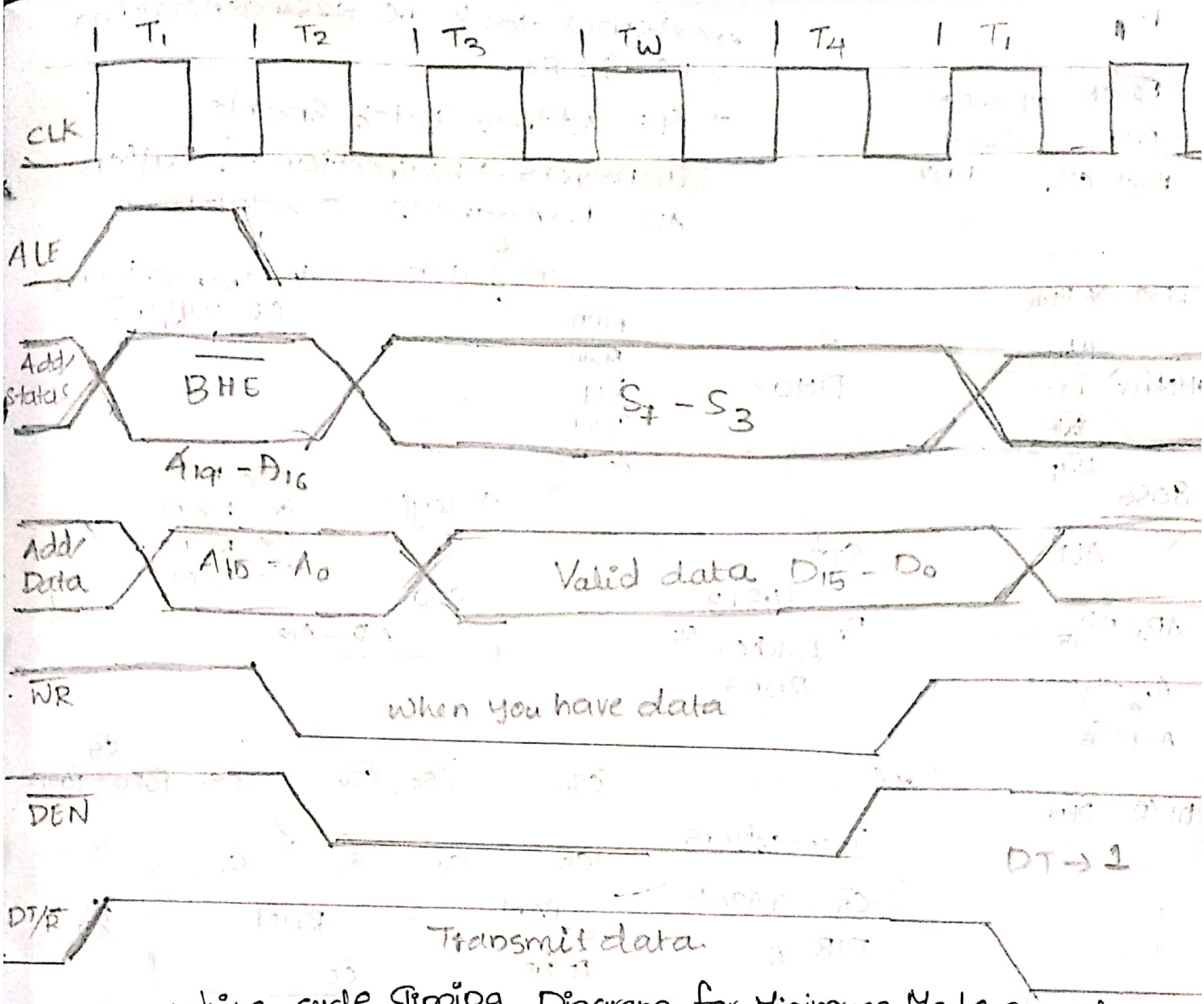
ADD/Status → T1 → Address
next T2, T3, TW, T4 → Data.

ADD/Data → T1 → Address
T2, T3, Bus reserved for data in
TW, T4 → Data.

RD → Read when reserving the data from bus in T2 & T3 State

DEN → Data enable in T2 to T4 States

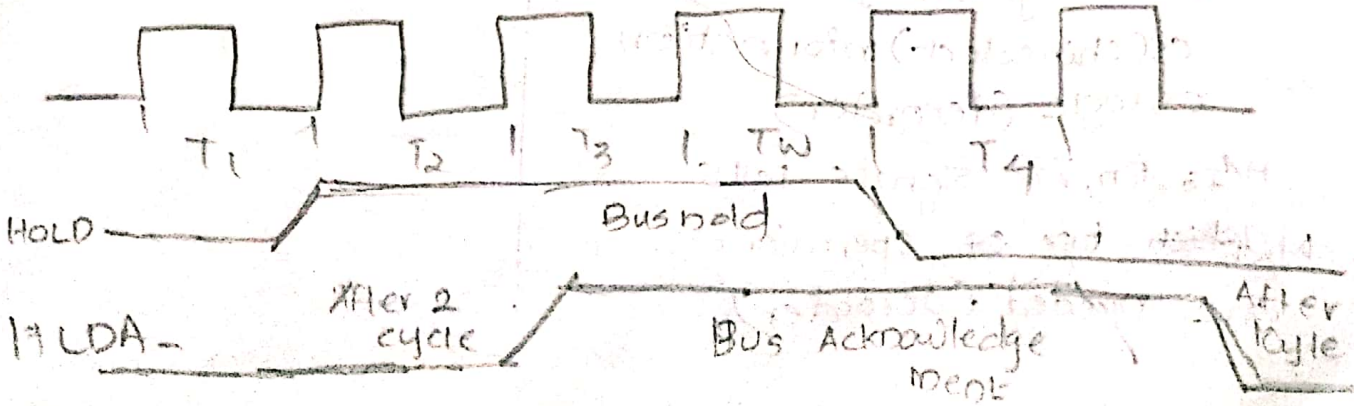
DT/R → Receive data T1 to T4 States



Write cycle timing Diagram for Minimum Mode operation

M /IO	RD	DEN	Transfer Type
0	0	1	I/O read
0	1	0	I/O Write
1	0	1	Memory read
1	1	0	Memory Write

Minimum mode 8086 System.



1)

→ external clock IC 8284 generating IC 8284

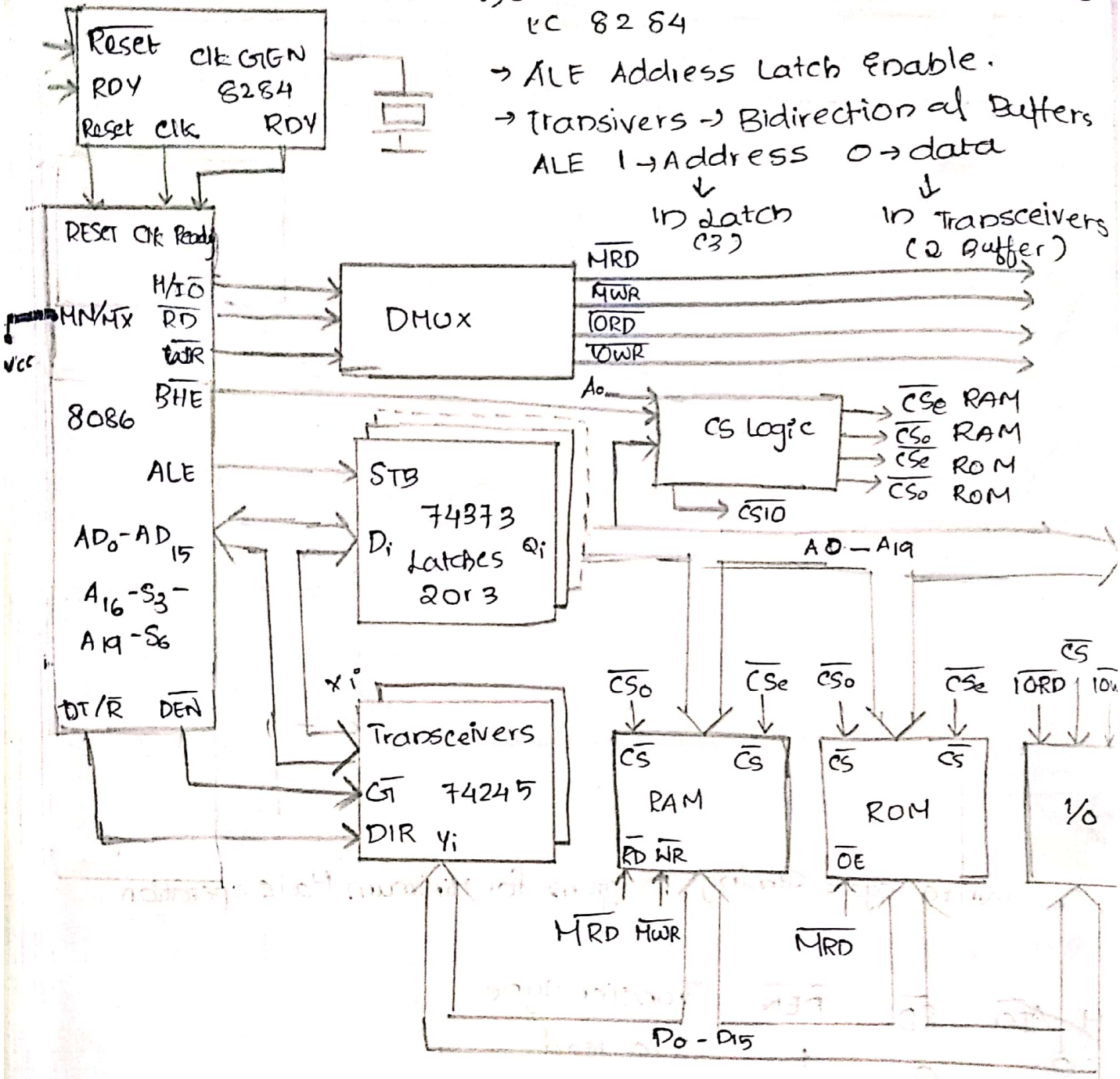
→ ALE Address Latch Enable.

→ Transivers → Bidirectional Buffers

ALE 1 → Address 0 → data

↓ ↓

In latch (3) In Transceivers (2 Buffer)



Minimum mode 8086 System.

DEN tells data is available

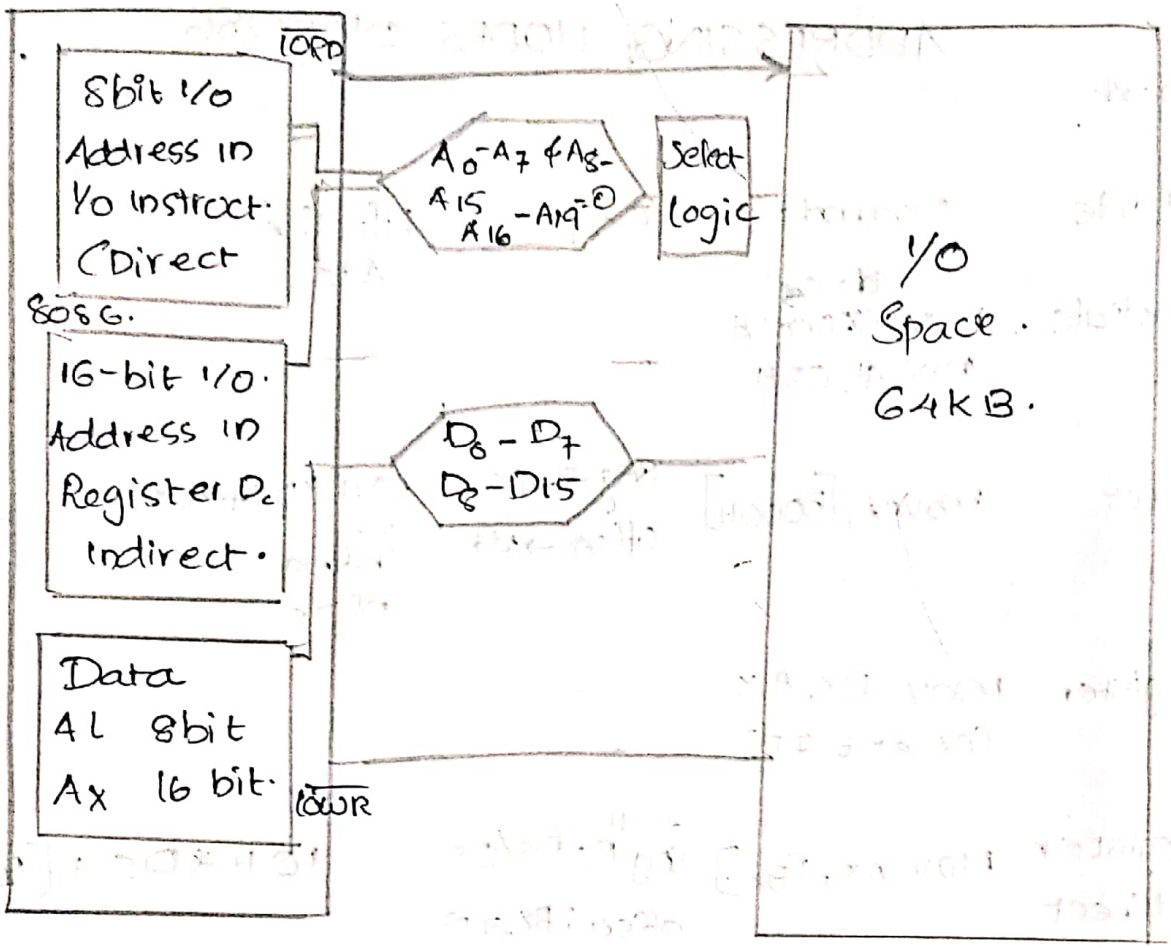
DT/R defines whether the data transmit / data Receiver

BHE / A0 together gives the CS (chip select) information CS logic (decorder)

M/IO, RD, WR signals tells Which ~~Which~~ type of operations core needed (decorder)

RAM, ROM are 2 banks ~~every bank~~ for each, odd bank, even bank.

I/O Organization.



A_{16} - A_{19} → low when we perform I/O operation.

I/O space have 64 kB.

A_0 - A_7 → pass lower byte

A_8 - A_{15} → pass Upper byte

Dx → Store I/O ~~Address~~ destination Address in it.

I/O operation (16 bit transfer)