



**8051 ARCHITECTURE**  
**8051 REGISTER ORGANIZATION**

## 8051 Vendors

- Intel introduced 8051, referred as MCS51, in 1981
  - The 8051 is an 8-bit processor
  - The CPU can work on only 8 bits of data at a time
- The 8051 family has the largest number of diversified (multiple source) suppliers
  - Intel (original)
  - Atmel
  - Philips/Signetics
  - AMD
  - Infineon (formerly Siemens)
  - Dallas Semiconductor/Maxim

## Main features of 8051

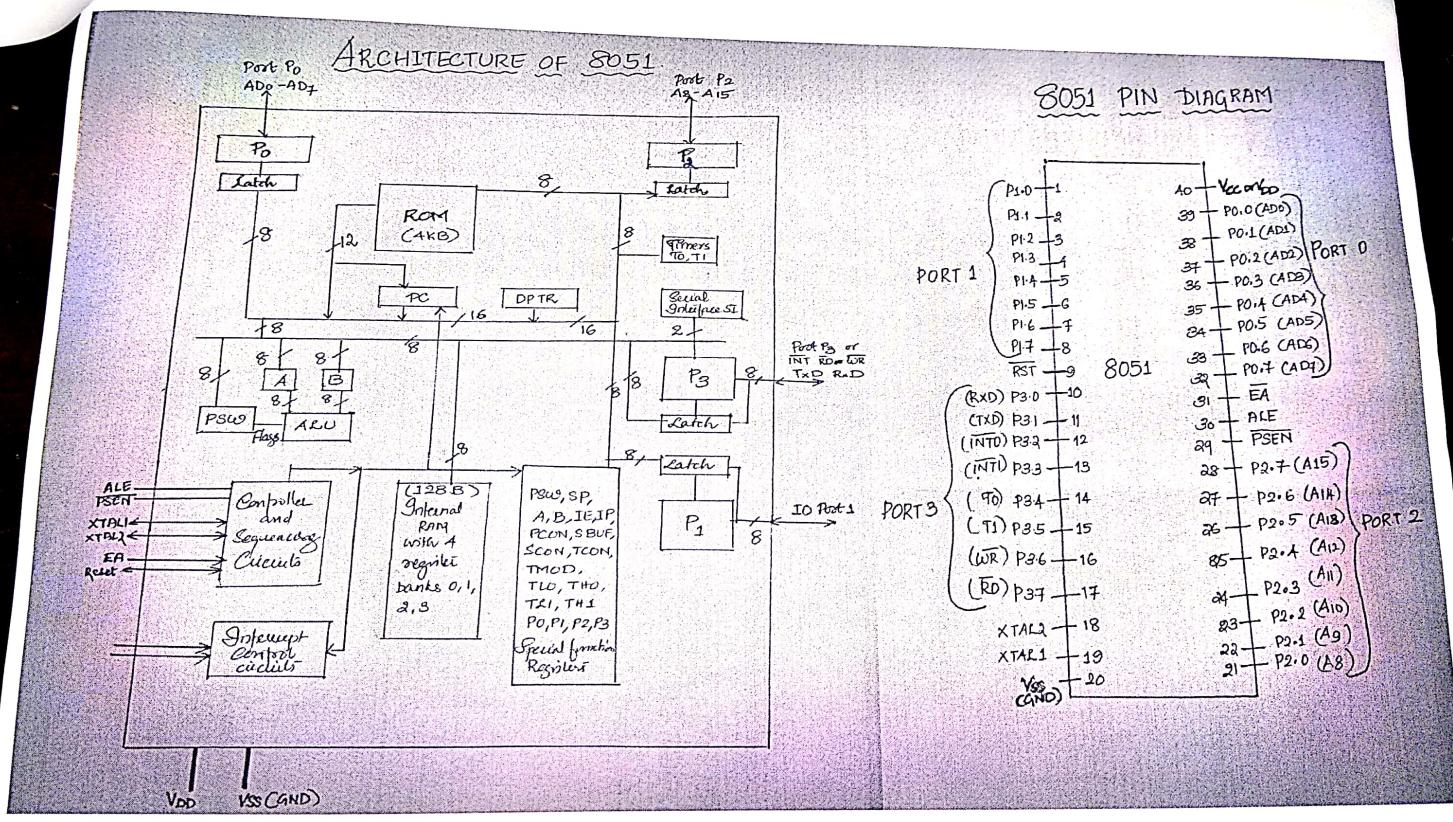
<b>Feature</b>	<b>8051</b>
ROM (on-chip program space in bytes)	4K
RAM (bytes)	128
Timers	2
I/O pins	32
Serial port	1
Interrupt sources	6

## Features of 8051

- 8051 is a DIP IC with 40 pins dedicated for various functions such as I/O, RD, WR, address, data, and interrupts.
- 8051 processing unit has
  - Control and sequencing circuit
  - Oscillator for generating clock
  - Reset circuit
- 8051 contains embedded program in ROM (4KB)
  - 8051 can work in Single mode (internal devices and circuits) and Expanded mode (address and data bus signals)
- Each program needs temporary variables
  - 128 B RAM (with register banks 0,1,2,3)
  - Special Function Registers (SFRs) : PSW, A, B, IE ,IP, SCON, TCON, SMOD, SBUF, PCON, TLo, THo, TL1, TH1, Po, P1, P2 , P3, SP

## Features of 8051

- Stack pointed by a special register Stack Pointer (SP – 8 bit)
- Program Counter (PC)
  - Lower byte at bus A<sub>0</sub>-A<sub>7</sub> / data bus D<sub>0</sub>-D<sub>7</sub> : Expanded mode (Port 0 : Single mode)
  - Higher byte at bus A<sub>8</sub>-A<sub>15</sub> : Expanded mode ( Port 2 : Single mode)
- Data Pointer (DPTR)
  - To access data from external memory
  - Lower byte (DPL) higher byte (DPH)
- IO devices connection through Ports : Port 0, 1, 2, 3
- Interrupts
  - Two external pins INT<sub>0</sub> and INT<sub>1</sub>
  - Interrupt control circuit
  - Two SFRs IP (interrupt priority) and IE (interrupt enable)
- Serial interface
- Two programmable timers/event counters for real time control of events and tasks – T<sub>0</sub> and T<sub>1</sub>



## Use of subunits and signals

Symbol	Full form	Use
PC	Program Counter	16 bit address pointer PC holds program memory address of instruction currently being fetched. PC consists of 2 bytes PCH(higher) and PCL (lower)
DPTR	Data Pointer	16 bit address pointer, it holds external data memory address of data being currently fetched. DPTR consists of DPH(higher) & DPL (lower)
A	Accumulator	8-bit register, saves an operand for ALU operation and accumulates final result in A
B	B register	8-bit register, saves second operand for ALU, accumulates part of result
ALU	Arithmetic & Logic	Unit performing arithmetic and logic operations
PSW	Processor Status Word	8-bit register to save status and state bits

## Use of subunits and signals

Symbol	Full form	Use
P <sub>0</sub>	Port 0	8 bit port for I/O in single mode & data bus /lower order address signals ADo-AD <sub>7</sub> in expanded mode
P <sub>2</sub>	Port 2	8 bit port for I/O in single mode & higher order address signals A <sub>8</sub> -A <sub>15</sub> in expanded mode
P <sub>1</sub>	Port 1	8 bit port for I/O in single mode
P <sub>3</sub>	Port 3	8 bit port for I/O in single mode & used for Serial Interface(SI) signals, timer T <sub>0</sub> and T <sub>1</sub> inputs, interrupts INT <sub>0</sub> and INT <sub>1</sub> inputs, sending RD and WR signals for memory read and write in expanded mode
SI	Serial Interface device	Serial IO operations. 2 modes : Full duplex ( input and output at an instance) UART , half duplex (input or output at an instance) synchronous communication; 2 pins of P <sub>3</sub> : RxD, TxD ; 2 pins of P <sub>3</sub> : DATA and CLOCK

## Use of subunits and signals

Symbol	Full form	Use
To & <b>T<sub>1</sub></b>	Timers To and T <sub>1</sub>	Timing devices; it has four registers TH <sub>1</sub> , TL <sub>1</sub> , TH <sub>0</sub> , TL <sub>0</sub>
<b>SFR</b>	Special Function Registers	SP, PSW, A, B, IE, IP, Po, P <sub>1</sub> , P <sub>2</sub> , P <sub>3</sub> , SCON, TCON, SMOD, SBUF, PCON, TLO, TH <sub>0</sub> , TL <sub>1</sub> , TH <sub>1</sub>
<b>ROM</b>	Read Only Program memory	Masked ROM, EPROM, flash EEPROM of 4kb , internally connects to PC bus of 12 bits; Address is between ox0000 & oxoFFF
<b>Internal RAM</b>	Internal Random Access Memory	RAM is 128Bytes for read and write, indirectly and directly addressable; Address between ox00 & ox7F
<b>Register Banks</b>	Four set of registers	Four registers banks each of 8 registers; part of internal RAM

## Use of subunits and signals

Symbol	Full form	Use
<b>XTAL<sub>1</sub> &amp; XTAL<sub>2</sub></b>	Pins to Crystal	Pins to crystal oscillator circuit,; 12MHz crystal in 8051
<b>EA</b>	External Enable	To enable use of external memory addresses
<b>RST</b>	Reset pin	Reset circuit input ; let processor reset and synchronize with external peripheral devices
<b>INT<sub>0</sub> INT<sub>1</sub></b>	Interrupt Pins	Two External interrupts, Active from low
<b>V<sub>cc</sub> (V<sub>dd</sub>) and V<sub>ss</sub> (GND)</b>	Voltage supply pin & Ground pin	V <sub>cc</sub> - 5V supply; V <sub>ss</sub> – Ground connections
<b>PSEN</b>	Program Store Enable	Activates for reading external program memory byte
<b>RD</b>	Read	Activates for reading a byte from external program memory byte
<b>WR</b>	Write	Activates for writing a byte to external program memory byte