Module : 1

17/09/19

8086 MICROPROCESSOR

Register Organisation of 8086

AX	AH	AL
BX	BH	BL
CX	CH	CL
DX	DH	DL

General Data registers

CS
SS
DS
ES

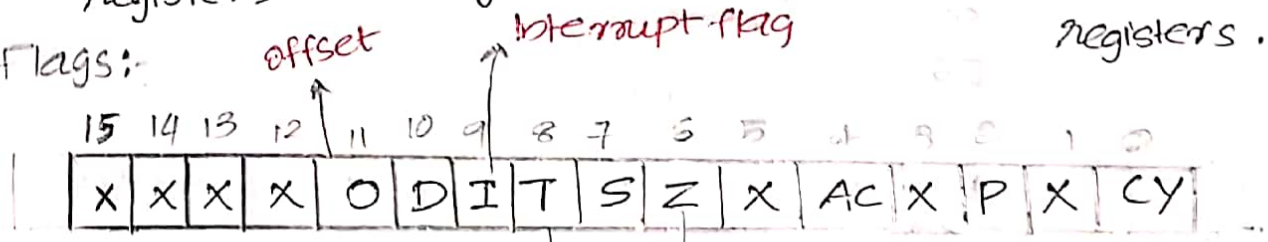
Segment registers

FLAGS/PSW

SP
BP
SI
DI
IP

Pointers and index registers.

Flags:



- 4 categories of register
- All the registers are 16 bit registers.

Normaly,
- They divided into 2
  - general purpose - General data registers
  - special purpose - segment, flag, Pointers & index registers.

General purpose: splited ← Higher / lower

- AX – 16 bit accumulator
- BX – Offset (The distance b/w base address & particular location)
- CX – Counter in strings & loops
- DX – Destination setting.

(String loop instruction)

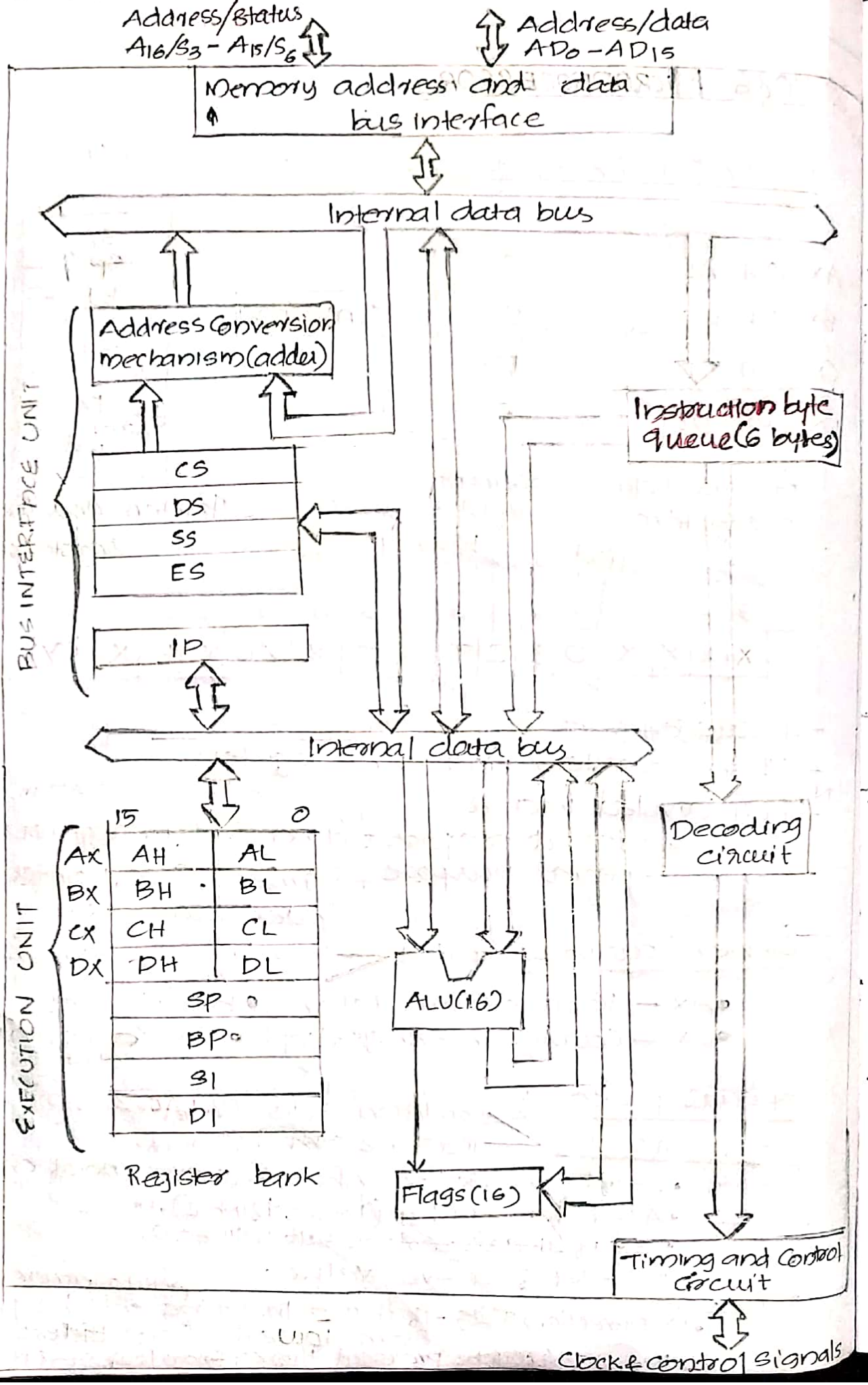
Special purpose:

- Flag register ← Condition codes CY, P, AC, Z, S, O (affected by accumulator / if any opn done in accumulator) / Machine control co: D, I, T

Condition
- P – is set if lower byte has even no. of one's
- AC – After 3rd bit (lower nibble), there is any carry. (3rd bit → 4 bit)
- Z – if all are zero, result will be 0.
- S – set if a –ve value.

Machine control
- D – Direction flag – if it is 0, the string will be processed from lowest to highest add. (auto incrementing)
- if it is 1, the string will be processed Highest to lowest – autodecrement

8086 Architecture

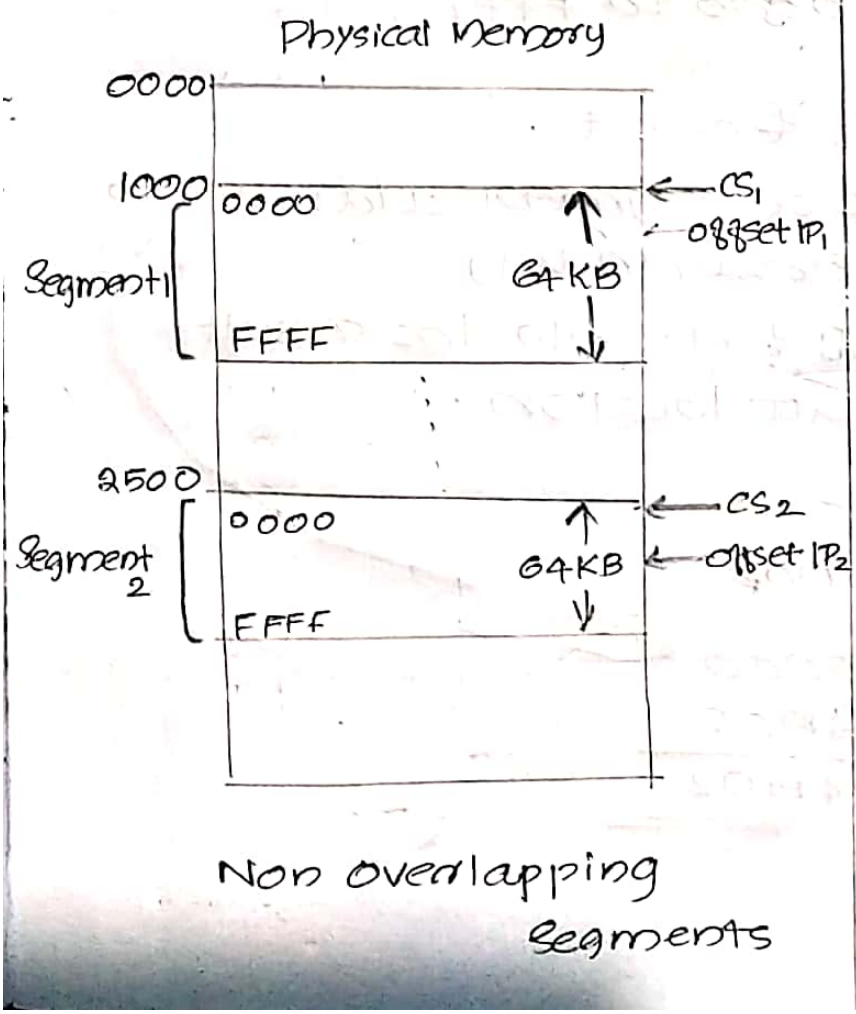


1st MP – Intel 4004 – 1971 – 4 bit MP (specific ins)
Intel 8008 – 1972
Intel 8080 – 1974 – For General purpose (1st General purpose MP)
Intel 8085 – 1975 – 8 bit MP
Intel 8086 – 1978 – 1st 16 bit MP
- Register capacity ↑ses
- segmented memory
- fast
- 40pin chip

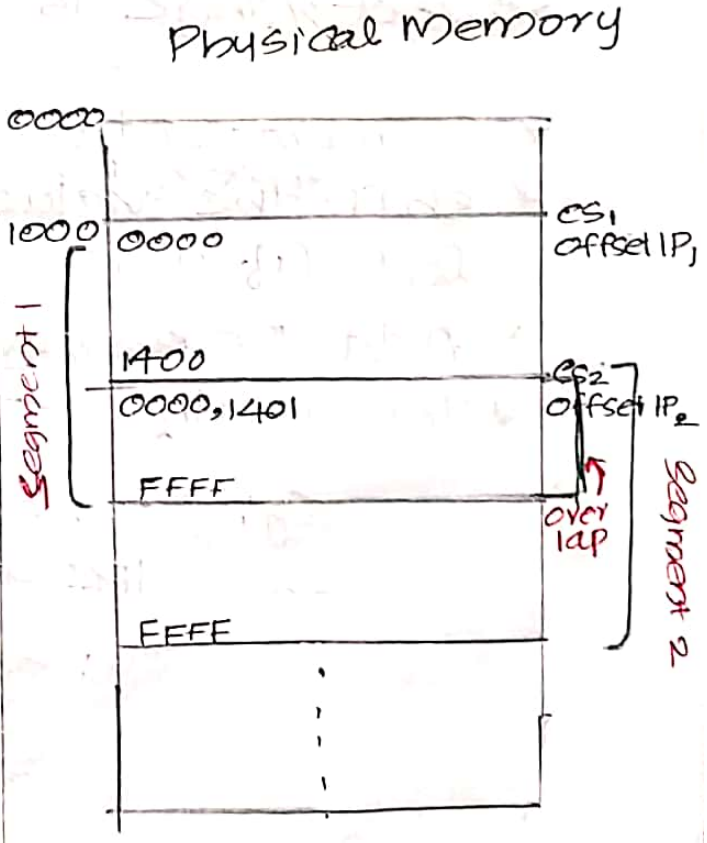
Machine control (balance)

• I – Interrupt flag
if it is set, the maskable (Type 2 interrupts) interrupts organised
↳ It can be change in b/w

• T – Trap (another type of interrupt.
If it is set, executable code will function in a single step execution mode (Type 1 Interrupts) organised.



Non overlapping Segments



Overlapping Segments

• Segment register

CS - Code Segment - Executable codes
SS - Stack Segment - the space for store stack
DS - Data Segment } Only stores datas.
ES - Extra Segment. } → source
→ Set destination.

→ For 1MB (memory capacity), 20 bit lines must be need.

→ Segment registers always keeps base address.

→ 1MB is divided into 16 logical segment.

→ each segment has 64 KB range.

→ Both base address & offset points to the exact location.

→ Offset range is 0000 to FFFF

* Segment address & offset.
* Shift 4 bit of the value (data) of segment address into left (if it is binary)
* Add the offset into the result.
* This is the exact location.

Eg: CS : 5000
IP : 4A02

CS : 50000
4A02
54A02

• Pointers and Index registers

SP – Stack Pointer [Points to a location]

BP – Base Pointer [to change/set offset]

IP – Instruction Pointer [this points to the next instruction to be executed]

SI – Destination index of source [mainly in string operation].

DI – Destination value present.

18/07/19

8086 Architecture

Instruction byte queue (6 bytes)

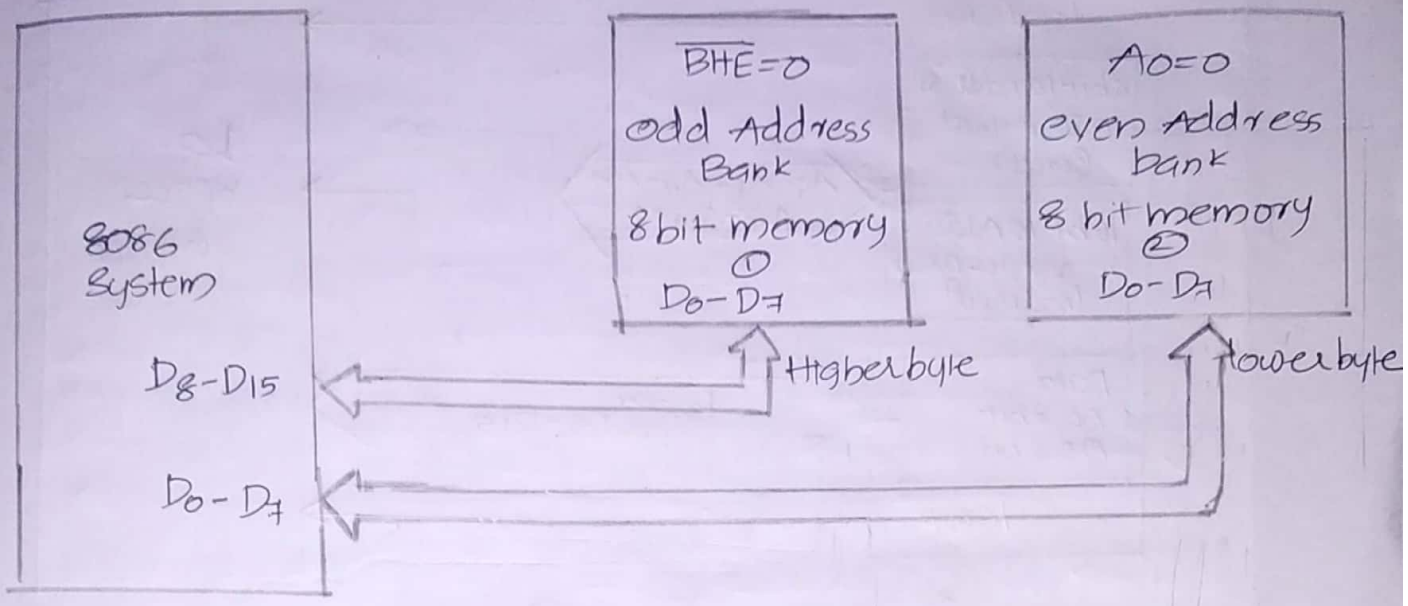
* It is the most important factor in the architecture.
* It fetches 6 bytes of instructions from memory into processor. This process is known as prefetching.
* if a fn call happens, it go to a new location & it clear all instructions.

Address conversion mechanism (adder)

* It generate 20 bit location.
* The location go to the internal data bus. So this part is called bus interface unit.

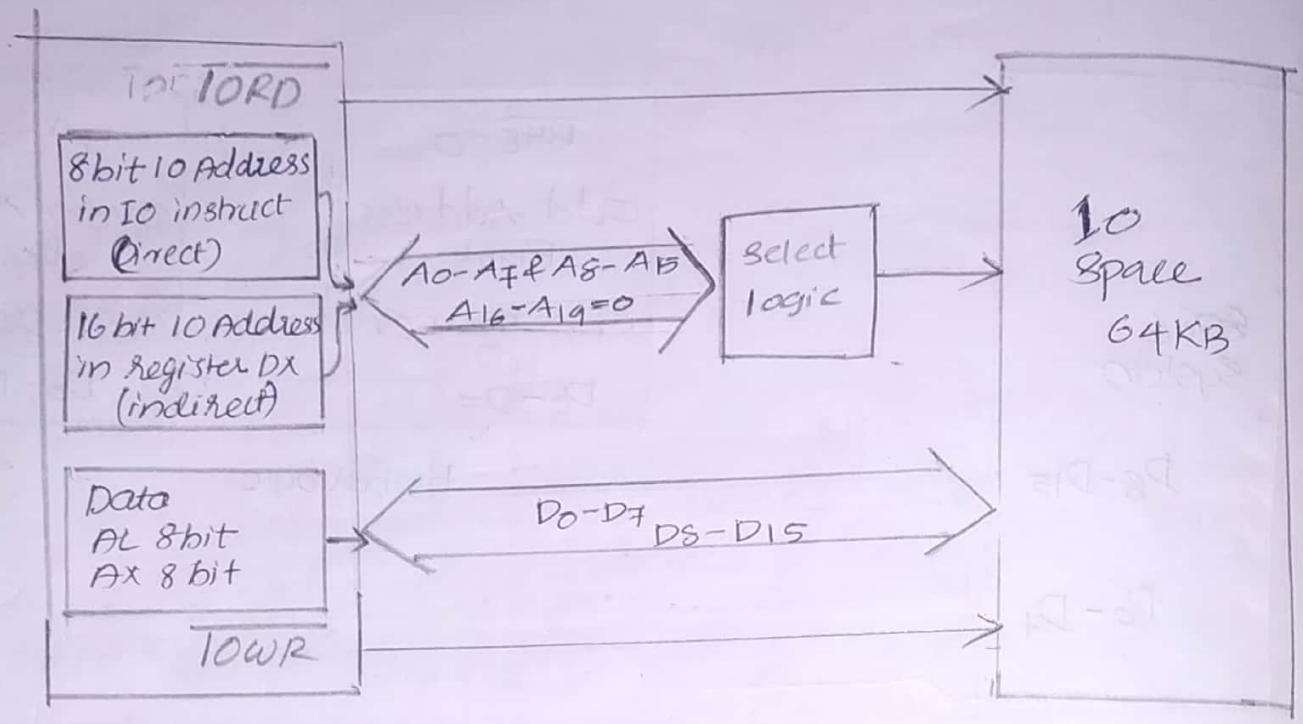
Not complete
5 pages

24/09/19 Physical memory organisation



- 8086 system has 1MB memory.
- 1MB memory partion into 2 512 KB & 512 KB.
- 16 bit (1 word) split into 2 8 bit in even bank & 8 bit in odd bank.
- Address starting from odd no's that stores in odd address bank & address starting from even no's that stores in even address bank.
- Both BHE & A0 will decide which bank will be select. They controls the banks.
- Read (fetch) entire word, if address starting from even address bank in one memory cycle.
- If add starts from odd bank, Then we need 2 memory cycle. 1st takes higher byte & go to take the lower bytes.
- BHE = Bus High Enable - control odd no's - active low signal

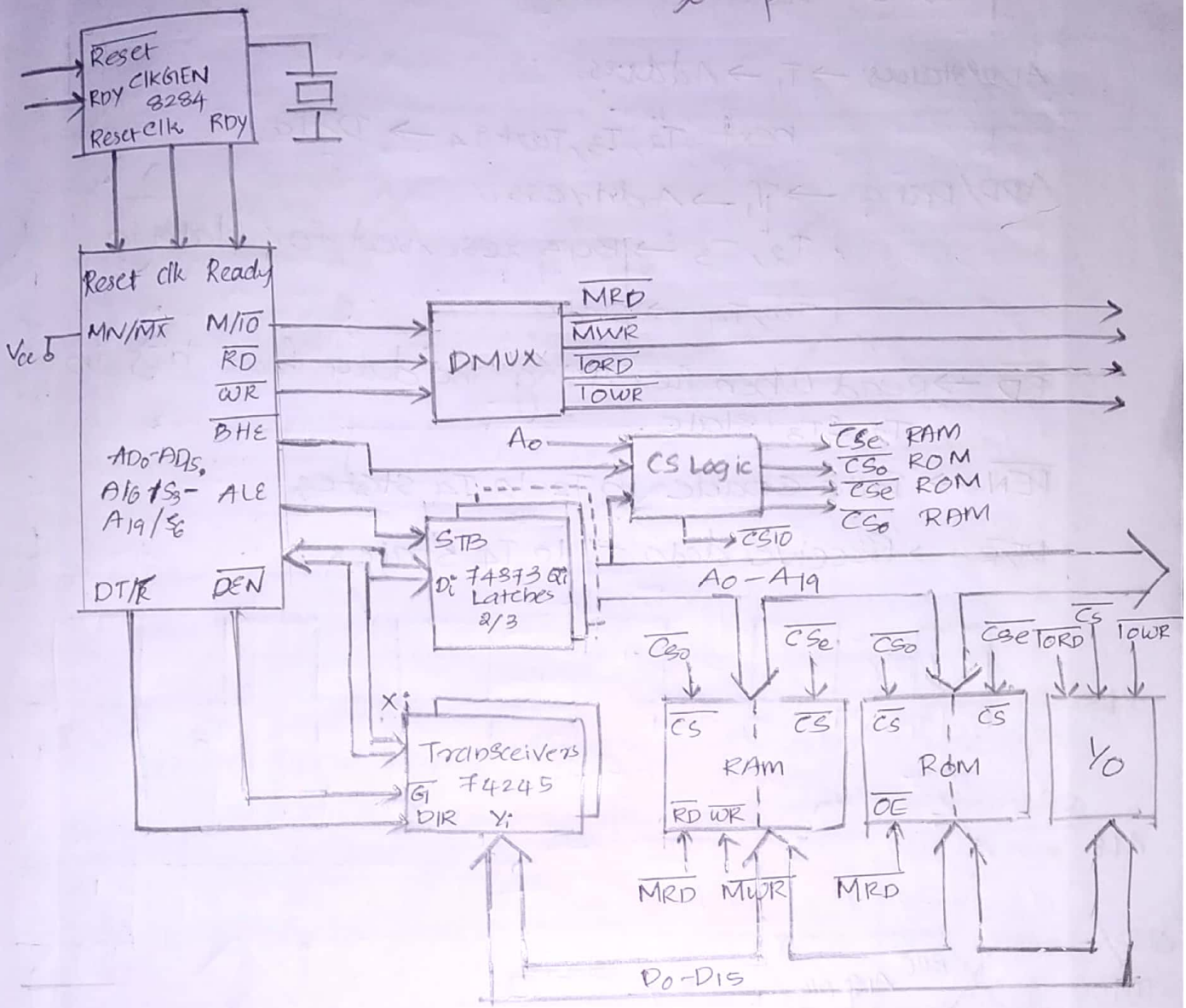
8086 IO Addressing (IO Organization)



- A_{16}-A_{19} = 1000 when we perform I/O operation.
- I/O space have 64 KB locations.
- 1MB memory
- 20 bits are required.
- A0-A7 : pass lower byte
  A8-A15 : pass upper byte.
- Dx → store I/O destination address in I/O operation (16 bit transfer)

Minimum mode 8086 system & Timings

Serial processor



- $\overline{DEN}$ tells data is available
- DT/$\overline{R}$ defines whether the data transmit / data receiver
- $\overline{BHE}$/A0 (Bus High Enable) together gives the CS (Chip select) information & CS logic (decoder).
- M/IO, $\overline{RD}$, $\overline{WR}$ signals tells which type of operations are needed (decoder)
- RAM & ROM are 2 banks.
- for each odd bank, even bank
- external clock generating IC 8284
- Transceivers = Bidirectional buffers.
- CLK → T_1, T_2, T_3, T_{w0}, T_4 (Read cycle) notes
- ALE → Add. Latch Enable in T_1

ALE ⇒ 1, Address in Latch (3 buffer)
⇒ 0, Data in Transceivers (2 buffer)

ADD/Status → T_1 → Addres

next T_2, T_3, Tw & T_4 → Data

ADD/Data → T_1 → Address

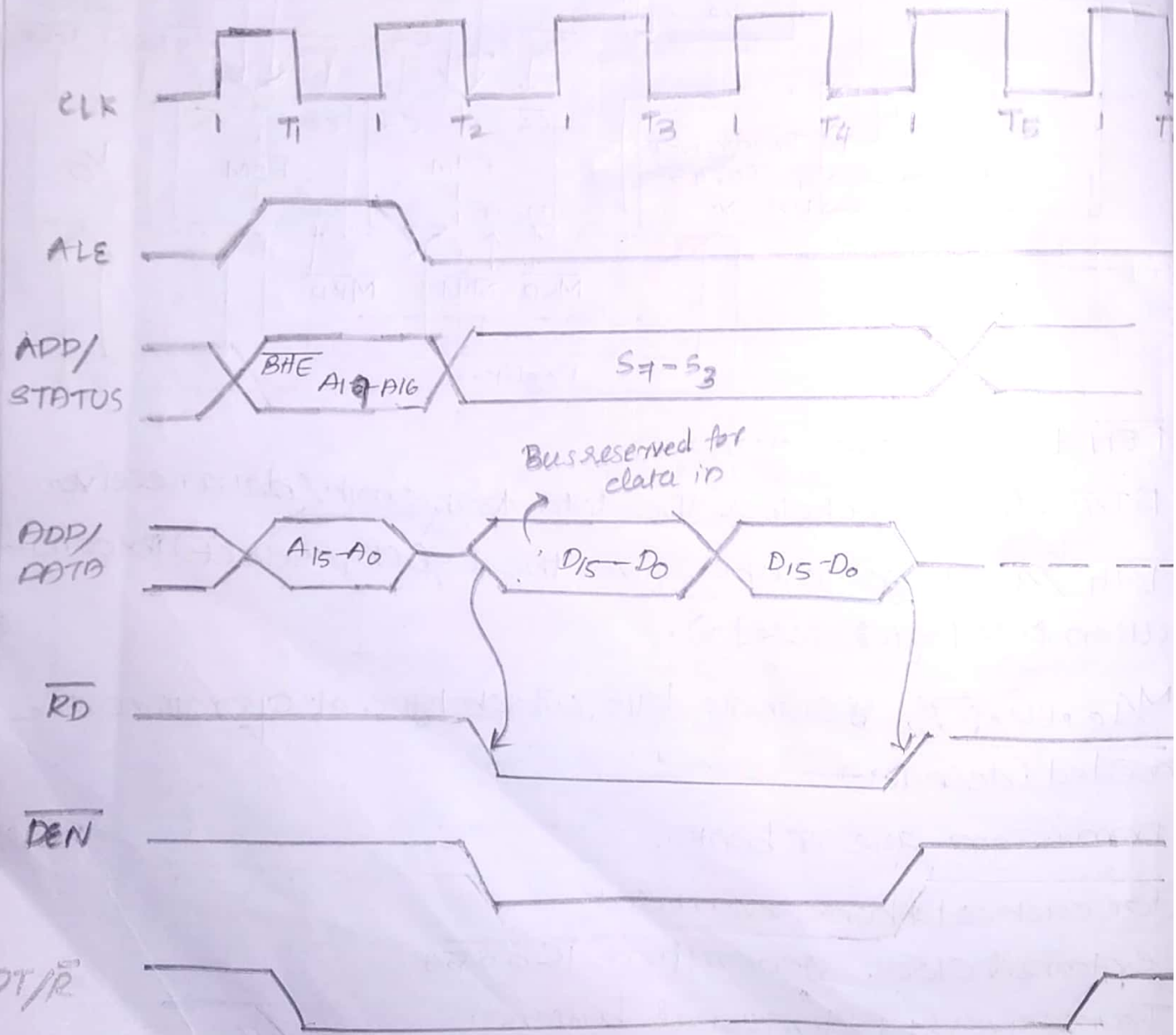
T_2, T_3 → Bus reserved for data in

Tw, T_4 → Data

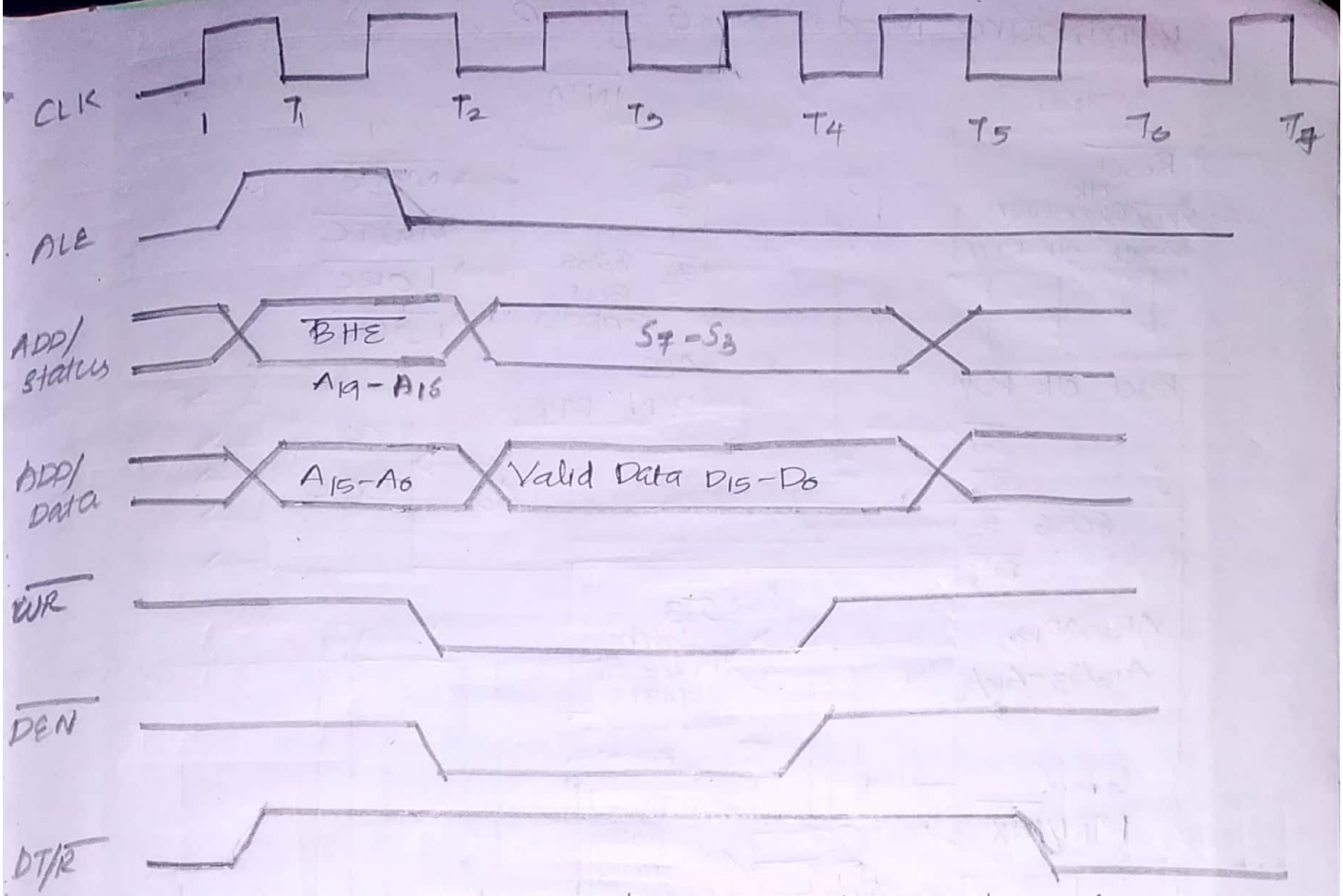
$\overline{RD}$ → Read when reserving the data from bus in T_2 & T_3 state.

$\overline{DEN}$ → Data enable in T_2 to T_4 states

DT/$\overline{R}$ → Receive data T_1 to T_4 States.



Read Cycle Timing Diagram for Mini. Mode

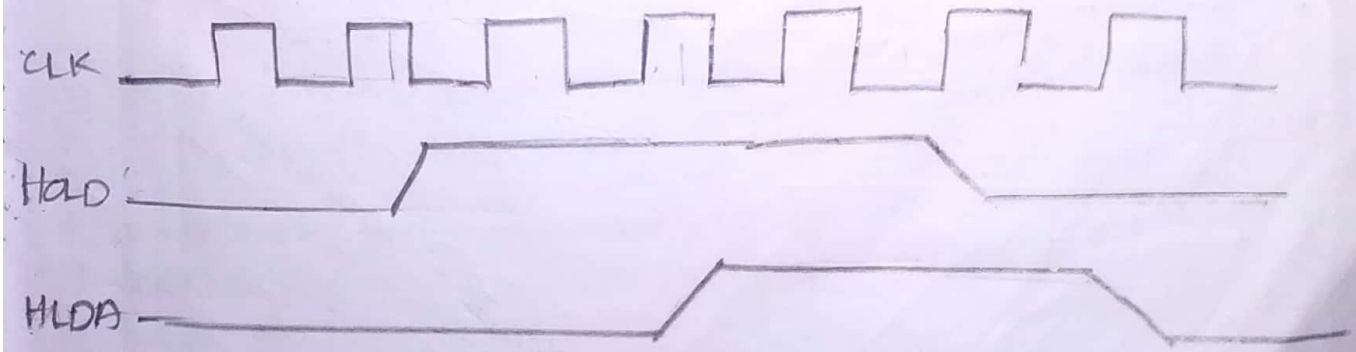


Write cycle Timing Diagram for mini. mode opn.

M/IO, RD, WR signals indicate types of data transfer

M/IO	RD	DEN	Transfer Type
0	0	1	I/O read
0	1	0	I/O write
1	0	1	memory read
1	1	0	memory write.

Bus Request and Bus Grant Timings in Minimum mode System.



Maximum Mode 8086 system