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A Brief Review on Multi Level Inverter Topologies

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***Abstract*—In this paper a brief review on different multilevel inverter topologies are discussed. Inverter is a power electronic device that converts DC power into AC power at desired output voltage and frequency. Multilevel Converters nowadays have become an interesting area in the field of industrial applications. Conventional power electronic converters are able to produce an output voltage that switches between two voltage levels only. Multilevel Inverter generates a desired output voltage from several DC voltage levels at its input. The input side voltage levels are usually obtained from renewable energy sources, capacitor voltage sources, fuel cells etc. The different multilevel inverter topologies are: Cascaded H-bridges converter, Diode clamped inverter, and Flying capacitor multilevel inverter. Multilevel inverters nowadays are used for medium voltage and high power applications. The different field of applications include its use as UPS, High voltage DC transmission, Variable Frequency Drives, in pumps, conveyors etc. The disadvantages of MLI are the need for isolated power supplies, design complexity and switching control circuits**

Keywords— Multi-Level Inverter topologies, MLI, PWM, sinusoidal pulse width modulation, phase opposition disposition, THD.

I. INTRODUCTION

Power electronic device which converts dc power into ac power at desired output voltage and frequency is known as inverter. The inverter producing an output voltage or current with two different levels of $\pm$ V is known as 2 level inverters. This two level conventional inverter operates at high switching frequency, with high switching losses and rating constraints for high power and voltage applications. It also faces harmonic distortion, EMI and high $\frac{dv}{dt}$ stress. High level of total harmonic distortion is another problem. Because of these problems, it is difficult to interface power electronic switches directly to high and medium voltage grid. Here comes the need for a different topology of multi level inverter. The multilevel inverter topology concept has been introduced in the early 1975 with three level converters. It is possible to increase the power rating with high number of voltage levels in the inverter. This reduces the device rating in the inverter. A multilevel inverter generates a smooth sinusoidal waveform from several d c voltage levels as its input.

Multi level inverters have become an interesting area in the industrial applications for high power and voltage ranges. It can be easily interfaced with renewable energy sources for various high power applications. The input side dc voltage sources are obtained from batteries, capacitor, renewable energy system, etc.

Thus the attractive features can be summarized as follows

1. Reduced harmonic distortion
2. Higher no. of voltage level
3. Staircase waveform quality
4. Operates at both fundamental and high switching frequency pwm
5. Lower switching losses
6. Better electromagnetic compatibility
7. Higher power quality
8.

One particular disadvantage is the need for large number of power semiconductor switches. Each switch have a related a gate driver circuit which adds complexity to the system. The overall system will be more expensive. Focuses are going on in present years to reduce the complexity of the circuit by decreasing the number of power electronic switches and gate driver circuits.

This paper presents the different multilevel power converter topologies with related structures and the pros and cons of each circuit.

II. THE CONCEPT OF MULTILEVEL INVERTERS

As in figure 1, Conventional two-level inverters normally generate an output AC voltage from an input DC voltage. Pulse Width Modulation switching scheme is used to generate the AC output voltage (as shown in figure2).

In the concept of Multilevel Inverter topology (MLI), several DC voltage levels are added together to create a smoother output waveform (as shown in figure3).The obtained output waveform have lower dv/dt and harmonic distortions. The circuit design is more complex with the increase in voltage levels. It needs a complicated switching controller circuit also.

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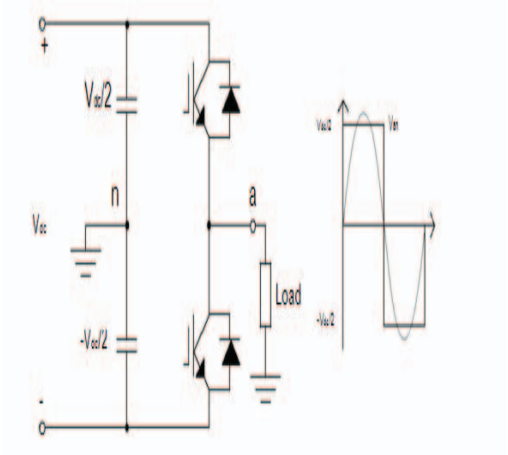

Figure1. One phase leg of a two-level inverter, two-level output waveform without PWM

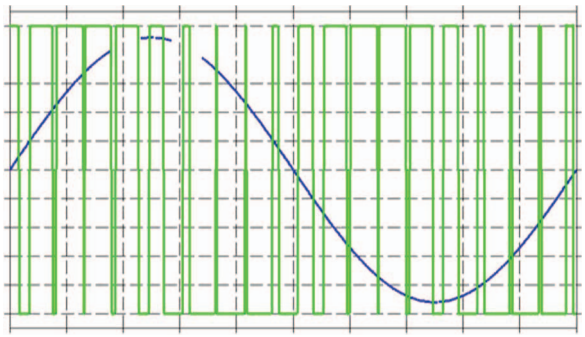

Figure 2. PWM voltage output.

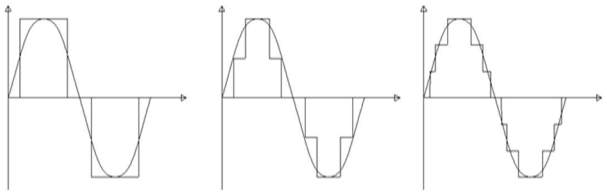

Figure 3. A three-level,five-level and seven-level output waveform at fundamental switching frequency

Figure4 shows the circuit of a conventional three-level inverter. In a three level inverter each phase leg generate the three voltage levels (Vdc/2, 0, –Vdc/2). Three-level inverter is similar to a conventional two-level inverter, but with clamping diodes in between the two valves and are connected to the neutral between two capacitors. The capacitors act as DC bus voltage sources, each one is charged with the voltage $V_{dc/2}$.

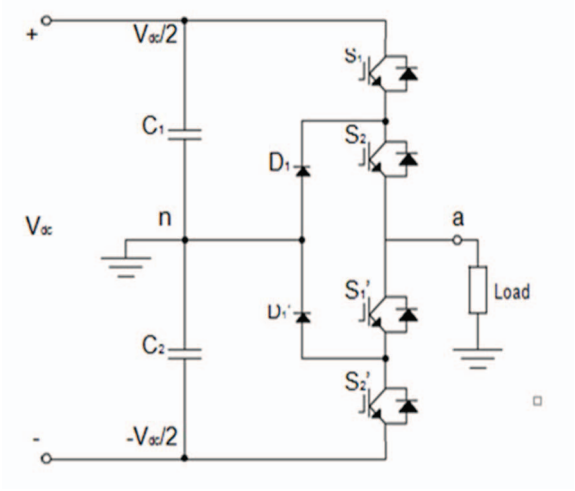

Figure4. Single leg of a three-level inverter

The number of levels can be increased by connecting another phase leg. Zero voltage level can be created by switching closer to the midpoint. Clamping diodes hold the voltage to zero with the neutral point. When valve pairs are more, capacitors and clamping diodes are added to generate more voltage levels in the inverter output. This results into a new topology of multilevel inverter with clamping diodes.

III. COMPARISON OF 2-LEVEL AND MULTILEVEL INVERTERS

In a 2-level inverter the output voltage waveform is obtained by Pulse Width Modulation scheme with two levels of voltage. This results in lower THD because of the distorted output waveform. Due to the sinusoidal nature of the output in a three level inverter, THD obtained is far better than a 2 level inverter. The sample output waveforms of a 2-level and 3-level inverter are shown in figure5.

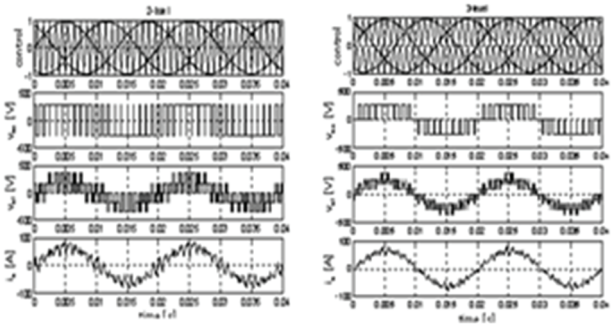

Figure.5.Output t waveforms for 2-level (left) ; 3-level (right) inverter.

Table 1: The difference between a 2-level and a 3- level inverter

Sl. No	Conventional Inverter	Multilevel Inverter
1	THD is high in the output waveform	THD is Low in the output waveform
2	High Switching stresses	Low Switching stresses
3	Not used for high Voltage applications	Used for high voltage Applications
4	High voltage levels cannot be produced	High voltage levels can be produced
5	High dv/dt and EMI	Low dv/dt and EMI
6	High switching frequency, increased switching losses	Lower switching frequency, reduced switching losses

IV. DIFFERENT MULTI LEVEL INVERTER TOPOLOGIES

There are mainly three different multilevel converter structures is being focused for industrial applications: cascaded H-bridge converter with separate dc sources, diode clamped inverter, and flying capacitor Multilevel inverter.

Figure.6. shows the classification of multilevel inverter topologies according to their uses in power conversions.

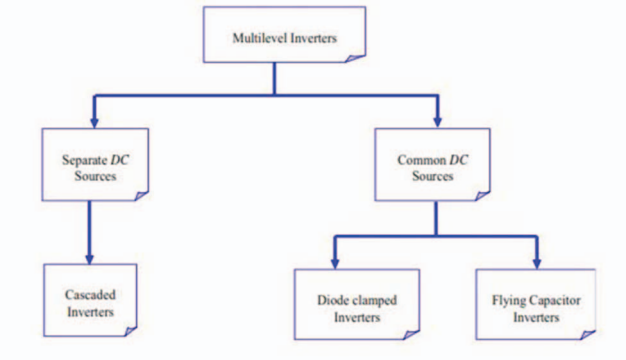

Figure6. Multilevel inverter schemes

4.1 Diode-Clamped Multilevel Inverter Topology:

Neutral-point-clamped(NPC) PWM topologies the first practical multilevel topology. Diode clamped multilevel inverters use clamping diodes. It helps to limit the voltage stress of power electronic devices. It was first proposed by Nabae, Takashi and Akagiin 1981. It is also known as neutral point converter.

An m level diode clamped inverter needs

Switching devices :(2m – 2),

Input voltage source :(m – 1)

No of diodes: (m – 1) (m – 2). Voltage present across each diode and the switch is Vdc . A five level diode clamped inverter is shown in figure7.

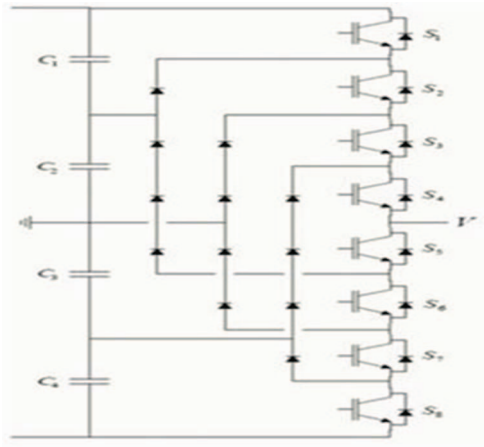

Figure7. A Five level diode clamped MLI

Advantages:

- Voltage across the switch is only half of the dc-link voltage
- Voltage harmonics is centred on twice the switching frequency
- Capacitance of the capacitor is low and they are precharged
- Back to back inverters are used
- Efficiency is high at fundamental frequency

Disadvantages:

- With the increase of each level, Clamping diodes are increased
- If the control and monitoring are not precise, Dc level will discharge

This topology however faces technical difficulties for high power converters. It requires high speed clamping diodes that will subject to reverse recovery stress. The design complexity is a major concern due to the series connection of diodes.

4.2 Flying Capacitor Multilevel Inverter Topology:

It is an alternative to the diode-clamped MLI topology. Here capacitors are used to limit the voltage. The presence of capacitors makes it different from that of diode clamped MLI where diodes are used. Capacitors divide the input DC voltages. The voltage across each capacitor and switch is *Vdc*.

An *m* level flying capacitor inverter needs

Switches: $(2m - 2)$

Number of capacitors: $(m - 1)$

The capacitor clamped switching cells are connected in series. The switching states are same as that of diode clamped inverter. No Clamping diodes are required in this

inverter. The output voltage is just half of the input DC voltage. A five level topology is shown below in figure8.

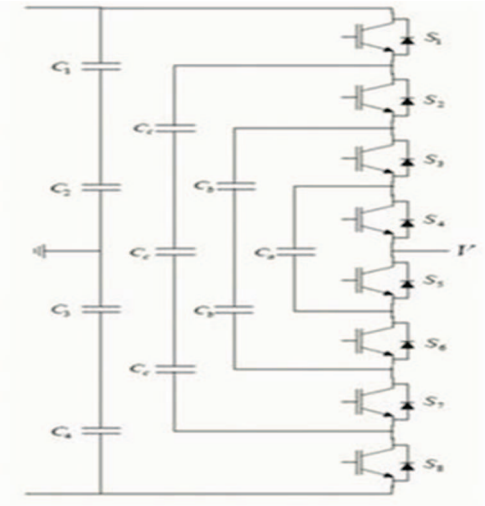

Figure8. Five level flying capacitor MLI

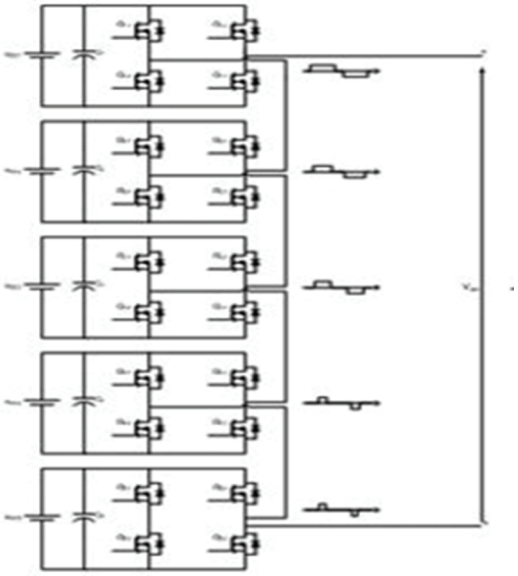

Figure9. A 5 level H-bridge inverter

Advantages:

- Eliminates the clamping diode problems
- Reduces dV/dt stress across the device
- Additional switching states help to maintain charge balance in the capacitors

Disadvantages:

- Complex start-up
- Lower Switching efficiency
- Capacitors are expensive than diodes
- Voltage control across all the capacitors is difficult

4.3 Cascaded voltage H bridge Multilevel Inverter topology:

The cascaded H-bridge inverter uses separate Dc sources or capacitors (as shown in figure 8.).It requires only less number of components in each level. There is a series connection of power conversion cells. The H-bridge consists of capacitors and switches pair combination. For each H Bridge, separate input DC voltage is obtained. It generates a sinusoidal output voltage. The inverter uses series connected H-bridge cells, each providing three different levels of Dc voltages (zero, positive DC and negative DC voltages).The output voltage is the sum of all the generated voltages from each H Bridge cell. If m cells are present, the numbers of output voltage levels will be2m+1.A five level H bridge Inverter is shown in figure 9.

Advantages:

- Easy packaging and storage
- Produce common mode voltage, stress is reduced
- Low distortions in the input current
- Operates at both fundamental switching frequencies
- Total harmonic distortion is very low in the output waveform without any filter circuit

Disadvantages:

- Separate DC sources or capacitor are required for each module
- A More complex controller is required due to the amount of capacitors

4.4 Comparison of Different Multilevel Inverters

The comparison of different multilevel inverters is based on the following criteria:

- Number of semiconductor devices in each phase leg
- Number of Dc bus capacitors present
- Amplitude of harmonic components
- Number of balancing capacitors in each phase leg
- Total Harmonic Distortion in the output voltage
- Control complexity based on power switches and voltage unbalances
- Cost estimation associated with power circuit

Table 2: The basic comparison based on the number of components used.

S.No.	Topology	Diode Clamped	Flying Capacitor	Cascaded
1	Power semi conductor switches	2(m-1)	2(m-1)	2(m-1)
2	Clamping diodes per phase	(m-1)(m-2)	0	0
3	DC bus capacitors	(m-1)	(m-1)	(m-1)/2
4	Balancing capacitors per phase	0	(m-1)(m-2)/2	0
5	Voltage unbalancing	Average	High	very small
6	Applications	Motor drive system, STATCOM	Motor drive system, STATCOM	Motor drive system, PV, fuel cells, battery system

V. MODULATION TECHNIQUES OF MULTI LEVEL INVERTER

The different modulation schemes are shown in figure10.

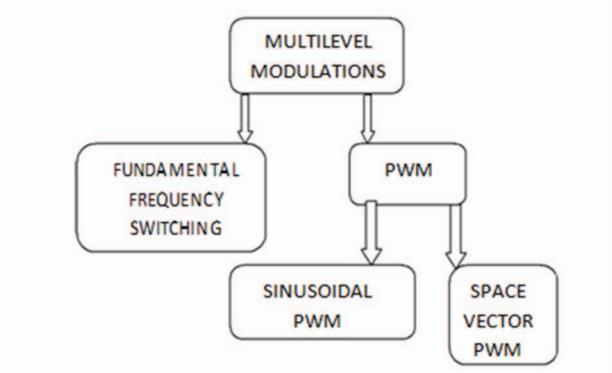

Figure10. Modulation topologies

The multilevel topology has several modulation techniques, each with different methods of modulation. The commonly used modulation topologies for multi level inverters are as follows:

- Sinusoidal or "Sub harmonic" Natural Pulse Width Modulation (SPWM)
- Selective Harmonic Eliminated Pulse Width Modulation (SHE PWM)
- Alternative Phase Opposition Disposition (APOD), where each carrier is having a phase shift of 180° from the adjacent carriers.
- Phase Opposition Disposition (POD) where the carriers above the reference zero point is out of phase with those below the zero point.
- Phase Disposition (PD) where all carriers are in phase.

VI. CONCLUSION

The paper presents a brief discussion on basic multi-level inverter topologies. Fundamental multilevel converter structures including the advantages and disadvantages of each technique have been discussed. The main advantage of MLI family is that it finds a solution to the problems of total harmonics distortion, EMI, and dv/dt stress on switch. In industrial and commercial market areas, more and more product are available that depends on the multi-level inverter topologies. Research works are in progress considering the structure complexity and control circuits. This helps to reduce the power electronics components and improve total harmonics profile and total cost of the system.

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