EE101: Circuit elements and laws

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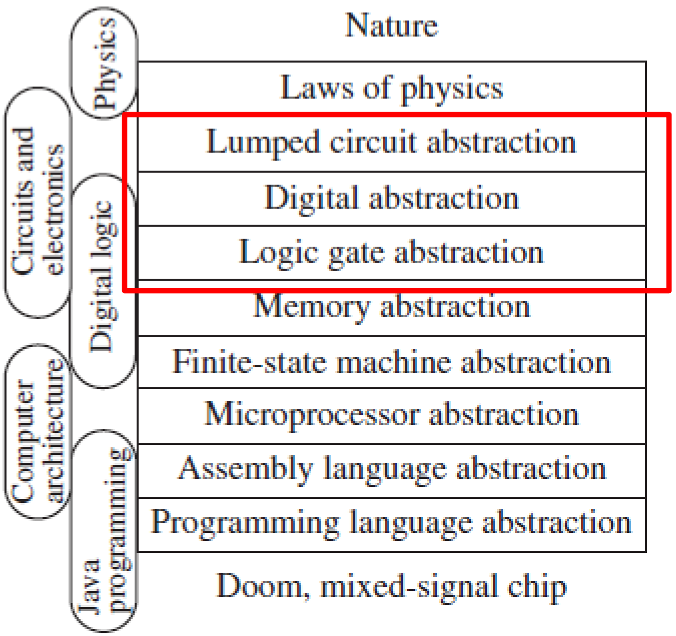
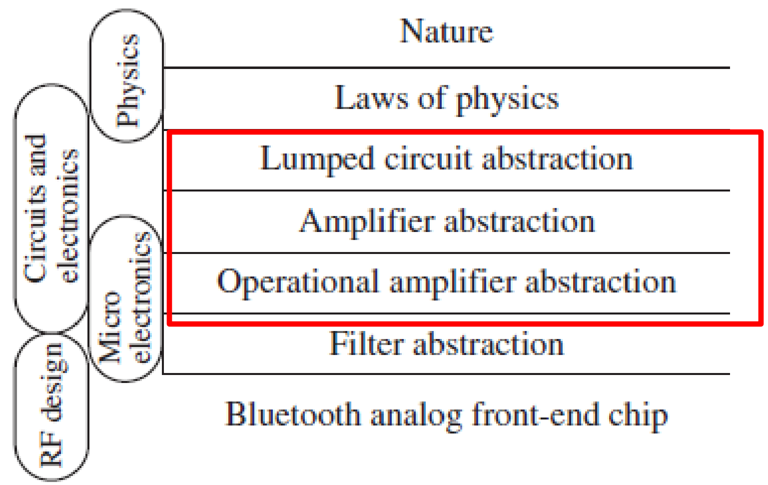
References: 1) L. Bobrow, 2) Agarwal and Lang

Layers of Abstraction





Example 1

Example 2

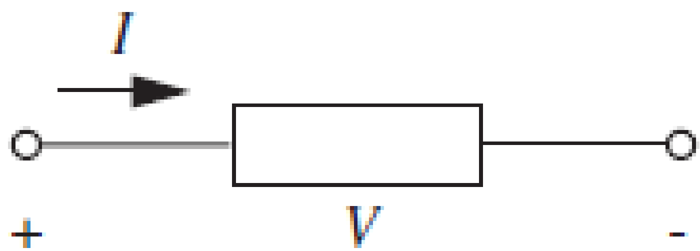
- Multiple layers of abstraction to build modern complex systems

Maxwell's laws

DIFFERENTIAL FORM	INTEGRAL FORM	POPULAR NAME
$\nabla \cdot \mathrm{E} = \frac{\rho}{\epsilon_0}$	$\oint \mathrm{E} \cdot d\mathrm{S} = \frac{q}{\epsilon_0}$	Gauss's law for electricity
$\nabla \cdot \mathrm{B} = 0$	$\oint \mathrm{B} \cdot d\mathrm{S} = 0$	Gauss's law for magnetism
$\boxed{\nabla \times \mathrm{E} = -\frac{\partial \mathrm{B}}{\partial t}}$	$\boxed{\oint \mathrm{E} \cdot d\mathrm{l} = -\frac{\partial \Phi_B}{\partial t}}$	Faraday's law of induction
$\nabla \times \mathrm{B} = \mu_0\epsilon_0 \frac{\partial \mathrm{E}}{\partial t} + \mu_0 \mathrm{J}$	$\oint \mathrm{B} \cdot d\mathrm{l} = \mu_0\epsilon_0 \frac{\partial \Phi_E}{\partial t} + \mu_0 i$	Ampere's law (extended)
$\boxed{\nabla \cdot \mathrm{J} = -\frac{\partial \rho}{\partial t}}$	$\boxed{\oint \mathrm{J} \cdot d\mathrm{S} = -\frac{\partial q}{\partial t}}$	Continuity equation

- Laws of physics describing natural phenomena
- Faraday's law and Continuity equation are critical to circuit analysis

Lumped circuit element

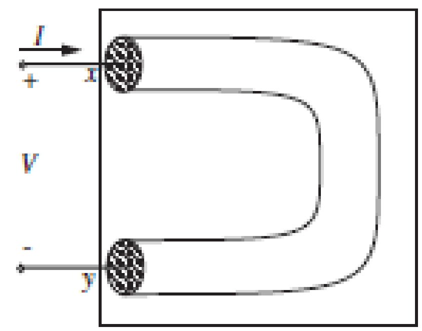


- ***Unique value*** of voltage from one terminal to another
- ***Unique value*** of current entering one terminal and exiting the other
- Elements in a circuit interact only through their terminal voltages and currents
  - No electric or magnetic field outside the elements that can cause interaction
  - Counter example?

Lumped element

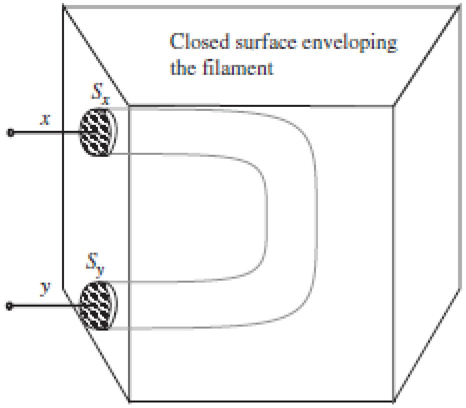
1. Rate of change of magnetic flux through any closed loop outside an element = 0 for all time

$$\oint \mathrm{E} \cdot \mathrm{dl} = -\frac{\partial \Phi_B}{\partial t} \qquad \boxed{\frac{\partial \Phi_B}{\partial t} = 0}$$



2. No time varying charge within the element for all time

$$\oint \mathrm{J} \cdot \mathrm{dS} = -\frac{\partial q}{\partial t}. \qquad \boxed{\frac{\partial q}{\partial t} = 0}$$



3. Operate where signal timescales >> propagation delay of EM waves → instantaneous propagation of the signals (electromagnetic waves → wavelength of the V and I signals is >> size of the element

Reading: Appendix A.1 of A. Agarwal's book

Lumped circuit

- Rate of change of magnetic flux linked with any portion of the circuit must be zero for all time

  Kirchoff's voltage law

- Rate of change of the charge at any node (connection of two or more element terminals) must be zero

  Kirchoff's current law

- Signal timescales must be much larger than the propagation delay of electromagnetic waves through the circuit

  Critical assumption → see next slide

Signal propagation

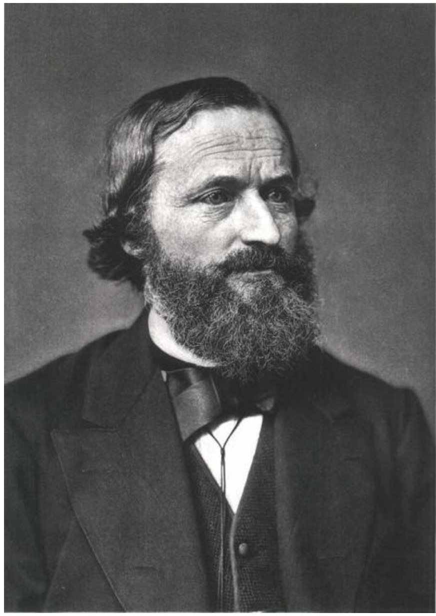
- Circuit must be smaller than the wavelength of the light at highest operating frequency of interest
  - e.g. 1 kHz, 1 MHz and 1 GHz circuits have to be smaller than 300 km, 300 m and 300 mm respectively
  - Else model wave phenomena accurately
  - Will a 5000-km power grid at 60 Hz or a 30 cm computer motherboard at 1 GHz satisfy this condition?

Signal propagation

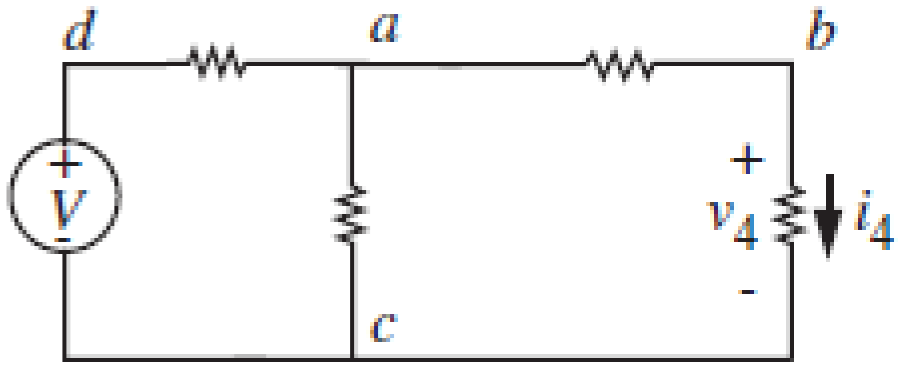
- Latest microprocessor (June 2015)
  - Intel Broadwell 14nm (i7, 37.5x37.5 mm, 3.3 GHz)
- Propagation speed of electromagnetic signals
  - In vacuum → 30 cm per ns
  - Approx ½ of that in microproc. (ϵ=4) → 15 cm per ns
  - ~1/4 ns to propagate through 37.5mm (~4 cm)
  - 3.3 GHz → 1/3.3 ns for a clock cycle
  - Propagation delay is the same as one clock cycle!
  - Need distributed circuit models using waveguides, transmission lines etc.

Gustav Kirchoff (1824- 1887)

- Kirchoff’s laws- 1845 (graduate student)
- Other contributions
  - Three laws in spectroscopy
  - Discovery of caesium and rubidium with Bunsen
  - Emission of black body radiation



Kirchoff's laws



$$\oint \mathbf{E} \cdot d\mathbf{l} = -\frac{\partial \Phi_B}{\partial t}$$

$$\oint \mathbf{E} \cdot d\mathbf{l} = 0$$

For closed circuit loops

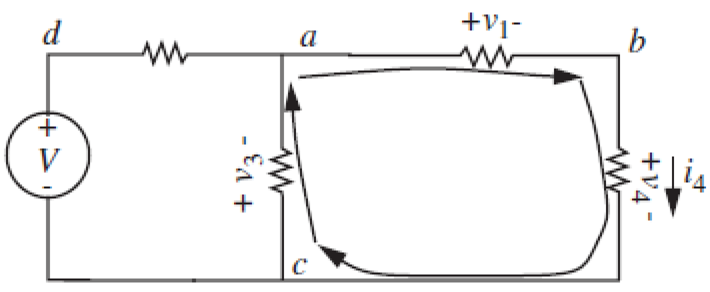
$$\oint \mathbf{J} \cdot d\mathbf{S} = -\frac{\partial q}{\partial t}.$$

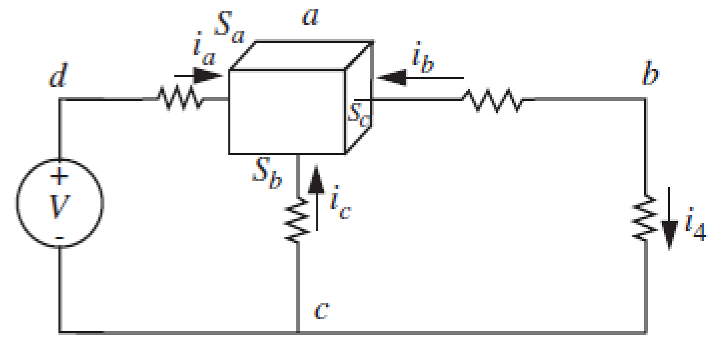
$$\oint \mathbf{J} \cdot d\mathbf{S} = 0.$$

For circuit nodes

Reading: Appendix A.2 of A. Agarwal's book

Kirchoff’s laws





$$\int_a^b \mathbf{E} \cdot d\mathbf{l} + \int_b^c \mathbf{E} \cdot d\mathbf{l} + \int_c^a \mathbf{E} \cdot d\mathbf{l} = v_1 + v_2 + v_3 = 0.$$

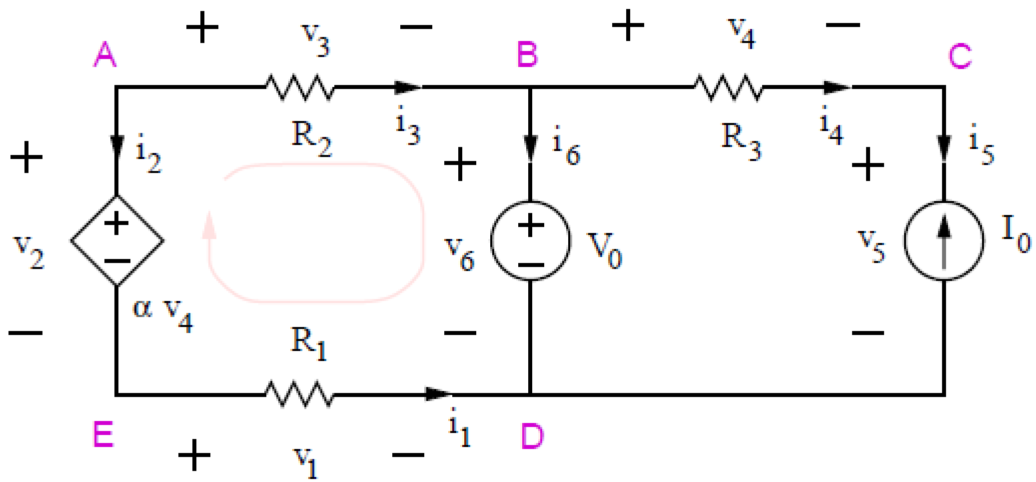
$$\int_{S_a} \mathbf{J} \cdot d\mathbf{S} + \int_{S_b} \mathbf{J} \cdot d\mathbf{S} + \int_{S_c} \mathbf{J} \cdot d\mathbf{S} = -i_a - i_b - i_c = 0.$$

- Algebraic sum of voltages around any closed path in a network is zero.
- Algebraic sum of currents flowing into any node is zero.

Kirchoff's Current Law (KCL)

- A connection of two or more elements is called a node (solid dot)
- KCL:
  - At any node of a circuit, at every instant of time, the sum of currents into the node is equal to the sum of currents out of the node
  - At any node of a circuit, the currents algebraically sum to zero

Example



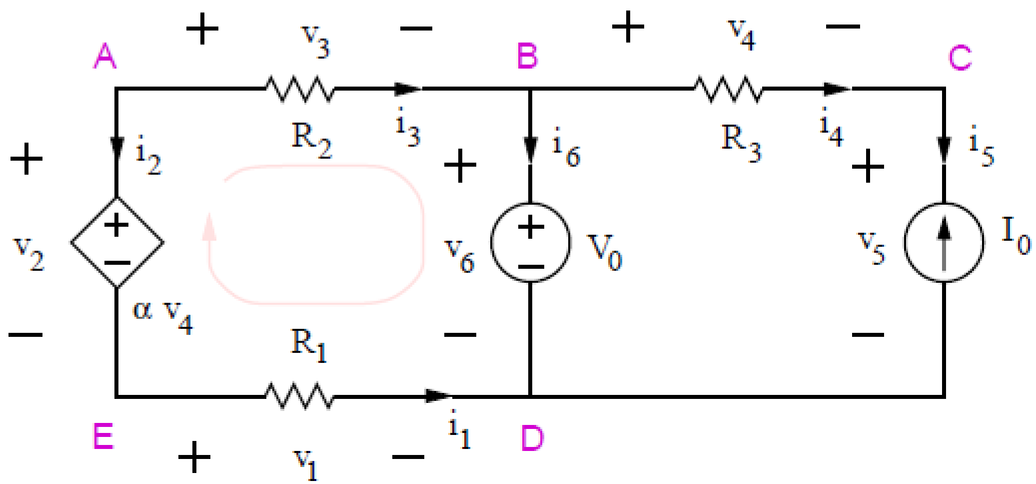
- At node B: $-i_3+i_6+i_4=0$
- Convention: Current leaving a node is positive
- In general KCL is also applicable for any closed region of the circuit (conservation of charge)

Kirchoff’s Voltage Law (KVL)

- Loop: Starting at any node n in a circuit, we form a loop by traversing through elements (open circuits included) and returning to the starting node n, and never encountering any other node more than once.

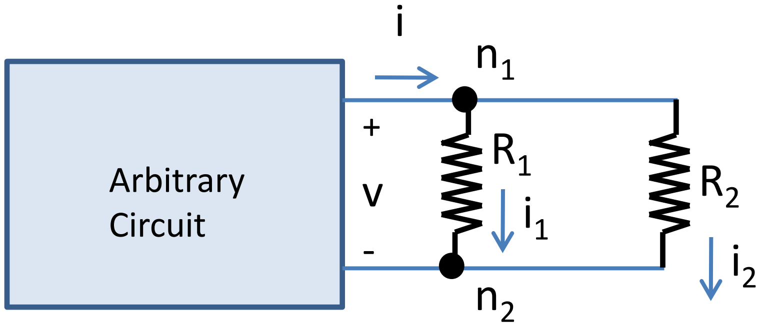
- KVL:
  - In traversing any loop in any circuit, at every instant of time, the sum of the voltages having one polarity equals the sum of the voltages having the opposite polarity.
  - Around any loop in a circuit, the voltages algebraically sum to zero.

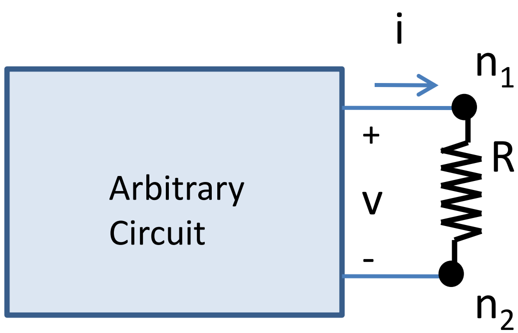
Example



- For the loop: $v_3+v_6-v_4-v_2=0$
- Convention: Voltage drop is positive

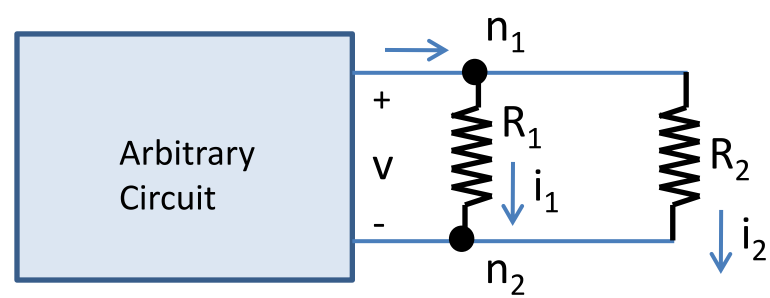
KCL examples





$i=i_1+i_2$
$=v/R_1+v/R_2$
$=v(1/R_1+1/R_2)$
$=v/R$
$\Rightarrow \boxed{1/R=1/R_1+1/R_2}$

Resistances in parallel



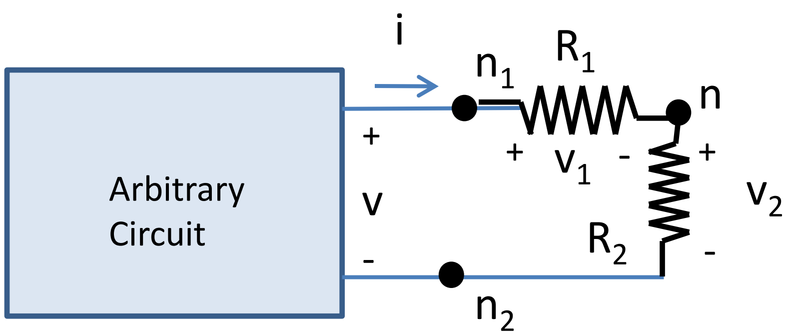
$v=i[R_1R_2/(R_1+R_2)]$
$i_1=v/R_1$ and $i_2=v/R_2$

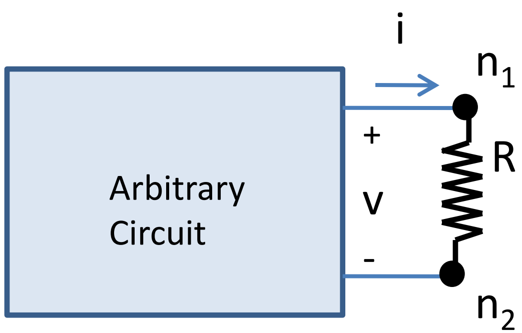
Therefore,
$i_1=i\ (R_2/R_1+R_2)$
$i_2=i\ (R_1/R_1+R_2)$

Current Division

- Assume $R_1 >> R_2 \rightarrow i_2 >> i_1$
- Current takes the path of least resistance!

KVL Examples

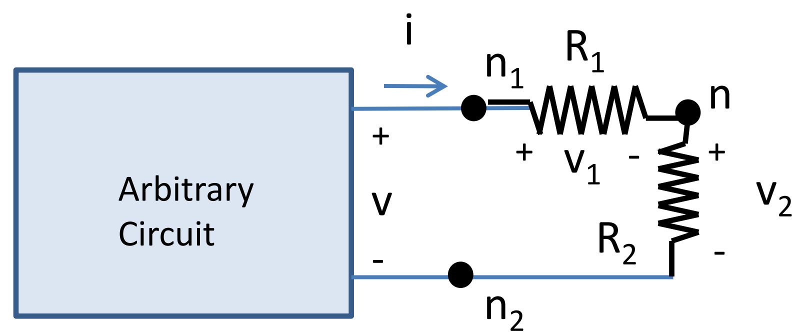




$v=v_1+v_2$
$=iR_1+iR_2$
$=i(R_1+R_2)$

$\boxed{\rightarrow R=R_1+R_2}$

Resistances in series



$i=v/(R_1+R_2)$

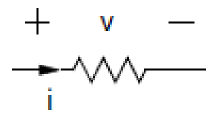
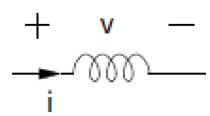
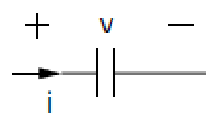
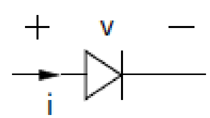
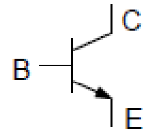
$v_1=iR_1=v(R_1/R_1+R_2)$

$v_2=iR_2=v(R_2/R_1+R_2)$

Voltage Division

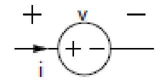
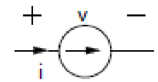
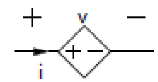
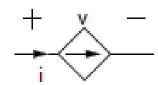
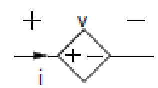
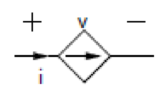
- Assume $R_1 >> R_2 \rightarrow v_1 >> v_2$
- Larger voltage drop across the larger resistor

Circuit Elements

Element	Symbol	Equation
Resistor		$v = R\,i$
Inductor		$v = L\,\dfrac{di}{dt}$
Capacitor		$i = C\,\dfrac{dv}{dt}$
Diode		to be discussed
BJT		to be discussed

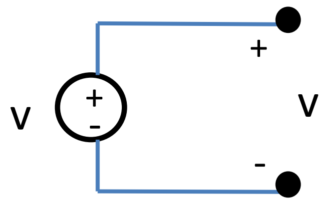
- Some typical elements

Ideal Current and Voltage Sources

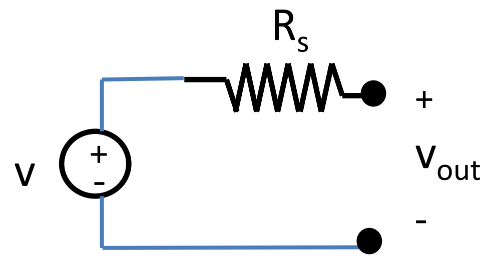
	Element	Symbol	Equation
Independent	Voltage source		$v(t) = v_s(t)$
	Current source		$i(t) = i_s(t)$
Dependent	VCVS		$v(t) = \alpha\, v_c(t)$
	VCCS		$i(t) = g\, v_c(t)$
	CCVS		$v(t) = r\, i_c(t)$
	CCCS		$i(t) = \beta\, i_c(t)$

- Note that these can be time dependent sources

Voltage Source



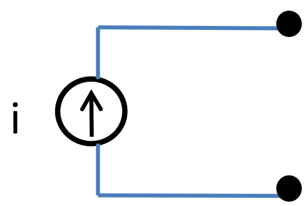
Ideal



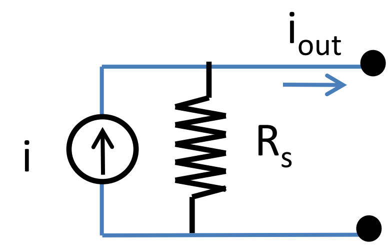
Non-ideal

- An ideal voltage source produces a voltage or potential difference of v volts across its terminals regardless of what is connected to it
  - Except for a short circuit (R=0)
  - Current flowing through it can take any value
- You cannot have two (or more) ideal voltage sources connected to the same pair of terminals

Current Source



Ideal



Non-ideal

- An ideal current source produces i amperes regardless of what is connected to it
  - Except for an open circuit (R=infinite)
  - It can take any voltage across its terminals

- You cannot have two (or more) ideal current sources in series