EE101: MOSFET and CMOS Digital Logic

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Digital Technologies

- Information en-coded in logic values = {0, 1}
- A logic value, 0 or 1, is called as BInary DigiT or BIT.
- Physical states representing bits in digital technologies:

Technology	State Representing Bit	
	0	1
Relay logic	Circuit open	Circuit closed
CMOS logic	0-1.5V	3.5-5V
Transistor-transistor logic	0-0.8V	2-5V
Fiber optics	Light off	Light on
Dynamic memory	Capacitor discharged	Capacitor charged
Nonvolatile, erasable memory	Electrons trapped	Electrons released
Bipolar read-only memory	Fuse blown	Fuse intact
Magnetic tape or disk	Flux direction N	Flux direction S
Read-only compact disc	No pit	Pit

CMOS Digital Logic

- CMOS: Complementary MOS
- Information can be encoded using:
  - Current, Voltage, Phase, Frequency
- CMOS Digital systems use two voltage levels for encoding bits.
  - LOW: A signal close to the GND
  - HIGH: A signal close to the VCC

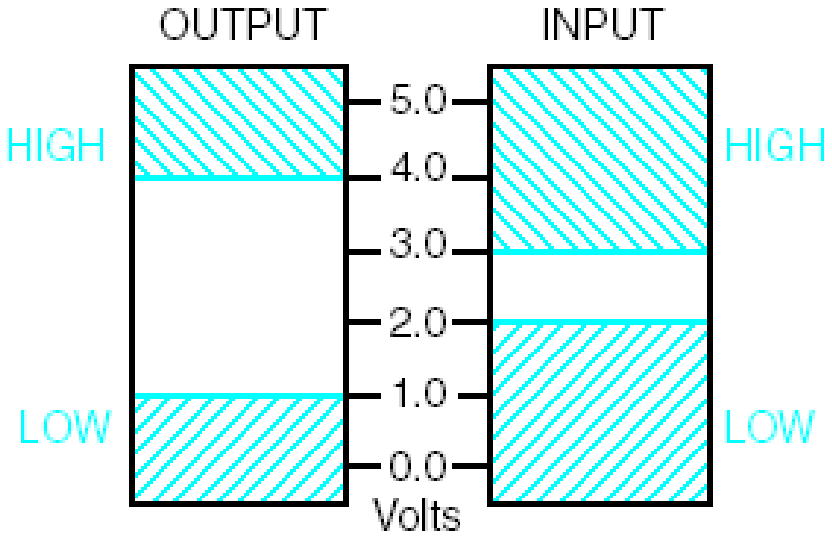
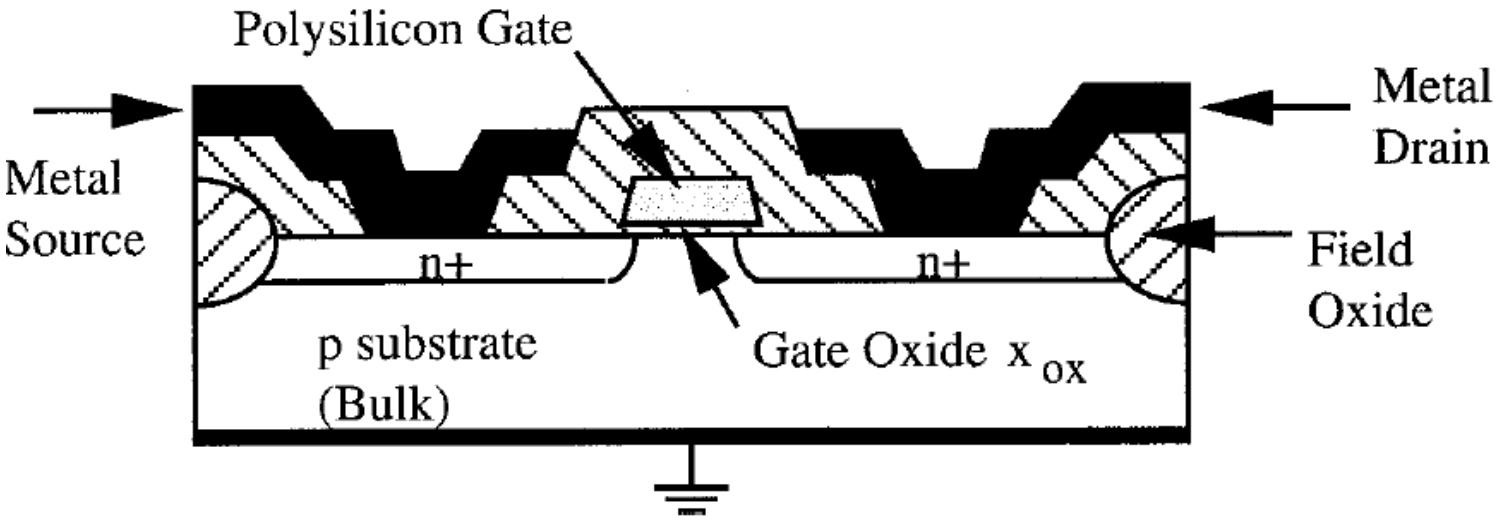


Fig. 1-1 An Example of Voltage Ranges for Binary Signals

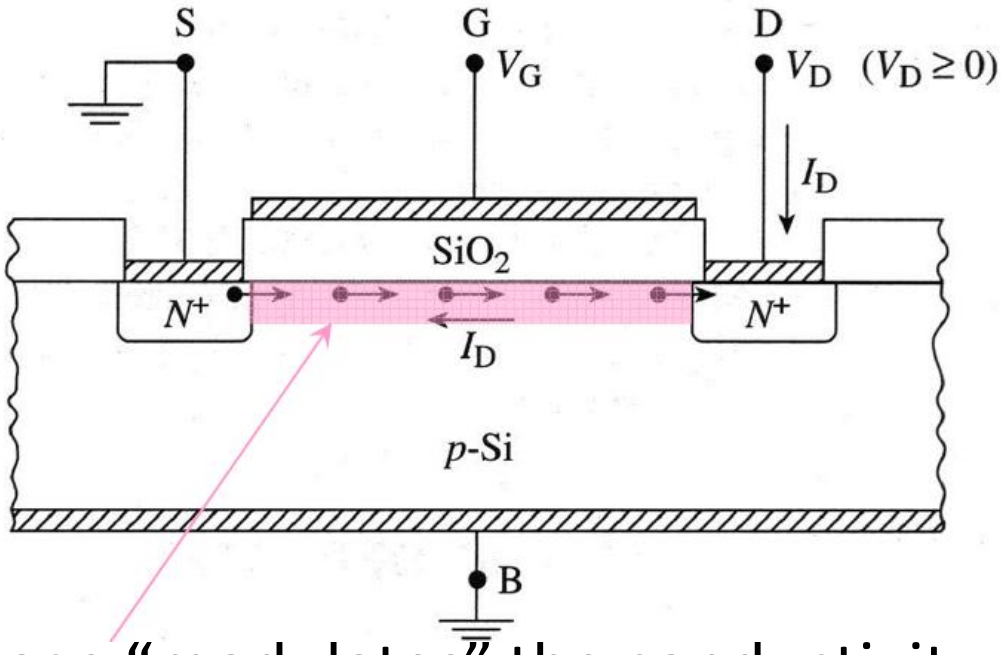
Basic building block for CMOS Digital Logic



- **MOS**FET: “Metal-oxide-semiconductor field effect transistor”

MOSFET operation

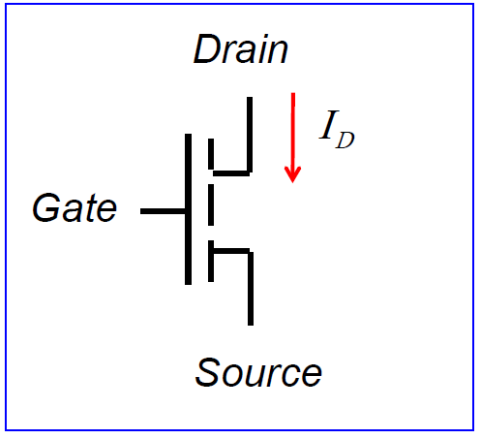
Flow of current from “source” to “drain” is controlled by the gate voltage through a “field effect”.



- Gate voltage “modulates” the conductivity of the region below the gate → “channel”

MOSFET as a 2-port device

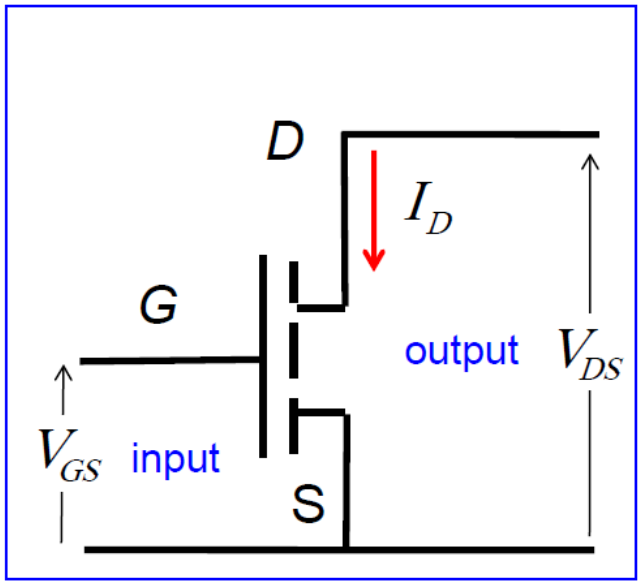
MOSFET circuit symbol



current vs. voltage (IV) characteristics

$I_D(V_G, V_S, V_D)$

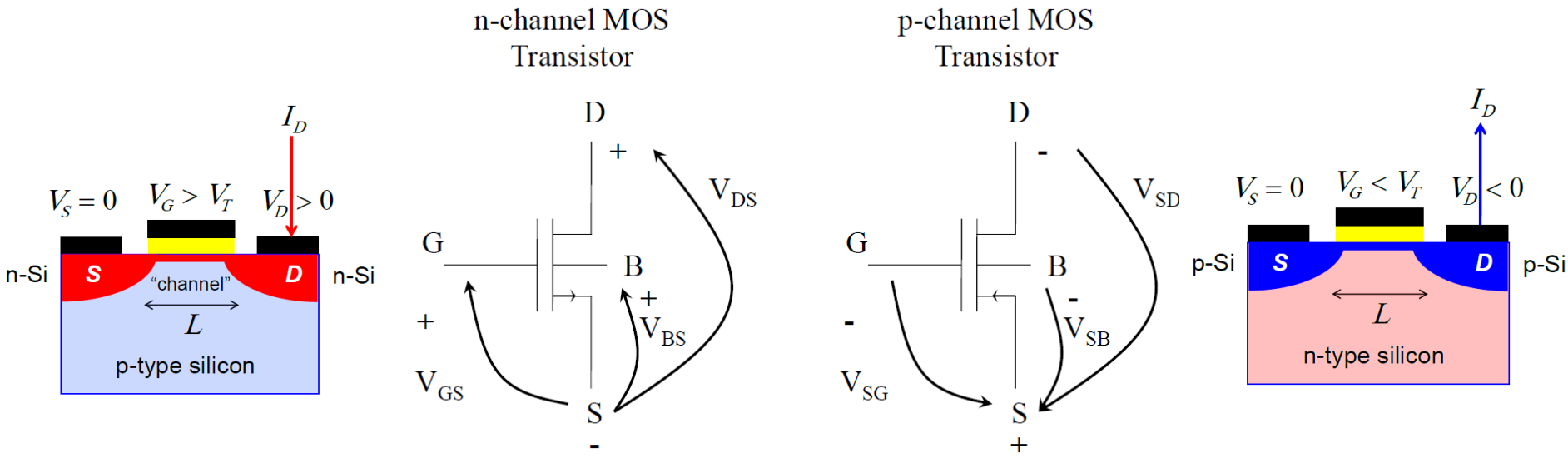
common source



$I_D(V_{GS})$ at a fixed V_{DS} transfer

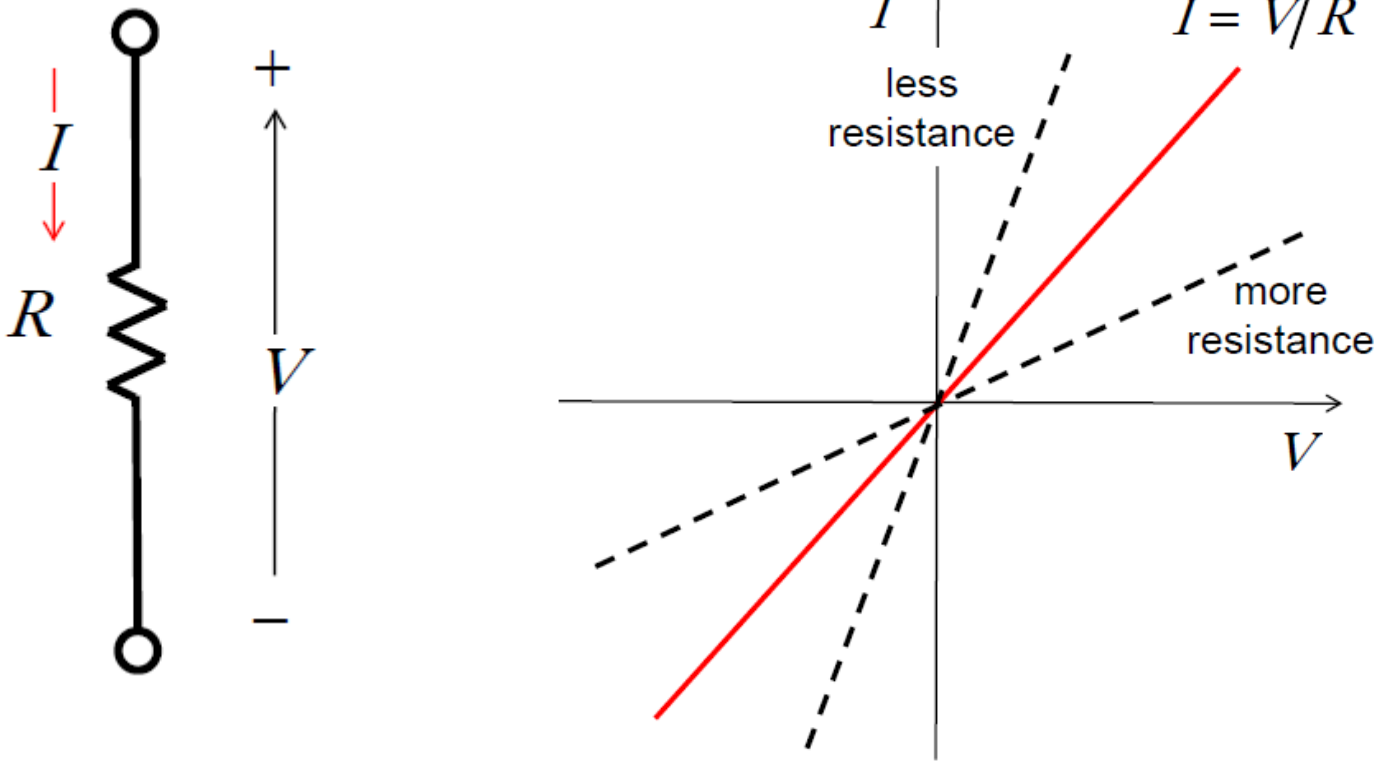
$I_D(V_{DS})$ at a fixed V_{GS} output

N and p-channel MOSFETs: Qualitative Description



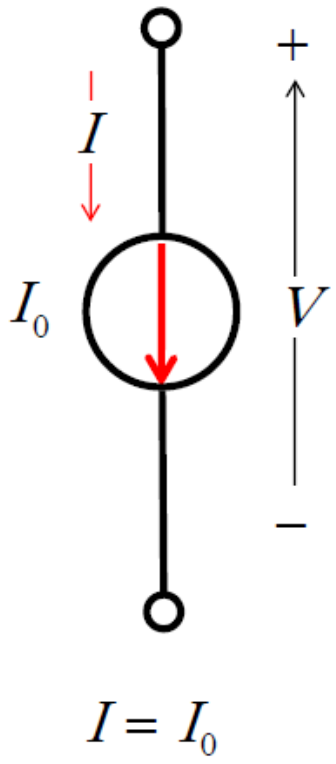
- G=Gate, D=Drain, S=Source, B=Body (substrate)

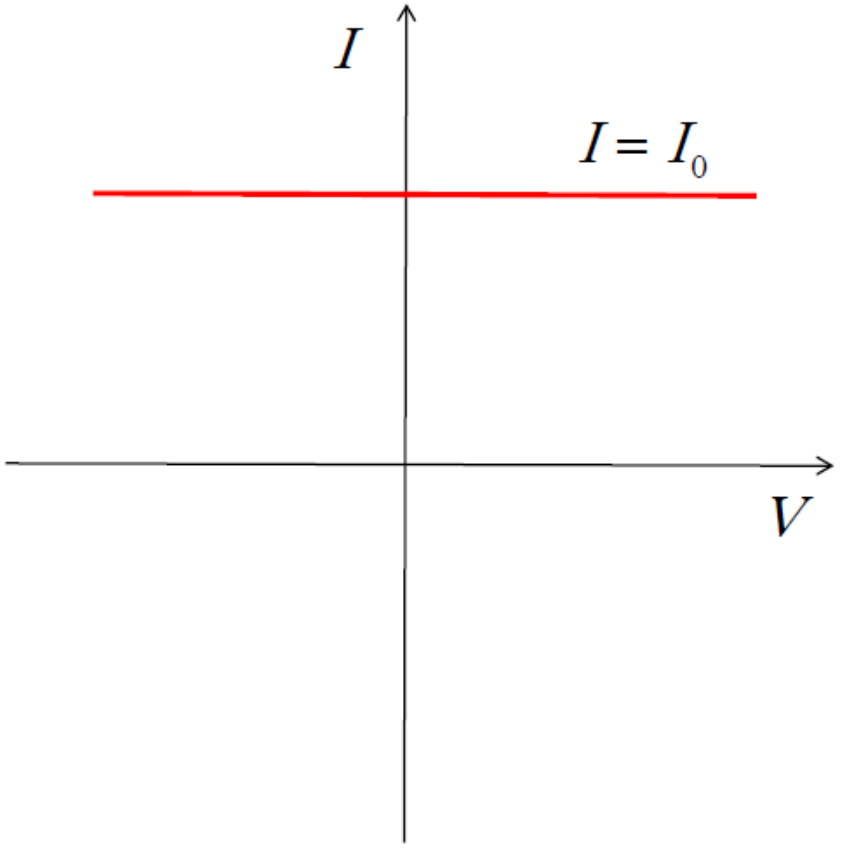
MOSFET IV Characteristics (1): Resistor



- “Linear” characteristics

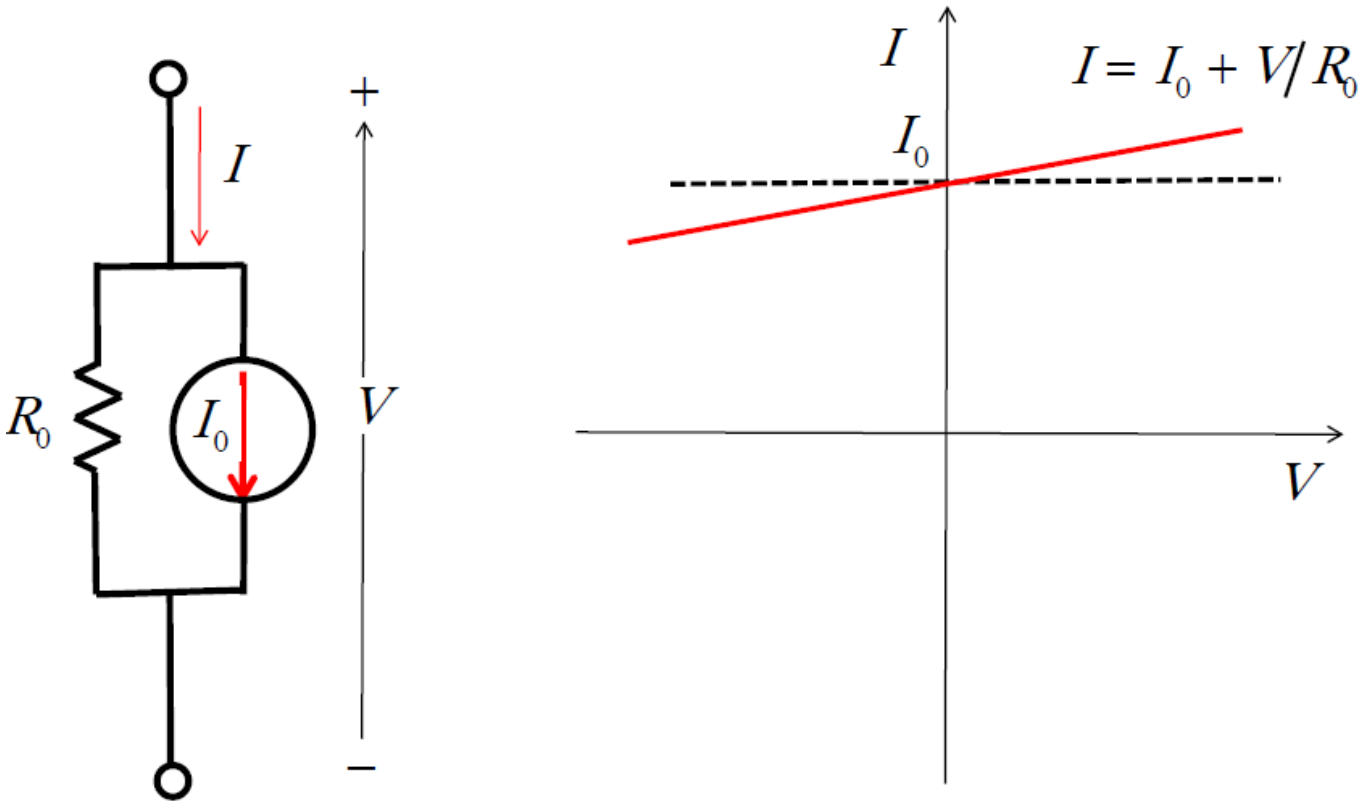
MOSFET IV Characteristics (2): Ideal Current Source





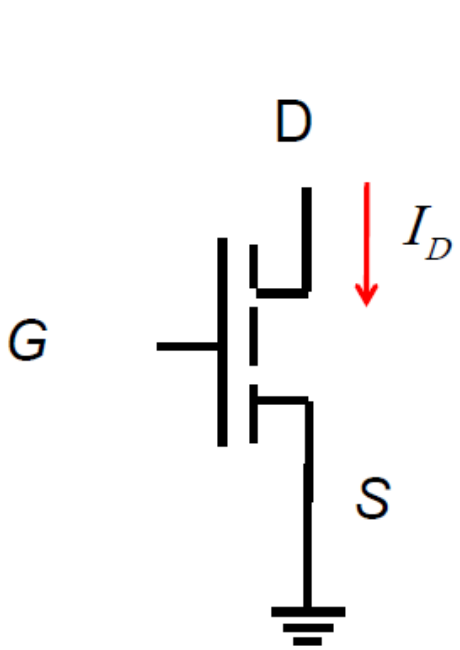
- Ideal current Source: “Saturation” Characteristics

MOSFET IV Characteristics (2): Real current source

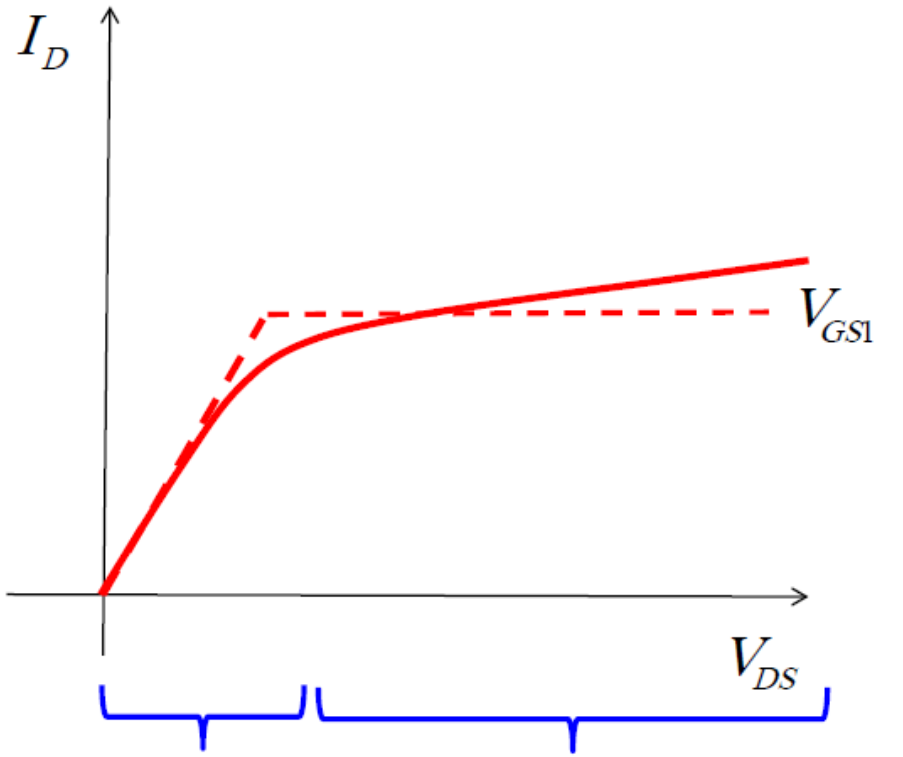


- Real Current Source: “Saturation” Characteristics

Combined Characteristics



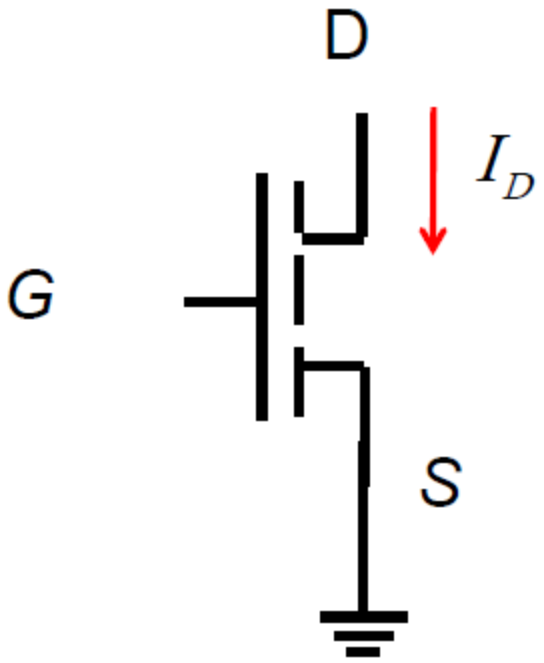
n-channel enhancement mode MOSFET



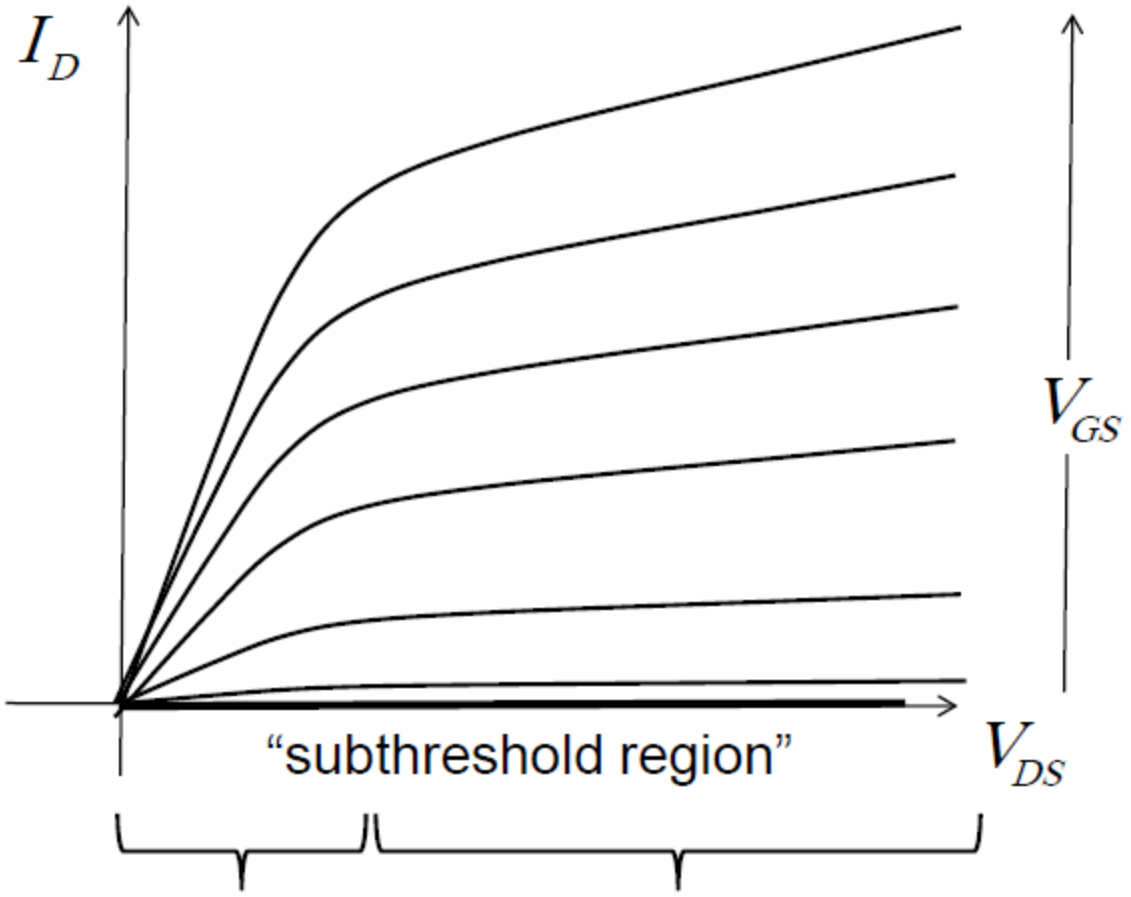
gate voltage controlled resistor "linear region"

gate voltage controlled current source "saturation region"

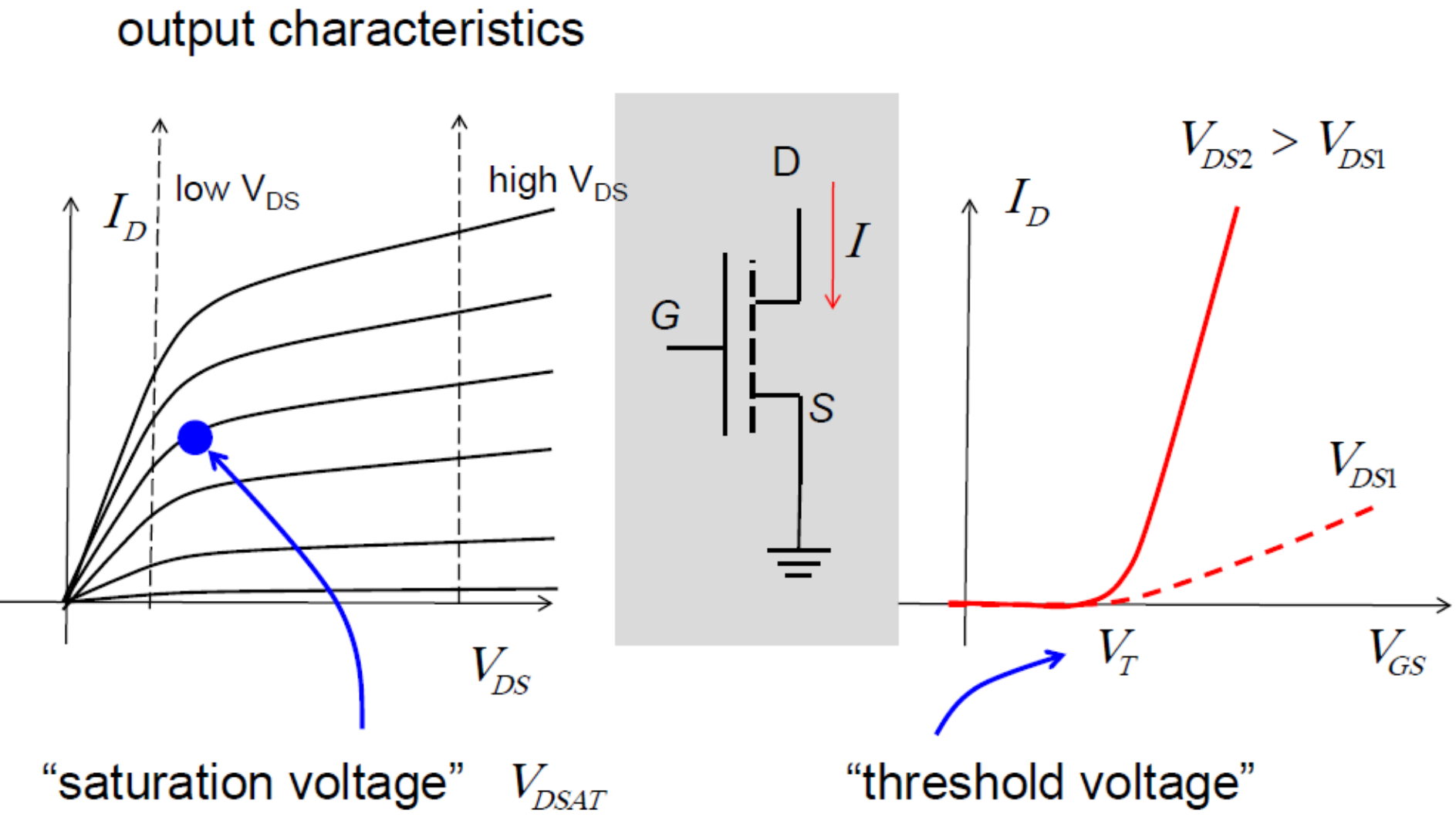
Combined Characteristics



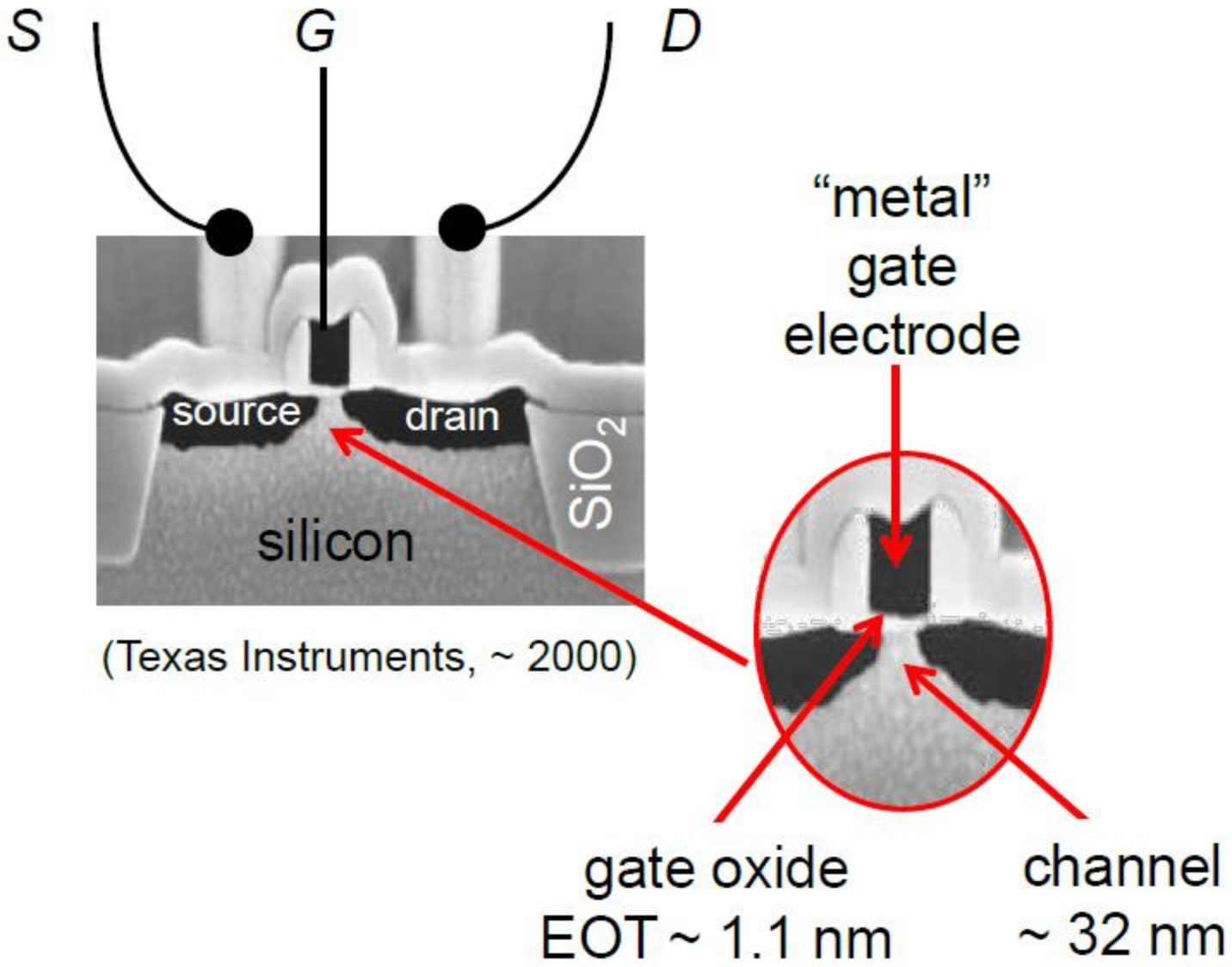
n-channel
enhancement
mode MOSFET



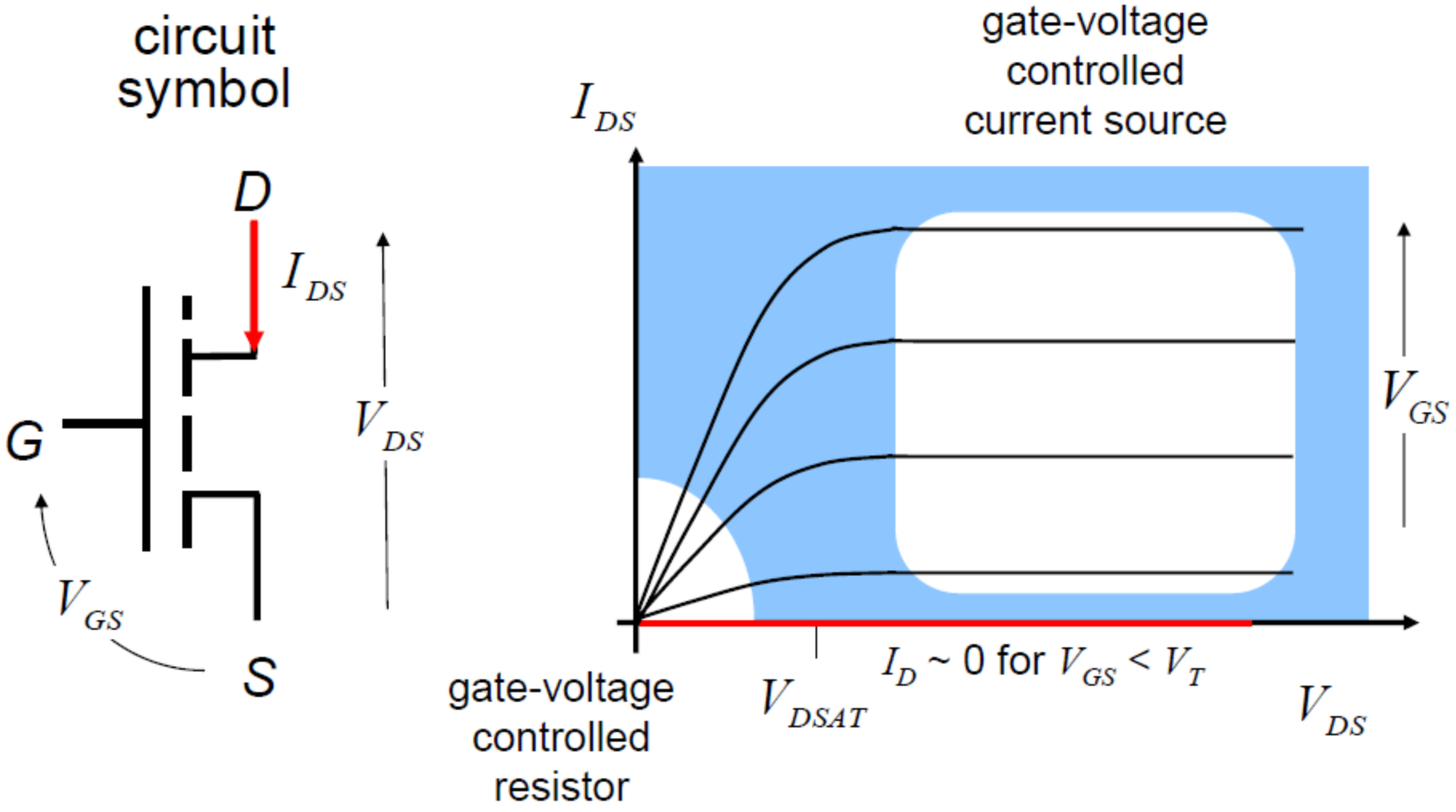
Output and Transfer Characteristics



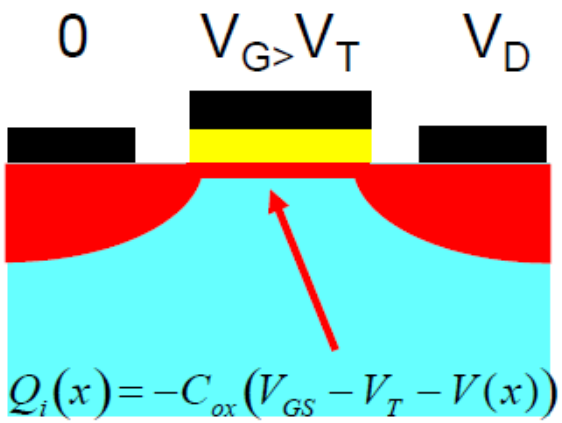
Physical MOSFET



I-V Characteristics: Details



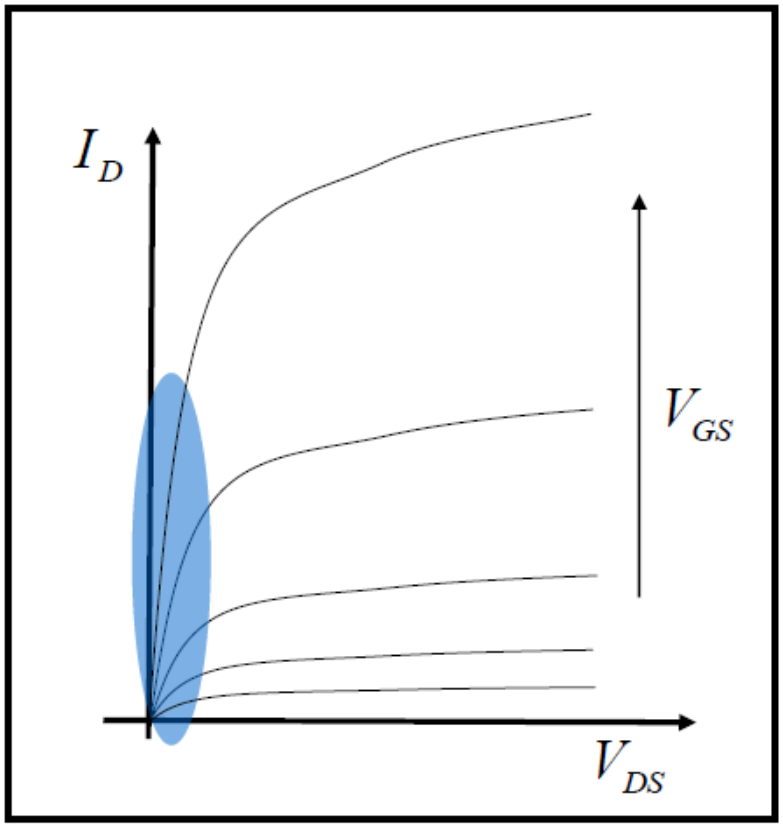
MOSFET I-V: Low V_{DS}



$$I_D = W\, Q_i(x)\, \upsilon_x(x)$$

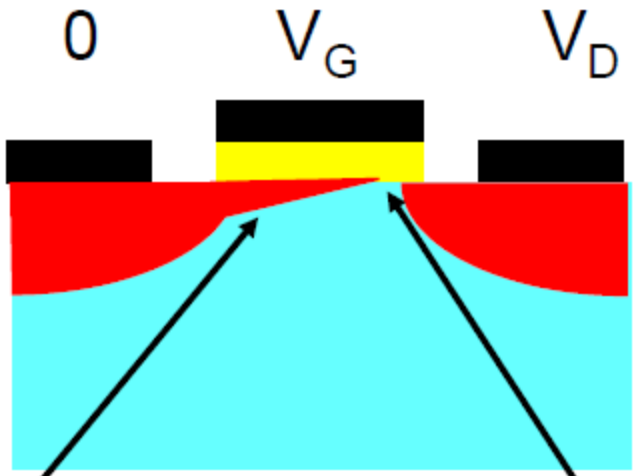
$$I_D = W\, C_{ox}(V_{GS} - V_T)\mu_{eff}\mathcal{E}_x$$

$$\mathcal{E}_x = \frac{V_{DS}}{L}$$



$$I_D = \frac{W}{L}\mu_{eff} C_{ox}(V_{GS} - V_T)V_{DS}$$

MOSFET I-V: Pinch-off at high V_{DS}

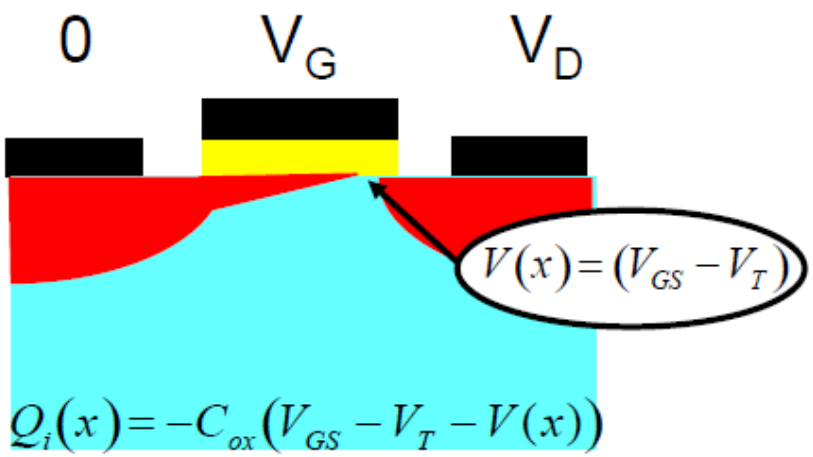


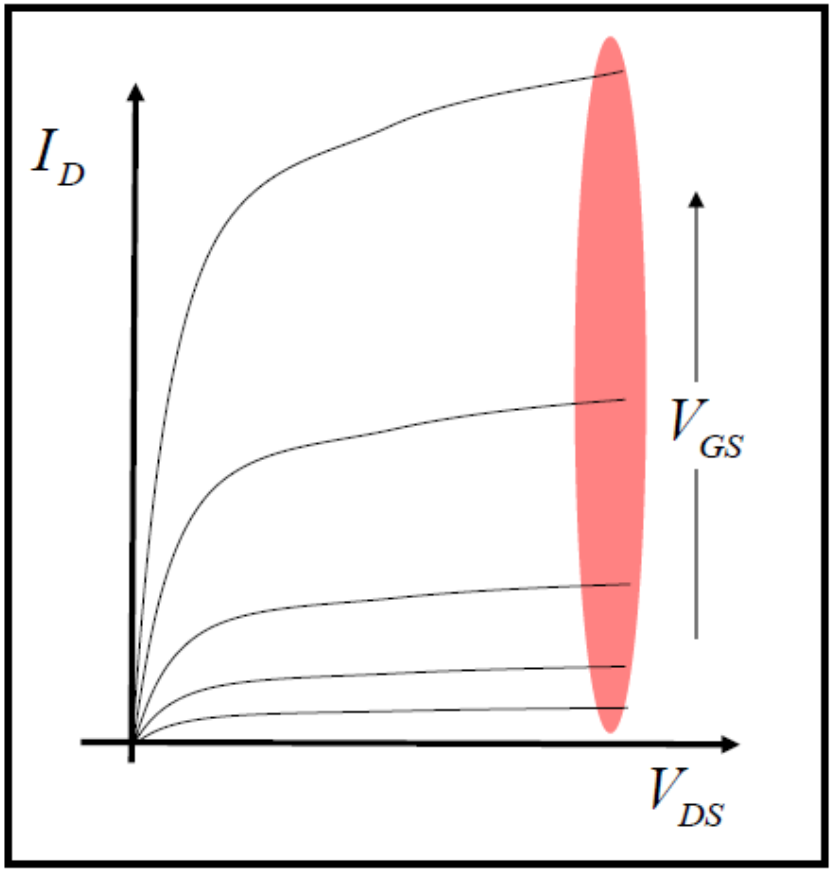
$$Q_i(x) = -C_{ox}\left(V_{GS} - V_T - V(x)\right)$$

$$V(x) = \left(V_{GS} - V_T\right)$$

$$Q_i(x) \approx 0$$

MOSFET I-V: High V_{DS}





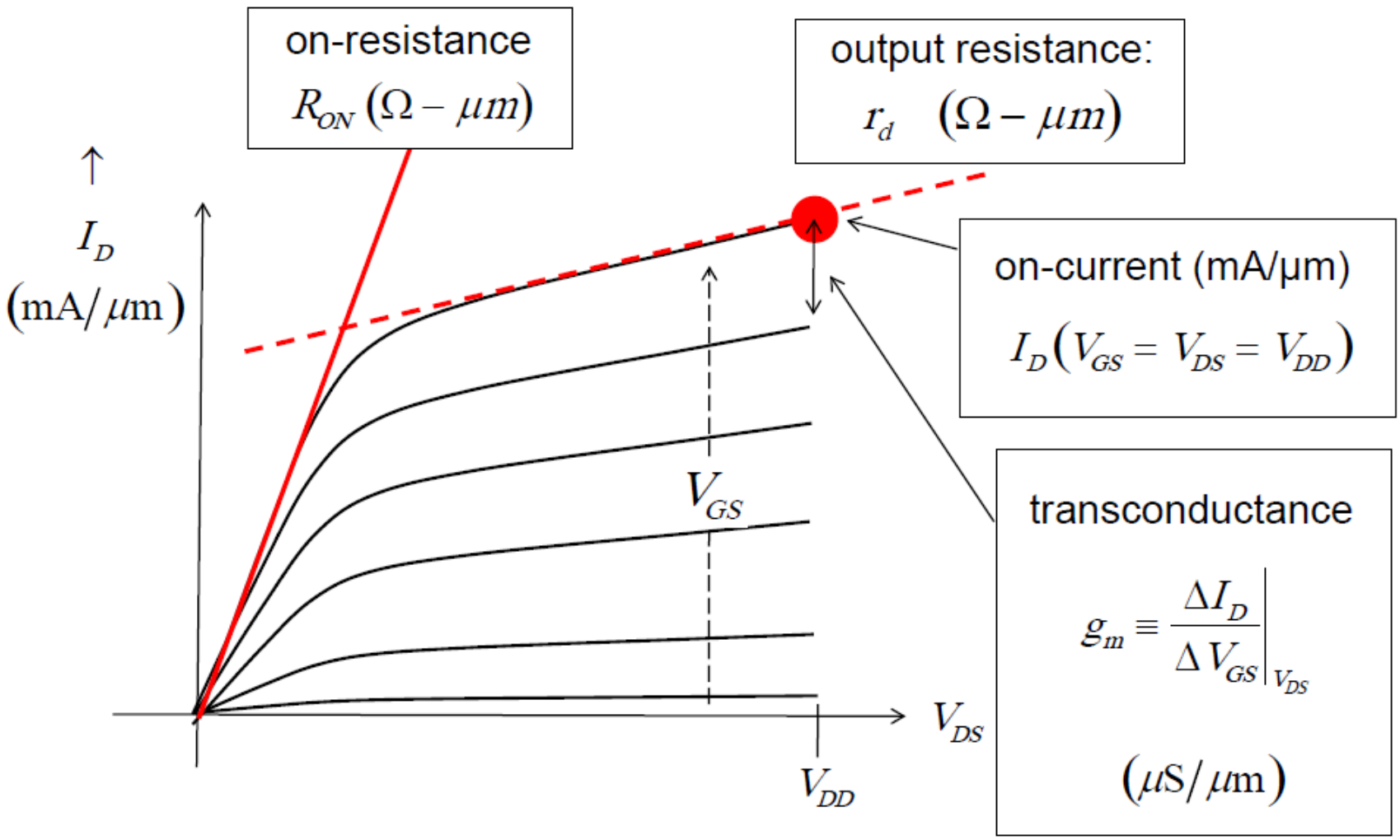
$$I_D = W\,Q_i(x)\upsilon_x(x) = W\,Q_i(0)\upsilon_x(0)$$

$$I_D = W\,C_{ox}\left(V_{GS}-V_T\right)\mu_{eff}\mathcal{E}_x(0)$$

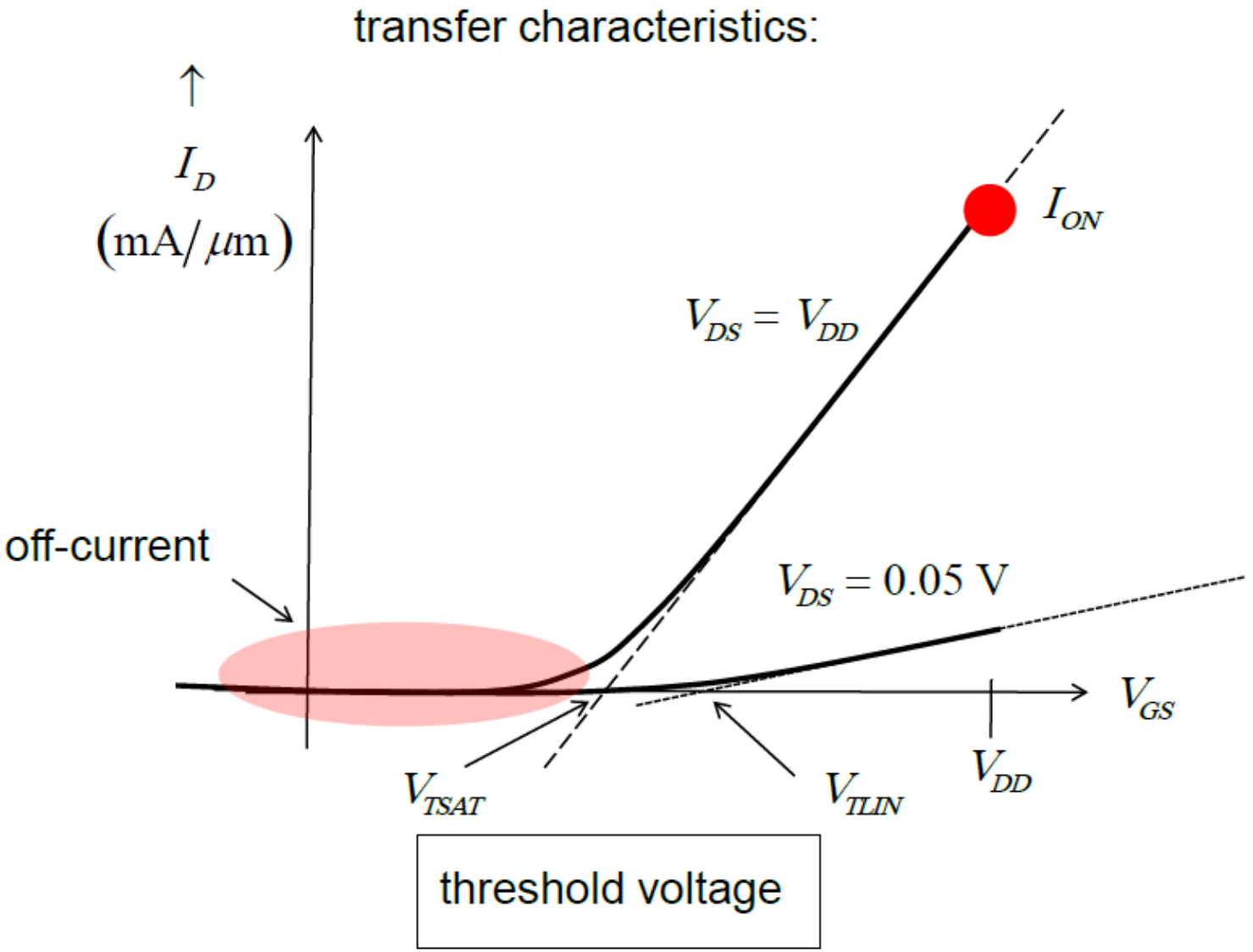
$$\mathcal{E}_x(0) \approx \frac{V_{GS}-V_T}{L}$$

$$I_D = \frac{W}{2L}\mu_{eff}C_{ox}\left(V_{GS}-V_T\right)^2$$

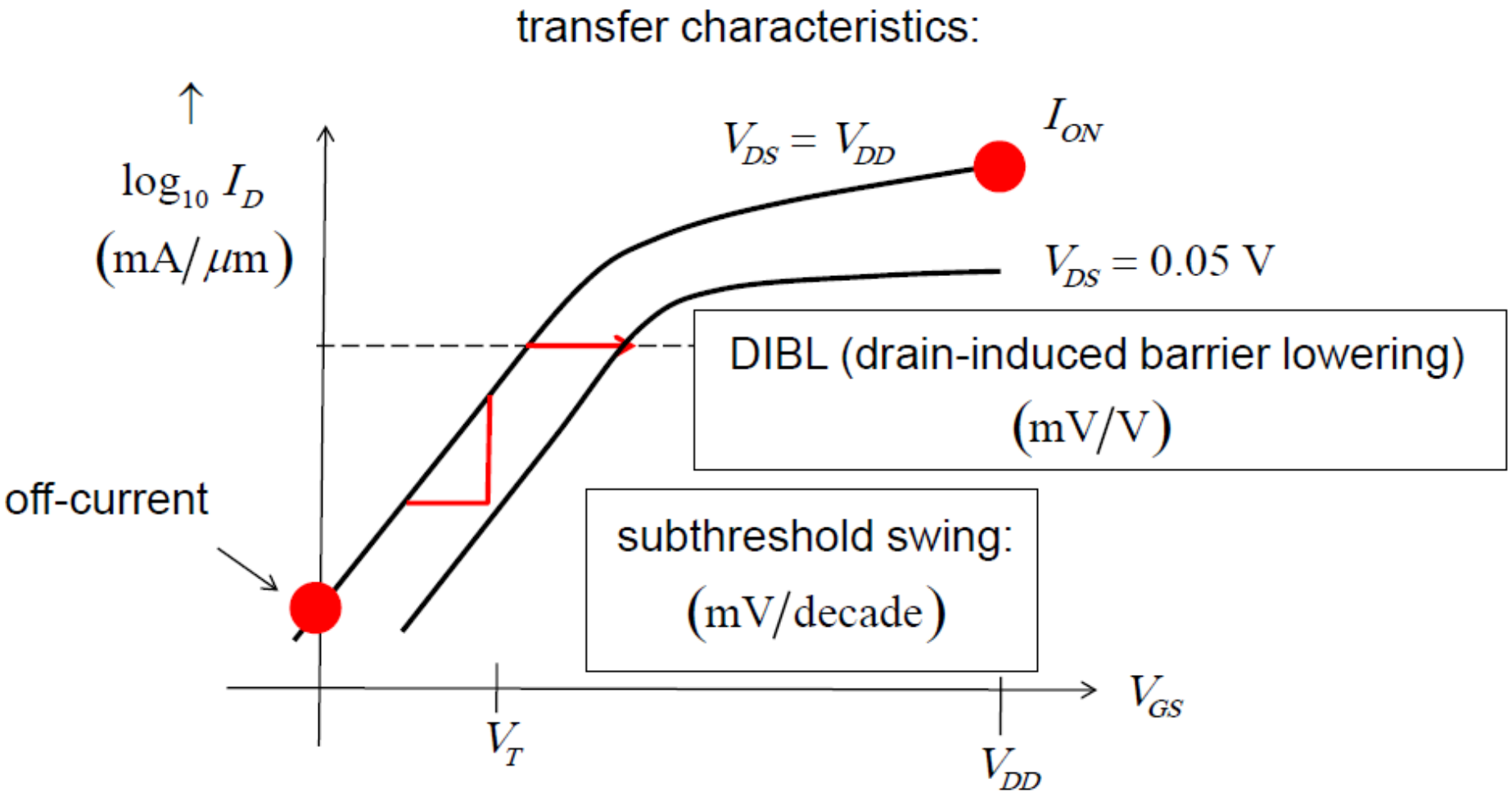
MOSFET Device Metrics: Output Characteristics



MOSFET Device Metrics: Transfer Characteristics



MOSFET Device Metrics: Transfer Characteristics



Some facts

The number of transistors manufactured in 1997 exceeded the number of ants on the planet.

The cost of an IC “fab” is more than $3B, but the cost of a transistor has dropped by more than a factor of one million over the past 30 years.

If the definition of a nanodevice is one that has two dimensions less than 100 nm, then the silicon transistor is the most successful nanodevice currently in production.

(channel length 22 nm and gate oxide thickness, < 2 nm)

Logic Gates

- Gates are basic digital devices.
  - A gate takes one or more inputs and produces an output.
  - Inputs are either 0 or 1.
    - Although they may have very different values of voltage.
  - Output is either 0 or 1.
  - A logic gate's operation is fully described by a truth table.

X	Y	X AND Y
0	0	0
0	1	0
1	0	0
1	1	1

X	Y	X OR Y
0	0	0
0	1	1
1	0	1
1	1	1

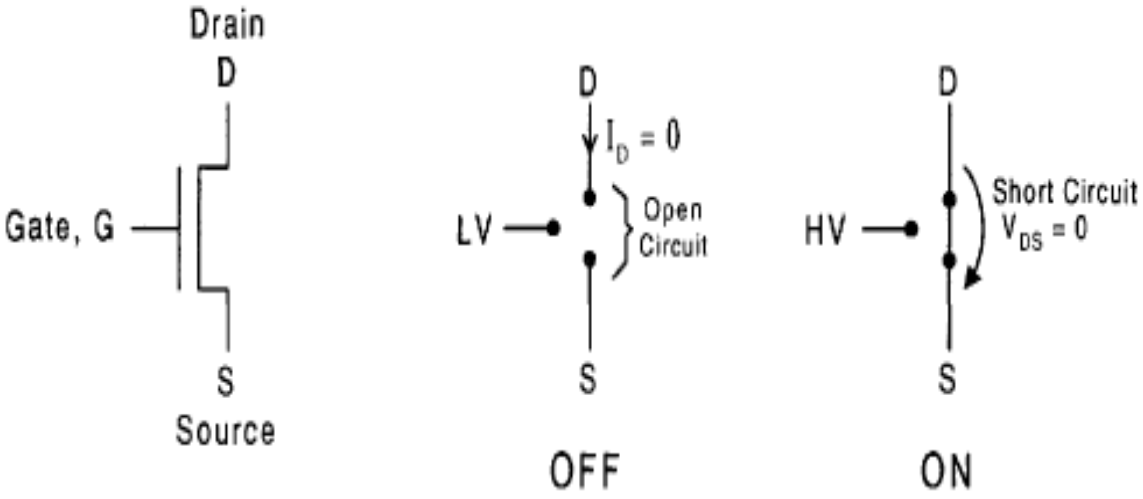
X	NOT X
0	1
1	0

Logic Family

- A logic family is a collection of different integrated-circuit chips that have similar input, output, and internal circuit characteristics, but that perform different logic functions.
- Logic gates are made from transistors.
  - TTL (Transistor-Transistor Logic) family gates are made from bipolar transistors.
  - CMOS (Complementary Metal Oxide Semiconductor) family logic gates are made from MOS transistors.

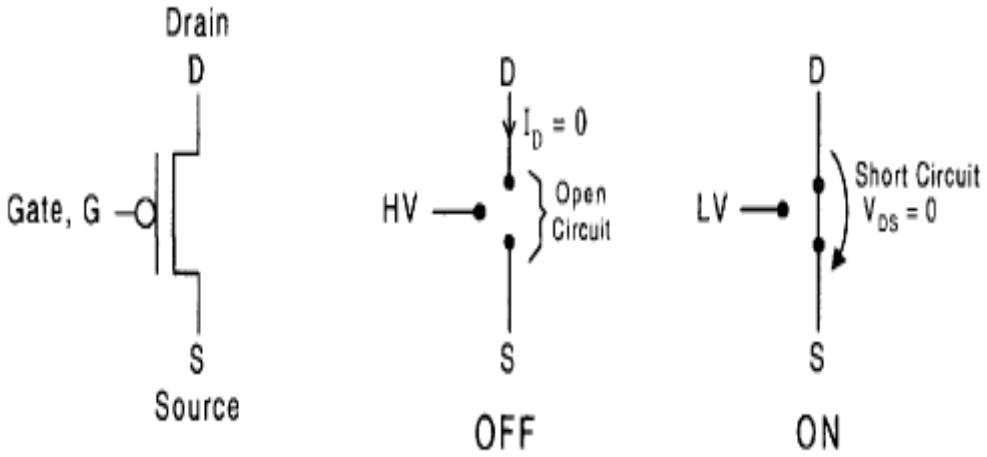
MOS Transistors – N-type MOSFET

- OFF (open circuit) : when gate is logical zero
- ON (short circuit) : when gate is logical one
- Passes a good logical zero
- Degrades a logical one



MOS Transistors – P-type MOSFET

- OFF (open circuit) : when gate is logical one
- ON (short circuit) : when gate is logical zero
- Passes a good logical one
- Degrades a logical zero

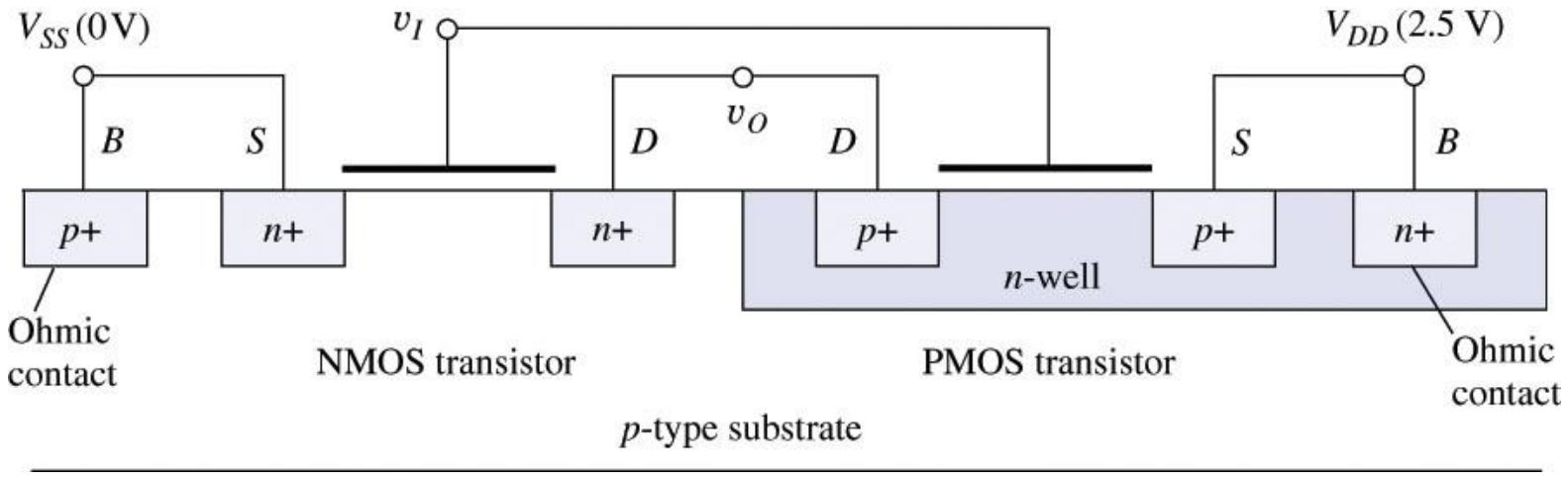


CMOS Inverter Technology

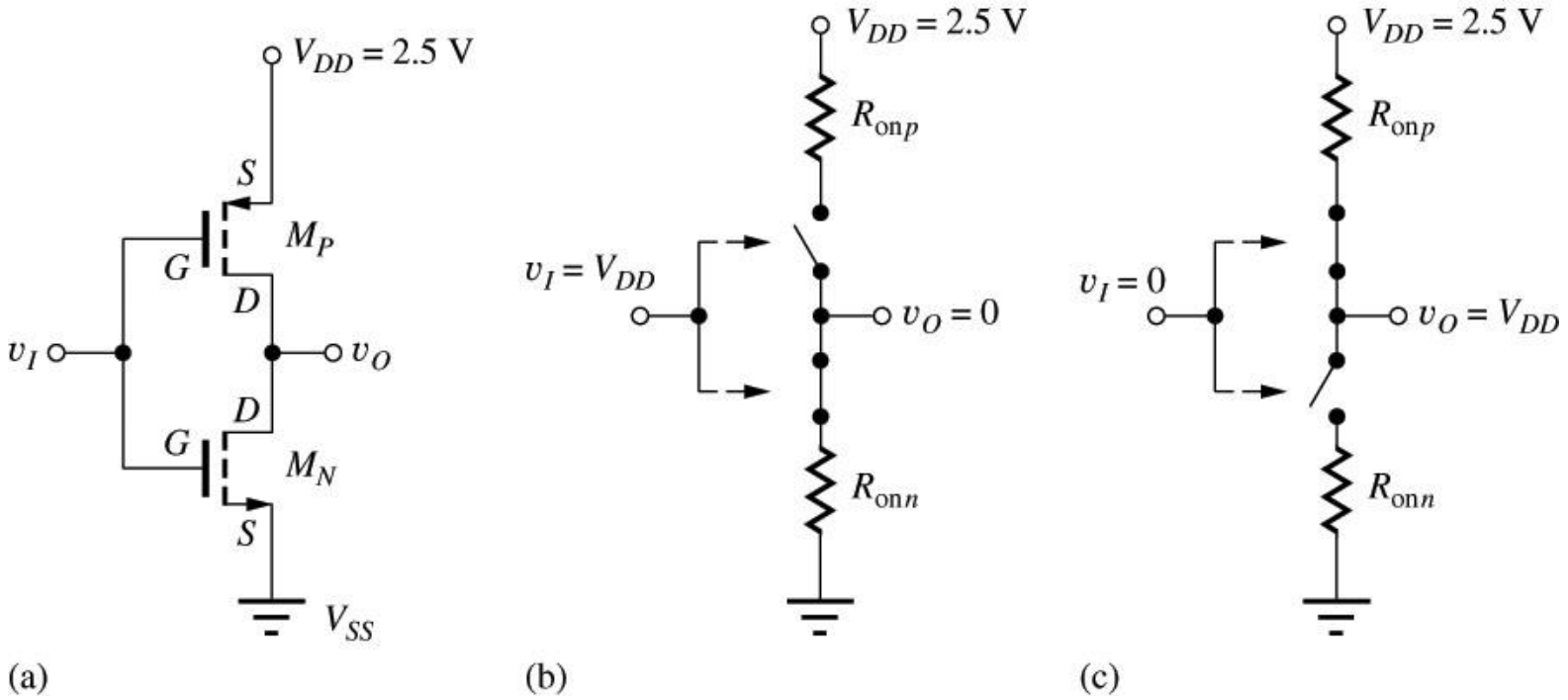
- Complementary MOS, or CMOS, needs both PMOS and NMOS devices for the logic gates to be realized
- The concept of CMOS was introduced in 1963 by Wanlass and Sah, but it did not become common until the 1980's as NMOS microprocessors were dissipating as much as 50 W and alternative design technique was needed
- CMOS dominates digital IC design today

CMOS Inverter Technology

- The CMOS inverter consists of a PMOS device stacked on top on an NMOS device, but they need to be fabricated on the same wafer
- To accomplish this, the technique of “n-well” implantation is needed as shown in this cross-section of a CMOS inverter



CMOS Inverter



(a) Circuit schematic for a CMOS inverter
(b) Simplified operation model with a high input applied
(c) Simplified operation model with a low input applied

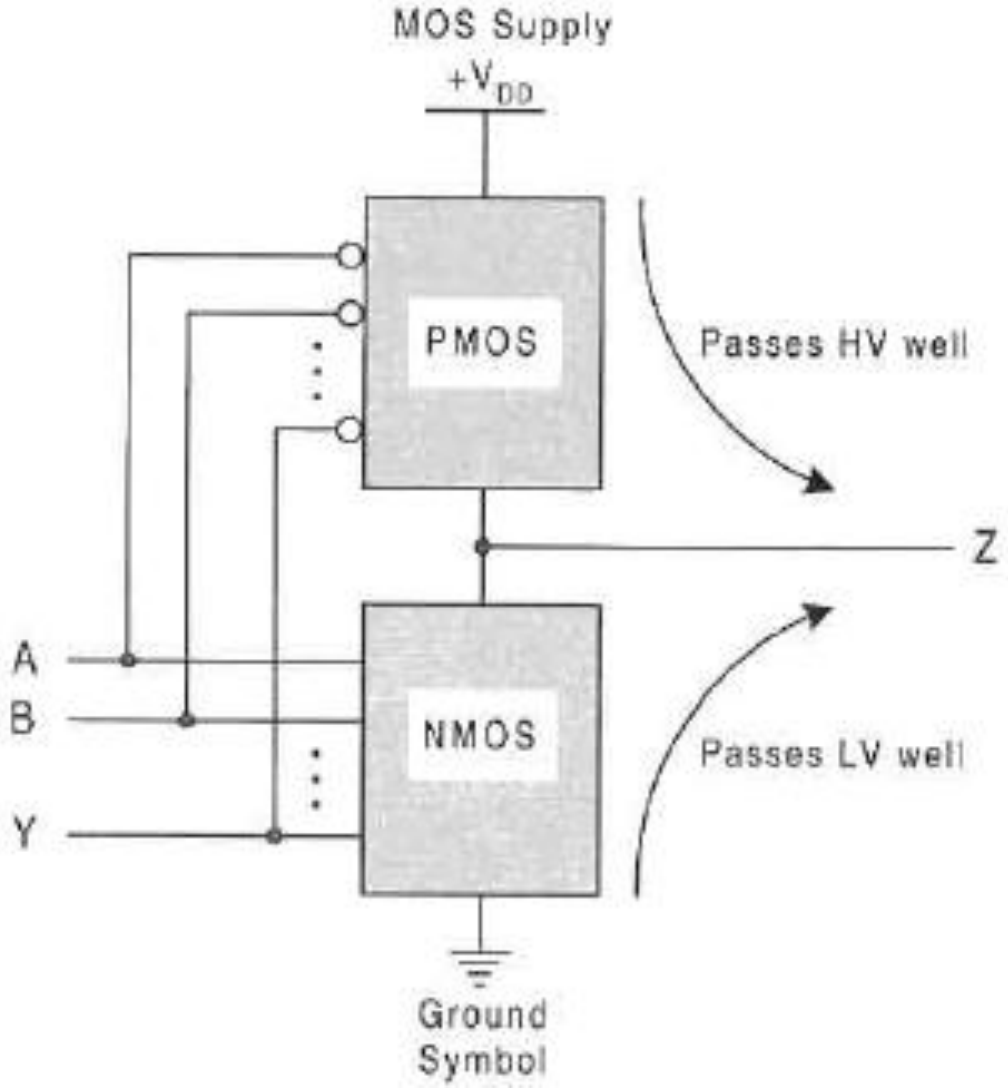
CMOS Inverter Operation

- When v_I is pulled high (to V_{DD}), the PMOS transistor is turned off, while the NMOS device is turned on pulling the output down to V_{SS}
- When v_I is pulled low (to V_{SS}), the NMOS transistor is turned off, while the PMOS device is turned on pulling the output up to V_{DD}

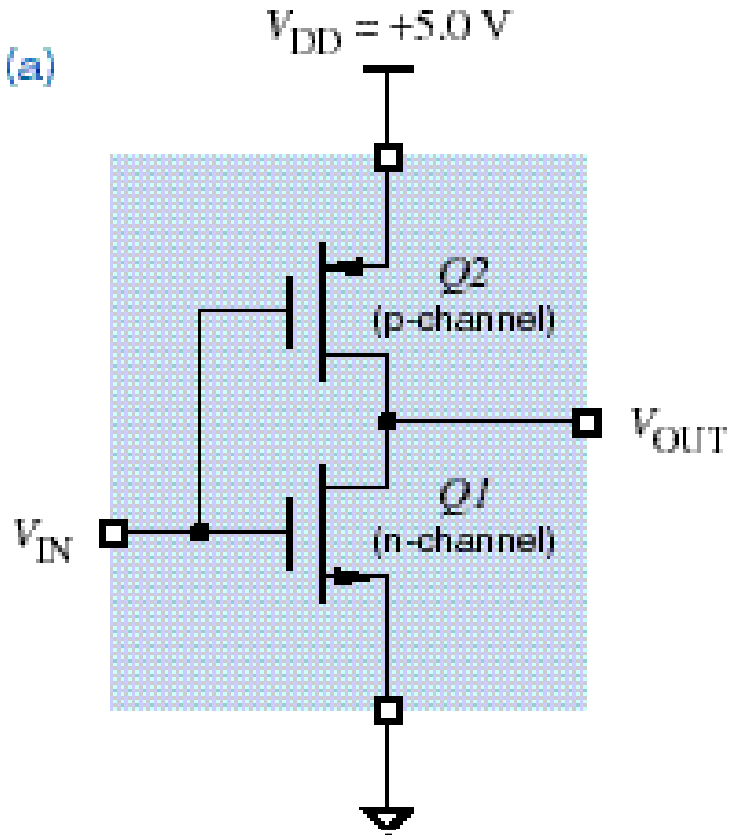
Key Properties

- Full rail-to-rail swing → high noise margins
  - Logic levels not dependent upon the relative device sizes→ Transistors can be minimum size→ ratio less
- Always a path to VDDor GND in steady state → low output impedance (output resistance in kΩ range)→ large fan-out.
- Extremely high input resistance (gate of MOS transistor is near perfect insulator) → nearly zero steady-state input current
- **No direct path steady-state between power and ground**
  - **no static power dissipation**
- Propagation delay function of load capacitance and resistance of transistors

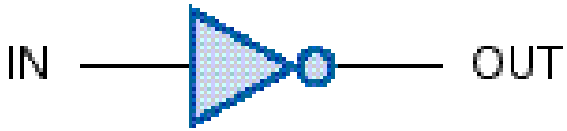
Generalized CMOS Logic Gates



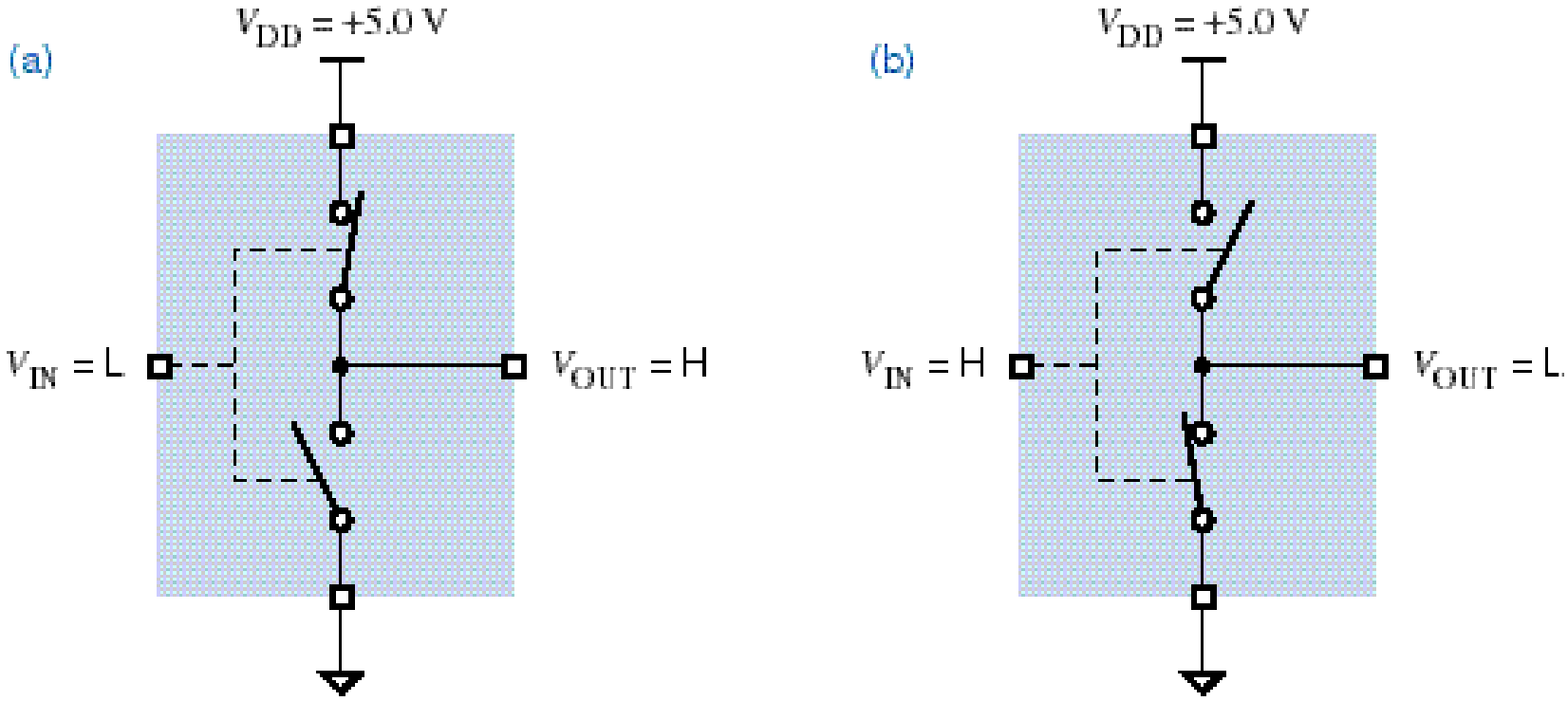
Inverter



V_{IN}	Q1	Q2	V_{OUT}
0.0 (L)	off	on	5.0 (H)
5.0 (H)	on	off	0.0 (L)

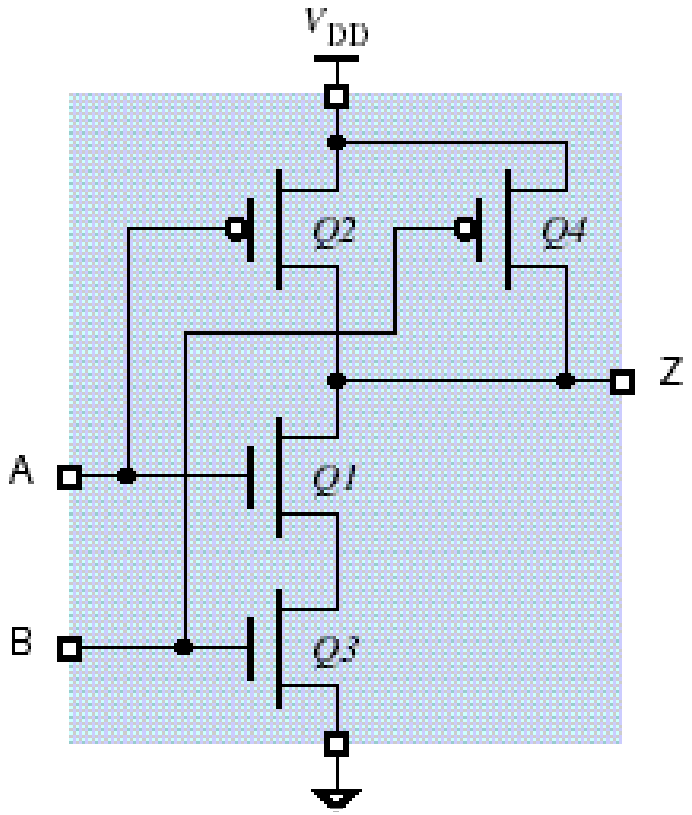


Inverter



NAND – Not AND

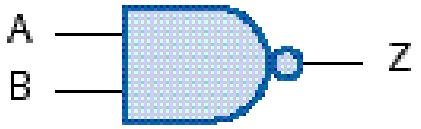
(a)



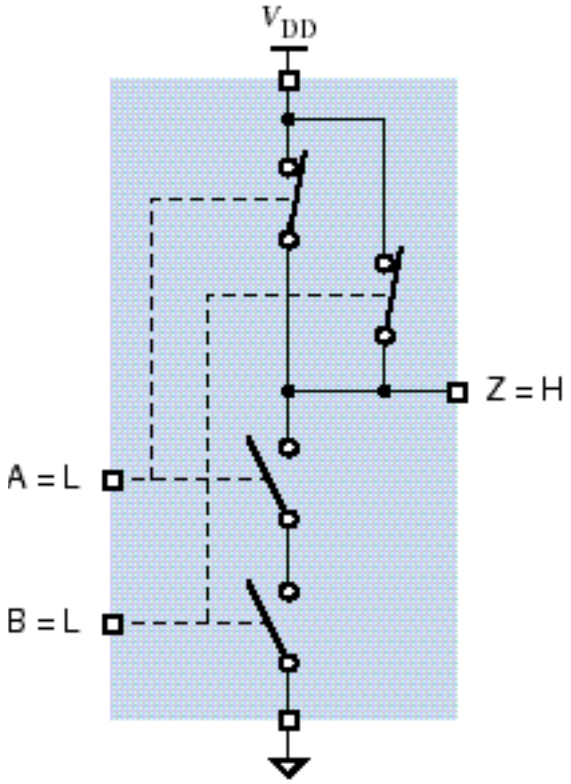
(b)

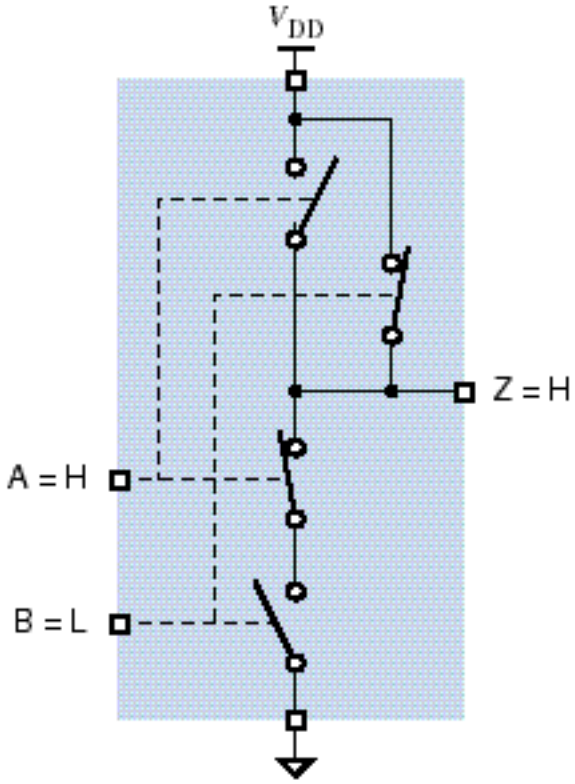
A	B	*Q1*	*Q2*	*Q3*	*Q4*	Z
L	L	off	on	off	on	H
L	H	off	on	on	off	H
H	L	on	off	off	on	H
H	H	on	off	on	off	L

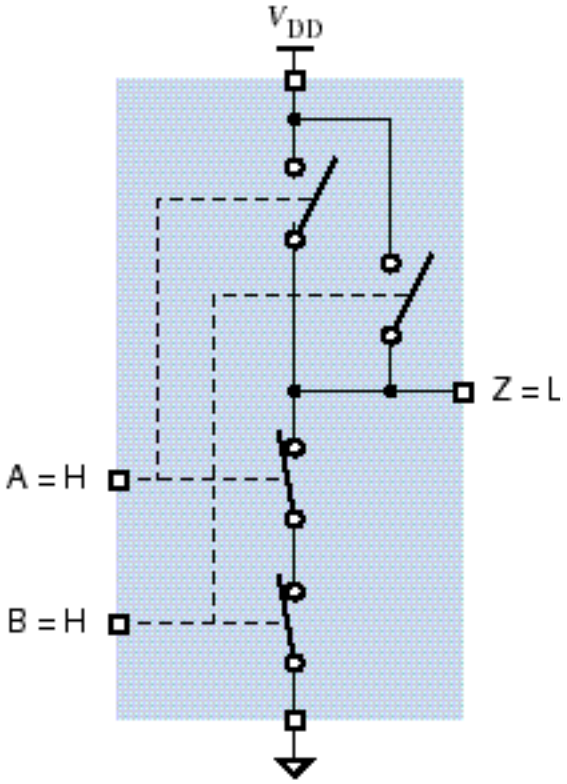
(c)



NAND

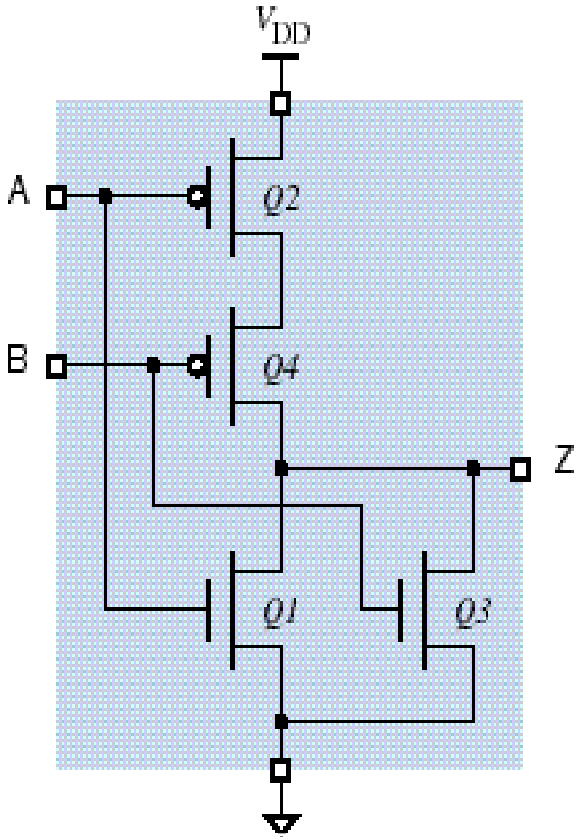






NOR – Not OR

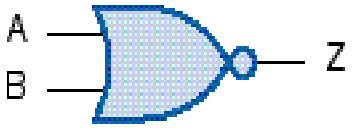
(a)



(b)

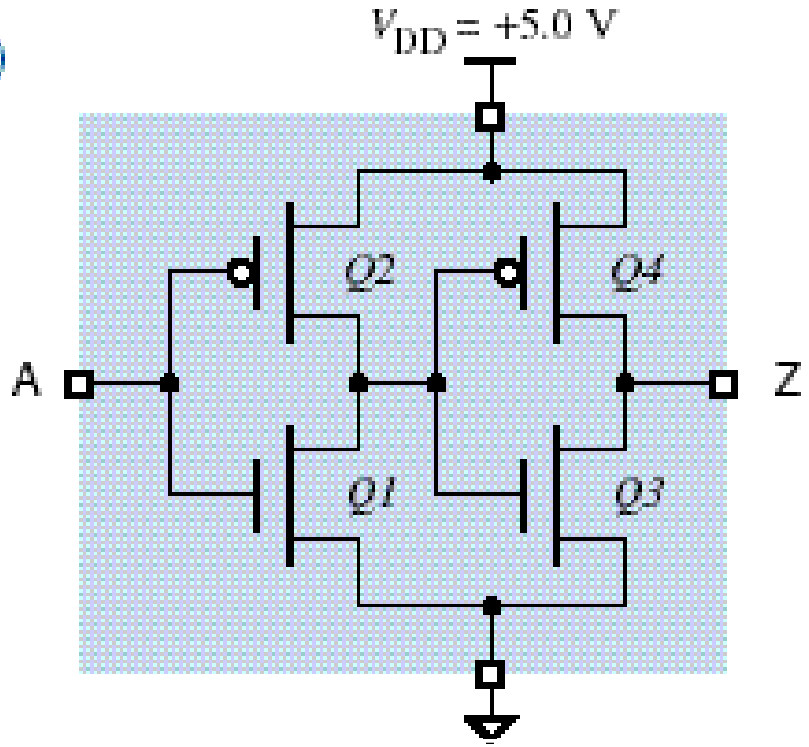
A	B	Q1	Q2	Q3	Q4	Z
L	L	off	on	off	on	H
L	H	off	on	on	off	L
H	L	on	off	off	on	L
H	H	on	off	on	off	L

(c)



Non-inverting Buffer

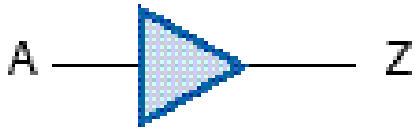
(a)



(b)

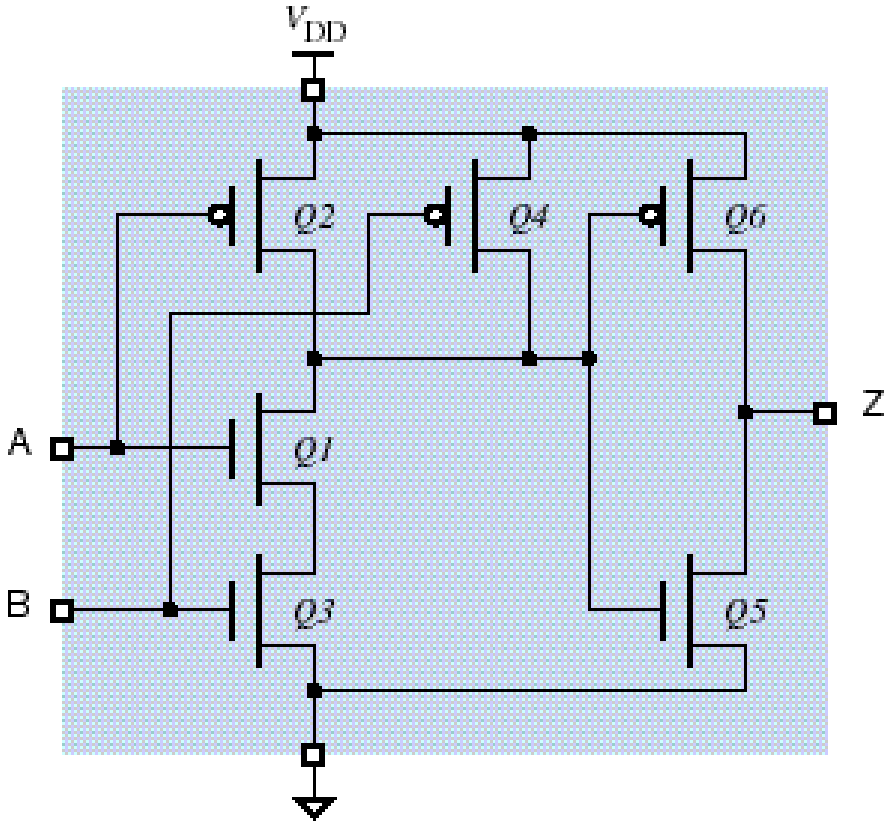
A	Q1	Q2	Q3	Q4	Z
L	off	on	on	off	L
H	on	off	off	on	H

(c)



AND Gate

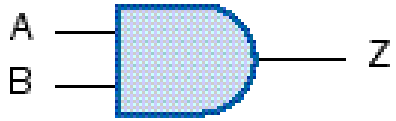
(a)



(b)

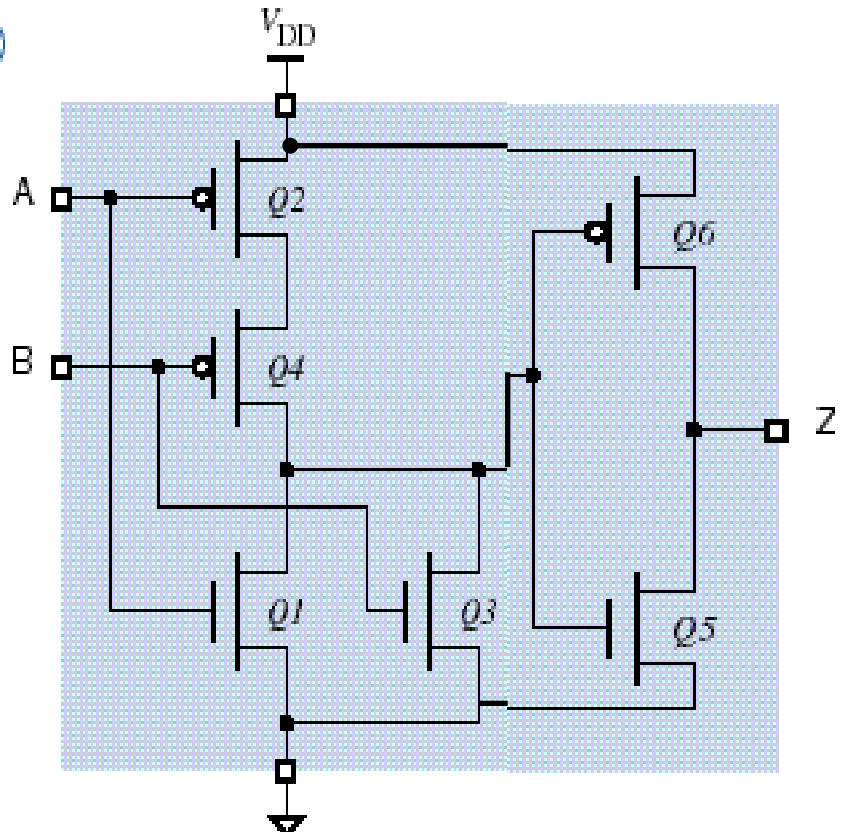
A	B	Q1	Q2	Q3	Q4	Q5	Q6	Z
L	L	off	on	off	on	on	off	L
L	H	off	on	on	off	on	off	L
H	L	on	off	off	on	on	off	L
H	H	on	off	on	off	off	on	H

(c)



OR Gate

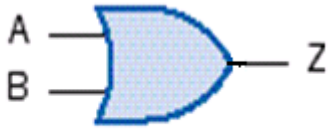
(a)



(b)

A	B	Q1	Q2	Q3	Q4	Q5	Q6	Z
L	L	off	on	off	on	on	off	L
L	H	off	on	on	off	on	off	H
H	L	on	off	off	on	on	off	H
H	H	on	off	on	off	off	on	H

(c)



Key CMOS Electrical Characteristics

- Logic voltage levels
- DC noise margin
- Speed
- Power consumption
- Fan-in
- Fan-out

Key CMOS Electrical Characteristics

- Logic voltage levels
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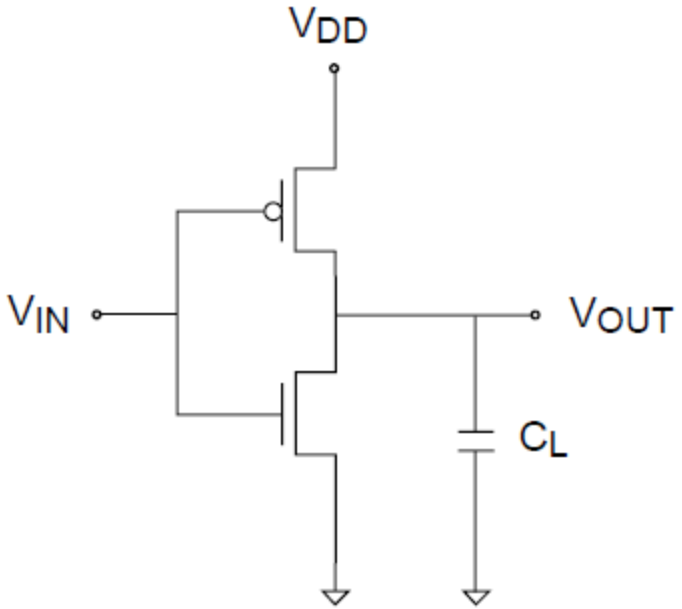
CMOS Inverter



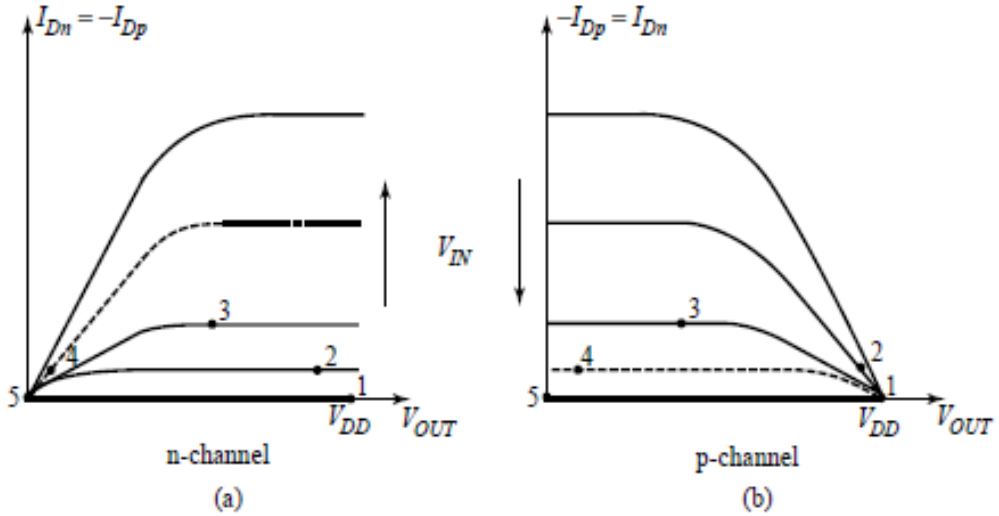
- No power consumption while idle in any logic state
  - No static power dissipation

Basic Operation:

- $V_{IN} = 0 \Rightarrow V_{OUT} = V_{DD}$
  $V_{GSn} = 0 < V_{Tn} \Rightarrow$ **NMOS OFF**
  $V_{SGp} = V_{DD} > -V_{Tp} \Rightarrow$ **PMOS ON**
- $V_{IN} = V_{DD} \Rightarrow V_{OUT} = 0$
  $V_{GSn} = V_{DD} > V_{Tn} \Rightarrow$ **NMOS ON**
  $V_{SGp} = 0 < -V_{Tp} \Rightarrow$ **PMOS OFF**

CMOS Static Characteristics

Output characteristics of both transistors:



Note:

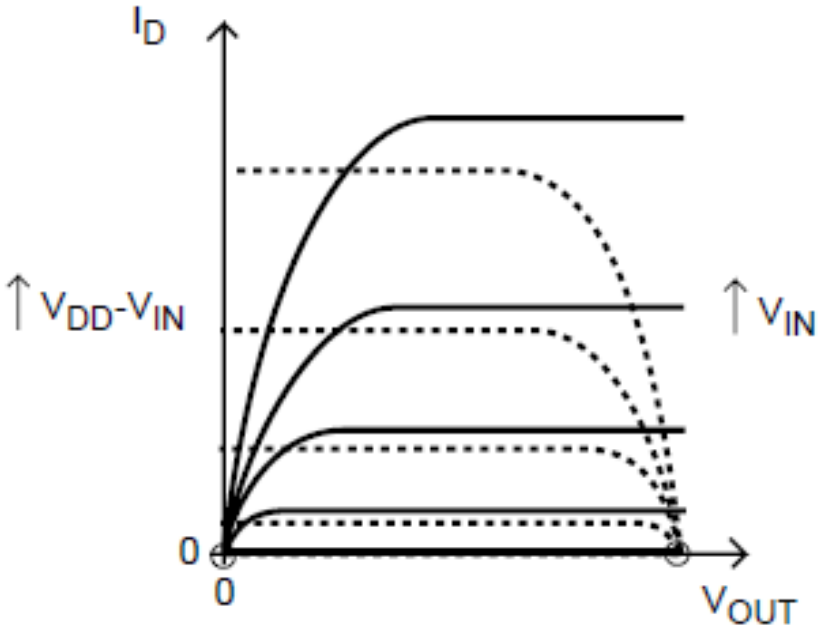
$V_{IN} = V_{GSn} = V_{DD} - V_{SGp} \Rightarrow V_{SGp} = V_{DD} - V_{IN}$

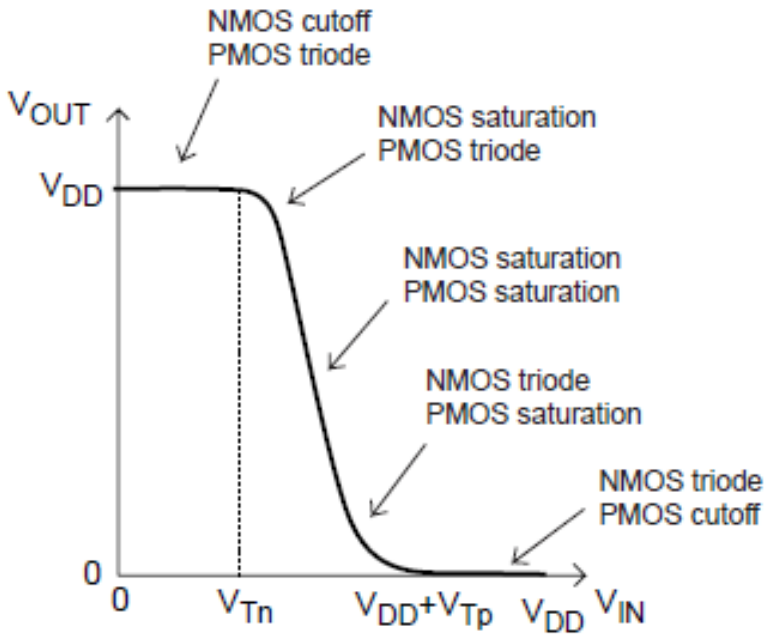
$V_{OUT} = V_{DSn} = V_{DD} - V_{SDp} \Rightarrow V_{SDp} = V_{DD} - V_{OUT}$

$I_{Dn} = -I_{Dp}$

Combine into single diagram of I_D vs. V_{OUT} with V_{IN} as parameter

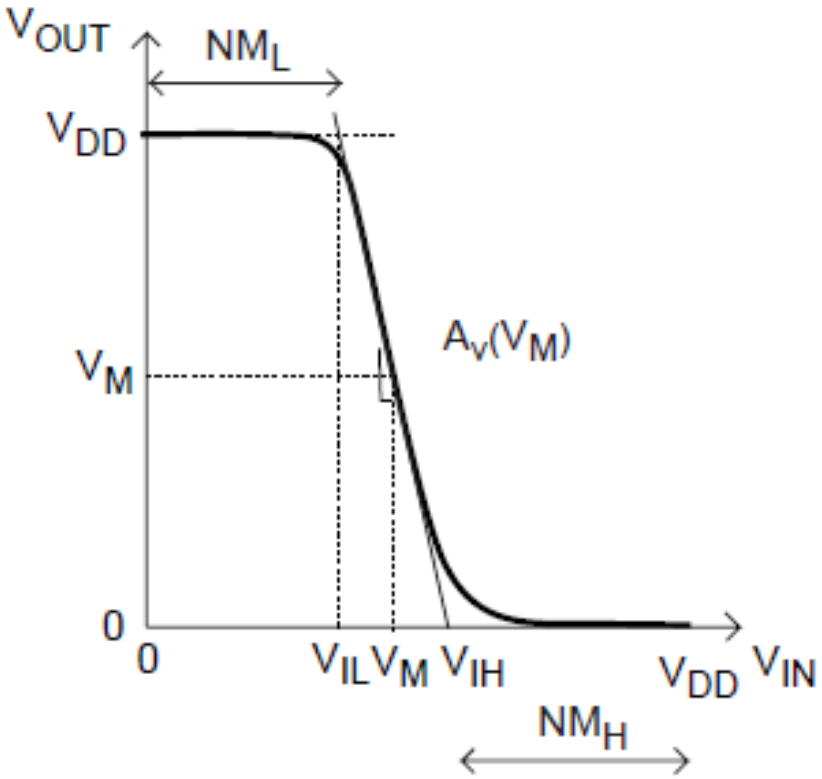
CMOS Inverter Static Characteristics





- Rail-to-Rail logic: logic levels are “0” and “VDD”
- High $|A_v|$ around threshold → high noise margins

CMOS Inverter: Noise Margins



- Calculate V_M
- Calculate $A_v(V_M)$
- Calculate NM_H and NH_L

CMOS Inverter: V_M

Calculate V_M ($V_M = V_{IN} = V_{OUT}$)

At V_M both transistors are saturated:

$$I_{Dn} = \frac{W_n}{2L_n}\mu_n C_{ox}\left(V_M - V_{Tn}\right)^2$$

$$-I_{Dp} = \frac{W_p}{2L_p}\mu_p C_{ox}\left(V_{DD} - V_M + V_{Tp}\right)^2$$

CMOS Inverter: V_M

Define:

$$k_n = \frac{W_n}{L_n}\mu_n C_{ox}; \qquad k_p = \frac{W_p}{L_p}\mu_p C_{ox}$$

Since :

$$I_{Dn} = -I_{Dp}$$

Then:

$$\frac{1}{2}k_n(V_M - V_{Tn})^2 = \frac{1}{2}k_p(V_{DD} - V_M + V_{Tp})^2$$

Solve for V_M:

$$V_M = \frac{V_{Tn} + \sqrt{\frac{k_p}{k_n}}(V_{DD} + V_{Tp})}{1 + \sqrt{\frac{k_p}{k_n}}}$$

Usually, V_{Tn} and V_{Tp} fixed and $V_{Tn} = -V_{Tp}$
$\Rightarrow$ V_M engineered through k_p/k_n ratio.

CMOS Inverter: V_M

- **Symmetric case**: $k_n = k_p$

$$V_M = \frac{V_{DD}}{2}$$

This implies:

$$\frac{k_p}{k_n} = 1 = \frac{\frac{W_p}{L_p}\mu_p C_{ox}}{\frac{W_n}{L_n}\mu_n C_{ox}} \approx \frac{\frac{W_p}{L_p}\mu_p}{\frac{W_n}{L_n}2\mu_p} \Rightarrow \frac{W_p}{L_p} \approx 2\frac{W_n}{L_n}$$

Since usually $L_p \approx L_n = L_{min} \Rightarrow W_p \approx 2W_n$

- **Asymmetric case**: $k_n >> k_p$, or $\frac{W_n}{L_n} >> \frac{W_p}{L_p}$

$$V_M \approx V_{Tn}$$

NMOS turns on as soon as V_{IN} goes above V_{Tn}.

- **Asymmetric case**: $k_n << k_p$, or $\frac{W_n}{L_n} << \frac{W_p}{L_p}$

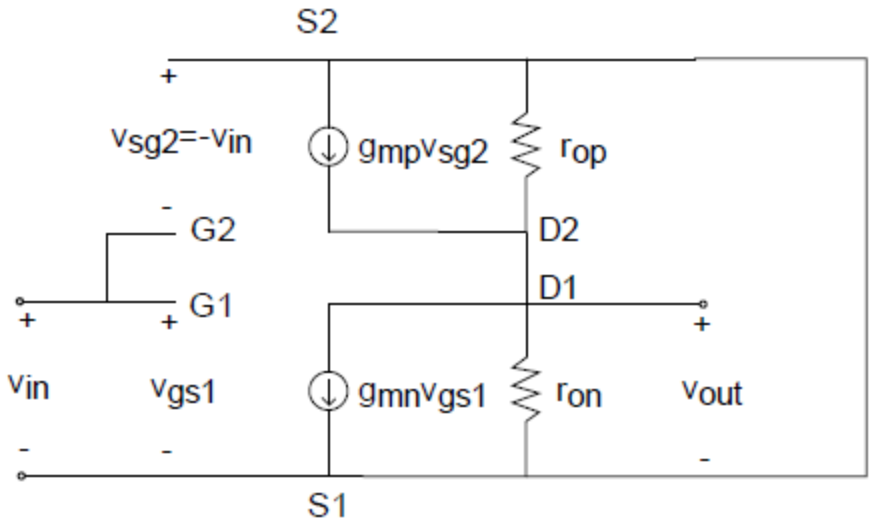
$$V_M \approx V_{DD} + V_{Tp}$$

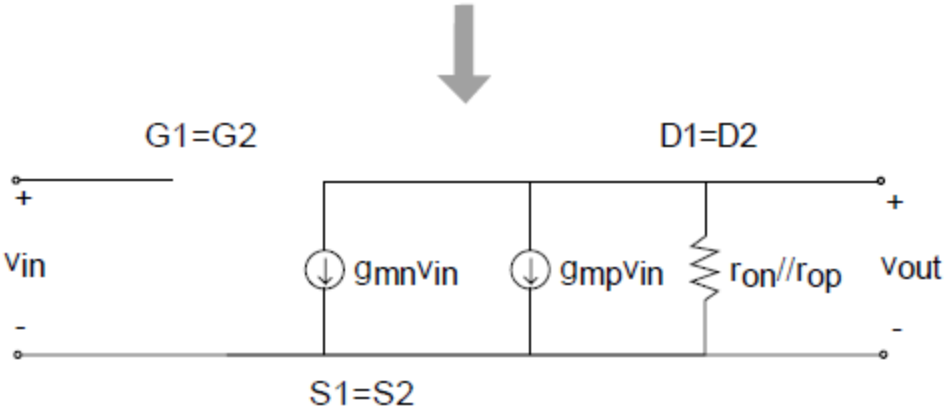
PMOS turns on as soon as V_{IN} goes below $V_{DD} + V_{Tp}$.

- Sizing of the transistors can be used to tune V_M

CMOS Inverter: A_v

Small Signal Model

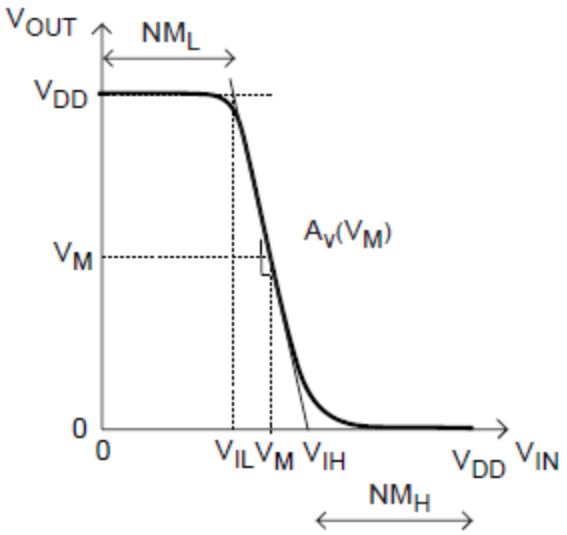




$$A_v = -(g_{mn} + g_{mp})(r_{on} // r_{op})$$

- A_v can be quite large

CMOS Inverter: Noise Margins



- High A_v gives high noise margins

- Noise-margin low, NM_L:

$$V_{IL} = V_M - \frac{V_{DD} - V_M}{|A_v|}$$

$$NM_L = V_{IL} - V_{OL} = V_{IL} = V_M - \frac{V_{DD} - V_M}{|A_v|}$$

- Noise-margin high, NM_H:

$$V_{IH} = V_M\left(1 + \frac{1}{|A_v|}\right)$$

$$NM_H = V_{OH} - V_{IH} = V_{DD} - V_M\left(1 + \frac{1}{|A_v|}\right)$$

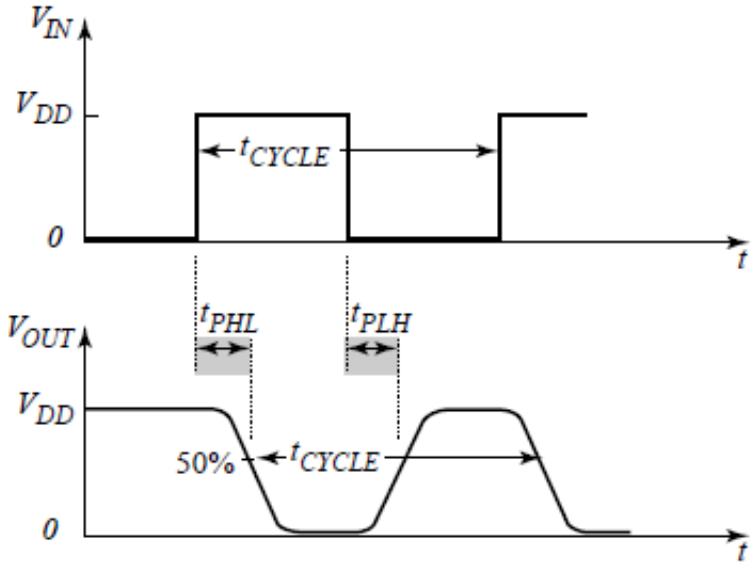
CMOS Inverter: Speed (Propagation Delay)

Inverter propagation delay: time delay between input and output signals; figure of merit of logic speed.

Typical propagation delays: < 100 ps.

Complex logic system has 10-50 propagation delays per clock cycle.

Estimation of t_p: use square-wave at input



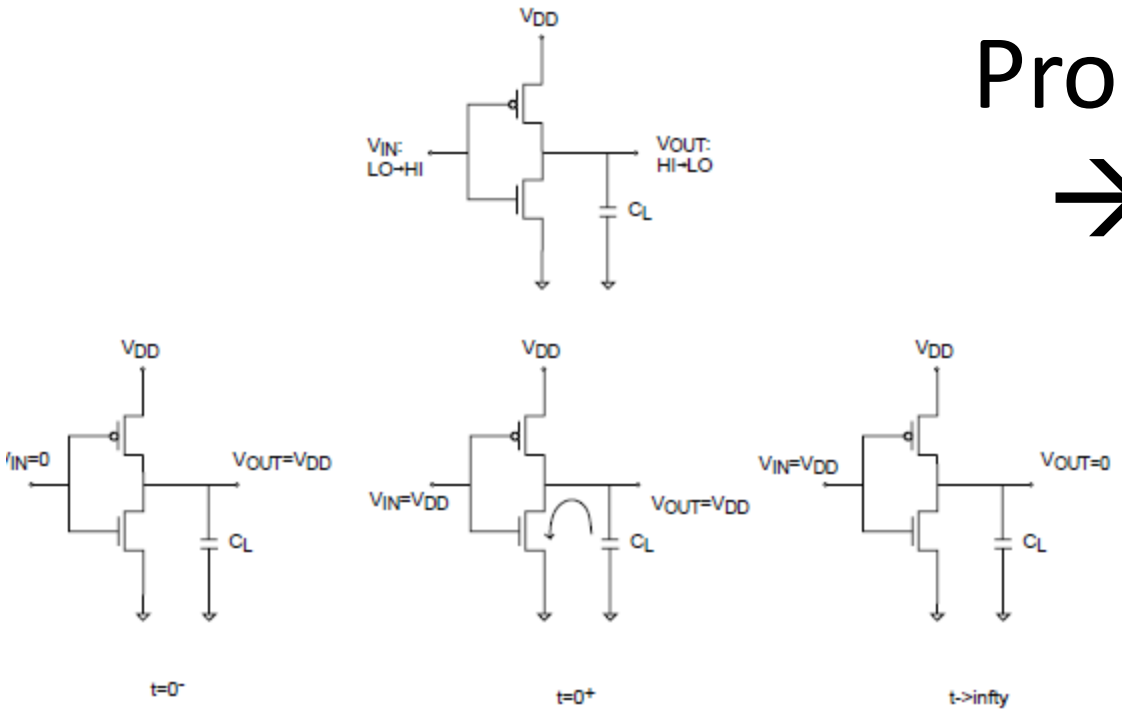
- More the delay less is the speed

Average propagation delay:

$$t_p = \frac{1}{2}(t_{PHL} + t_{PLH})$$

CMOS Inverter: Propagation Delay → High to Low

Propagation delay high-to-low



During early phases of discharge, NMOS is saturated and PMOS is cut-off.

Time to discharge ***half*** of charge stored in C_L:.

$$t_{pHL} \approx \frac{\frac{1}{2}\text{charge on } C_L \ @t = 0^-}{\text{NMOS discharge current}}$$

- Discharging of Load Capacitance

CMOS Inverter: Propagation Delay → High to Low

Charge in C_L at t=0⁻:

$$Q_L(t = 0^-) = C_L V_{DD}$$

Discharge Current (NMOS in saturation):

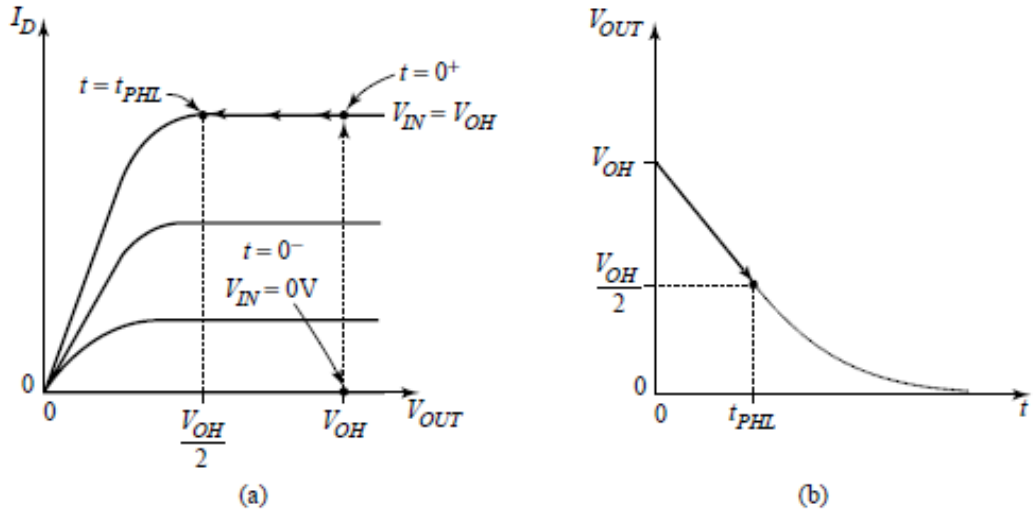
$$I_{Dn} = \frac{W_n}{2L_n}\mu_n C_{ox}(V_{DD} - V_{Tn})^2$$

Then:

$$t_{PHL} \approx \frac{C_L V_{DD}}{\frac{W_n}{L_n}\mu_n C_{ox}(V_{DD} - V_{Tn})^2}$$

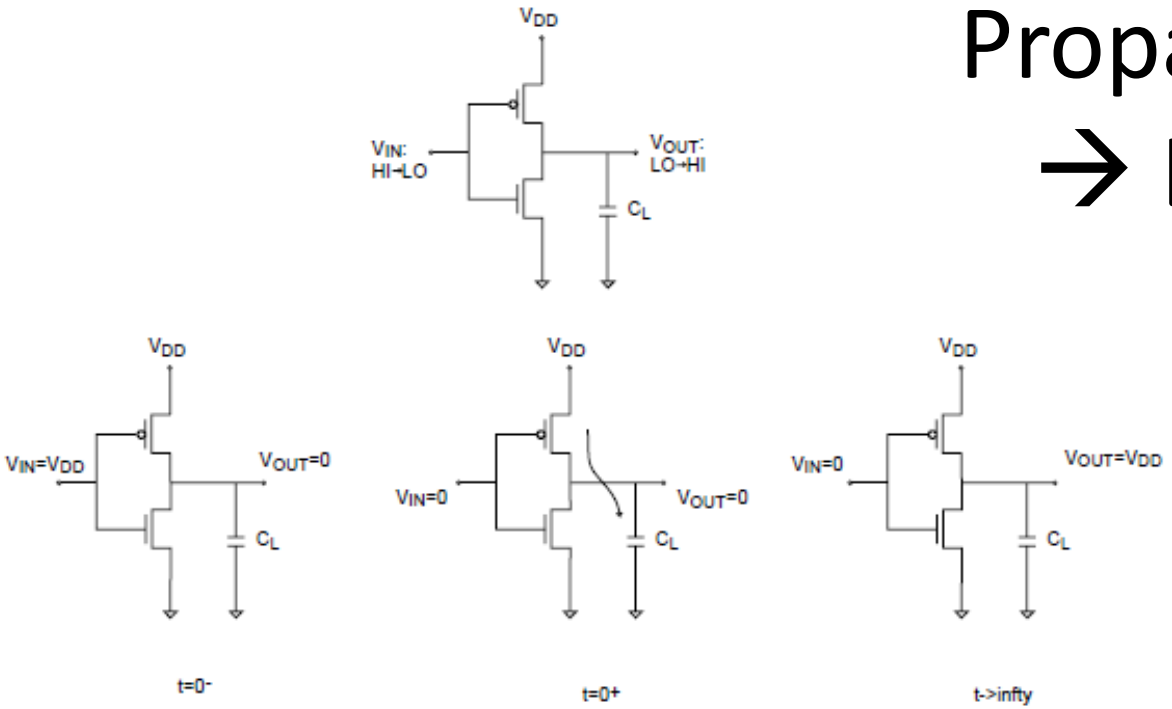
- High V_{DD} reduces t_{PHL}
- Higher current (I) reduces t_{pHL}

Graphical Interpretation



CMOS Inverter: Propagation Delay → Low to High

- Charging of load capacitance



During early phases of discharge, PMOS is saturated and NMOS is cut-off.

Time to charge to ***half*** of final charge on C_L:.

$$t_{PLH} \approx \frac{\frac{1}{2}\text{charge on } C_L \ @t=\infty}{\text{PMOS charge current}}$$

CMOS Inverter: Propagation Delay → Low to High

Charge in C_L at $t=\infty$:

$$Q_L(t=\infty) = C_L V_{DD}$$

Charge Current (PMOS in saturation):

$$-I_{Dp} = \frac{W_p}{2L_p}\mu_p C_{ox}\left(V_{DD} + V_{Tp}\right)^2$$

Then:

$$t_{PLH} \approx \frac{C_L V_{DD}}{\frac{W_p}{L_p}\mu_p C_{ox}\left(V_{DD} + V_{Tp}\right)^2}$$

Key dependencies of propagation delay:

- $V_{DD} \uparrow \Rightarrow t_p \downarrow$
  - Reason: $V_{DD} \uparrow \Rightarrow Q(C_L) \uparrow$, but I_D goes as square$\uparrow$
  - Trade-off: $V_{DD} \uparrow \Rightarrow$ more power consumed.
- $L \downarrow \Rightarrow t_p \downarrow$
  - Reason: $L \downarrow \Rightarrow I_D \uparrow$
  - Trade-off: manufacturing cost!

- Scaling L can help reduce delay
  - New CMOS technologies
- Increasing V_{DD} → higher power!

Power Dissipation

- Energy from power supply needed to charge up the capacitor:

$$E_{charge} = \int V_{DD} i(t) dt = V_{DD} Q = V_{DD}^2 C_L$$

- Energy stored in capacitor:

$$E_{store} = 1/2 C_L V_{DD}^2$$

- Energy lost in p-channel MOSFET during charging:

$$E_{diss} = E_{charge} - E_{store} = 1/2 C_L V_{DD}^2$$

- During discharge the n-channel MOSFET dissipates an identical amount of energy.

- If the charge/discharge cycle is repeated f times/second, where f is the clock frequency, the dynamic power dissipation is:

$$P = 2 E_{diss} * f = C_L V_{DD}^2 f$$

In practice many gates do not change state every clock cycle which lowers the power dissipation.

- Note
  - V_{DD} dependence
  - f-dependence
- Reduction of C_L is a win-win for both speed and power