CS341 - Lab on Memory Caching

Wed, Oct 19th 2016

1 Goals

- Learning to use a cache simulator
- Understanding and analyzing cache performance using program traces on the cache simulator

2 Instructions

- These exercises are to be done individually. While you are encouraged to discuss with your colleagues, do not cross the fine line between discussion to understand versus discussion as a short-cut to complete your lab without really understanding.
- Create a directory called $< rollno > - < labno >$. Store all relevant files to this lab in that directory.
- In the exercises, you will be asked various questions. Note down the answers to these in a file called $< rollno > - < labno > .txt$.
- In some parts of the exercises, you will have to show a demo to a TA; these are marked as such. The evaluation for each lab will be in the subsequent lab, or during a time-slot agreed upon with the TAs. For this evaluation, you need to upload your code as well.
- While submitting (on moodle), you have to create a tar.gz or zip of the entire $< rollno > - < labno >$ directory in which all your relevant files reside.
- Before leaving the lab, ensure the following: (1) You have signed the attendance sheet (2) You have uploaded your submission

3 Understanding the dineroIV cache simulator

dineroIV is a cache simulator which takes as input a program's memory access trace. The program is installed in /opt/dineroIV in the NSL machines.

Learn to use the dineroIV simulator. You can use the man page as `man /opt/dineroIV/d4.1` or use the "-help" command line option. Learn the various cache configuration options; there may be some which you do not understand, that's alright.

Also learn the input trace format. There are some memory access traces from real programs, given in the directory "/opt/dineroIV/traces". Can you interpret the format? The man page above tells you the data format.

4 Warmup exercise

Use the following cache configuration: unified cache size of 4KB, 4-word blocks, direct-mapped, write-back+write-allocate.

Question [1 mark]: If the Nth memory reference is the first non-compulsory miss, find the value of N. Find N for each of the 3 trace files given. Hint: the simulator can be told to run for only a certain number of memory references.

5 Impact of cache size

Use the following cache configuration: unified cache, 2-way set associative, 4-word blocks, write-back+write-allocate.

Question [3 marks]: Vary the cache size from 4KB to 512KB (8 different sizes). Plot the miss-rate as a function of the cache size. Your graph should have 3 plots: one for each of the 3 trace files. Explain the shape of the graph.

6 Impact of block size

Use the following cache configuration: unified cache of 8KB size, 2-way set associative, write-back+write-allocate.

Question [3 marks]: Vary the block size from 1-word to 256-words (9 different sizes). Plot the miss-rate as a function of the block size. The graph should have one plot each for the 3 trace files. Explain the shape of the graph.

7 Impact of associativity

Use the following cache configuration: unified cache of 8KB cache size, 4-word blocks, write-back+write-allocate.

Question [3 marks]: Vary the associativity from the minimum possible to the maximum possible. Plot the miss-rate as a function of the associativity. As earlier, there should be a plot each for the 3 trace files. Explain the shape of the graph.