MEMORY-REFERENCE INSTRUCTIONS

TABLE 5-4 Memory-Reference Instructions

Symbol	Operation decoder	Symbolic description
AND	D_0	$AC \leftarrow AC \wedge M[AR]$
ADD	D_1	$AC \leftarrow AC + M[AR], \quad E \leftarrow C_{out}$
LDA	D_2	$AC \leftarrow M[AR]$
STA	D_3	$M[AR] \leftarrow AC$
BUN	D_4	$PC \leftarrow AR$
BSA	D_5	$M[AR] \leftarrow PC, \quad PC \leftarrow AR + 1$
ISZ	D_6	$M[AR] \leftarrow M[AR] + 1,$ If $M[AR] + 1 = 0$ then $PC \leftarrow PC + 1$

AND:

D0T4 : DR ← M[AR]

D0T5 : AC ← AC & DR,

SC ← 0

ADD:

D1T4 : DR ← M[AR]

D1T5 : AC ← AC + DR,

E ← C out

SC ← 0

LDA: LOAD AC

D2T4 : DR ← M[AR]

D2T5 : AC ← DR,

SC ← 0

; VERİ YOLU DOĞRUDAN AC YE BAĞLI DEĞİLDİR. BU YUZDEN ONCE DR YE DAHA SONRA AC YE VERI AKTARILIR. VERİ YOLUNUN AC YE DOĞRUDAN BAĞLI OLMAMASININ SEBEBI TOPLAYICI VE MANTIK BIRIMLERINDEKI GECIKMELERDIR.

STA: STORE AC

$D_3T_4 : M[AR] \leftarrow AC,$

$SC \leftarrow 0$

; AC NIN ÇIKIŞLARI VERİ YOLUNA, VERI YOLUDA BELLEĞİN VERİ GİRİŞLERİNE BAGLI OLDUGUNDAN TEK BIR MIKRO ISLEMLE YAPILABILIR.

BUN: BRANCH UNCONDITIONAL

$D_4T_4 : PC \leftarrow AR,$

$SC \leftarrow 0$

BSA: BRANCH AND SAVE RETURN ADDRESS

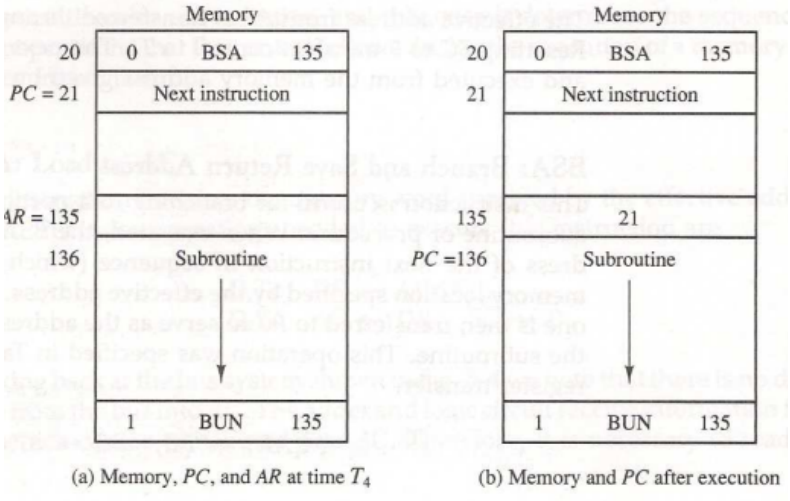
$D_5T_4 : M[AR] \leftarrow PC,$

$AR \leftarrow AR + 1$

$D_5T_5 : PC \leftarrow AR,$

$SC \leftarrow 0$

Figure 5-10 Example of BSA instruction execution.



(a) Memory, *PC*, and *AR* at time T_4 (b) Memory and *PC* after execution

ISZ : Increment and Skip if Zero

D_6T_4 : $DR \leftarrow M[AR]$

D_6T_5 : $DR \leftarrow DR + 1$

D_6T_6 : $M[AR] \leftarrow DR$,
if (DR is 0) then $PC \leftarrow PC + 1$,
$SC \leftarrow 0$

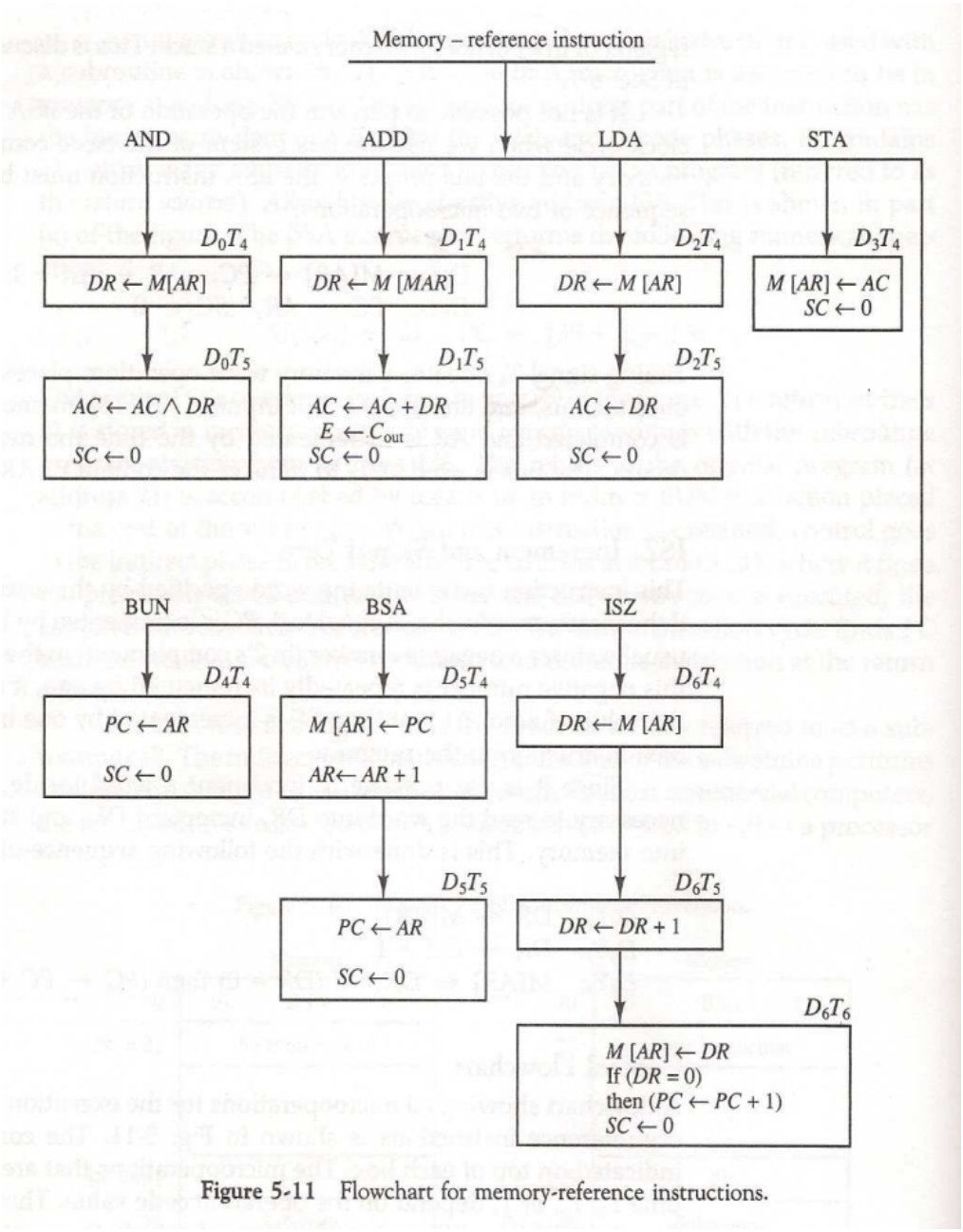


Figure 5-11 Flowchart for memory-reference instructions.