CSE206

Digital Logic Design Sessional

Offline 2

Comparator, Adder / Subtractor

Bangladesh University of Engineering & Technology

Group: 02

Section: B2

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Level - 2, Term - 1

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Question NO :1

Problem specification :

We have to design using basic gates, a 2-bit comparator to compare 2-bit numbers P and Q. The circuit should provide 3 output lines to indicate P>Q, P=Q and P<Q.

Required Instruments:

1. NOT Gate (IC 7404)
2. AND Gate (IC 7408)
3. OR Gate (IC 7432)
4. Wires
5. Power source etc.

Truth Table :

Truth table for a 2-bit comparator to compare 2-bit numbers shown below :

P		Q		Output (Binary Code)		
P_1	P_0	Q_1	Q_0	L(P<Q)	E(P=Q)	G(P>Q)
0	0	0	0	0	1	0
0	0	0	1	1	0	0
0	0	1	0	1	0	0
0	0	1	1	1	0	0
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	0	1	0
1	0	1	1	1	0	0
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	0	1	0

Required Equations:

E Function:
P = Q, only when **P1 = Q1** and **P0 = Q0**
E = f(P = Q) = x_0x_1
x_0 = $\bar{P}_0\bar{Q}_0 + P_0Q_0$ [**x_0** is true when the LSB are same]
x_1 = $\bar{P}_1\bar{Q}_1 + P_1Q_1$ [**x_1** is true when the MSB are same]

G Function:
We can observe that, **P > Q** in either of two cases

- **P1 > Q1**
- **P1 = Q1** and **P0 > Q0**

So,
G = f(P > Q) = $P_1\bar{Q}_1 + x_1P_0\bar{Q}_0$
x_1 = $\bar{P}_1\bar{Q}_1 + P_1Q_1$ [**x_1** is true when the MSB are same]

L function:
We can observe that, **P < Q** in either of two cases

- **P1 < Q1**
- **P1 = Q1 and P0 < Q0**

So,
L= **f(P < Q) = $\bar{P}_1Q_1 + x_1\bar{P}_0Q_0$**
x_1 = **$\bar{P}_1\bar{Q}_1 + P_1Q_1$** [**$x_1$** is true when the MSB are same]

Circuit Diagram:

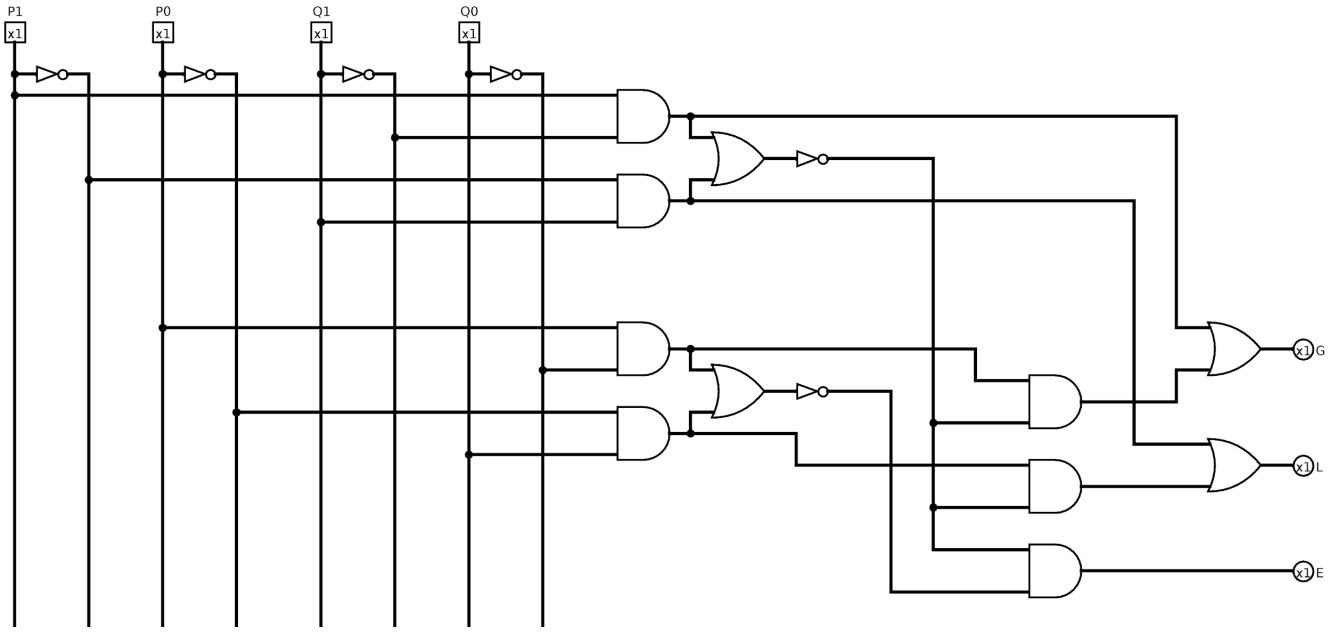

Fig: Logic Circuit Diagram for 2-bit Comparator

Question No: 2

Problem Specification:

We are required to design a 1-bit full subtractor circuit using basic logic gates. The inputs are **D** (minuend), **E** (subtrahend), **F** (Previous Borrow) and the outputs are **R** (Difference), **B** (Output Borrow).

Required Instruments:

1. NOT Gate (IC 7404) – Quantity: X
2. AND Gate (IC 7408) – Quantity: X
3. OR Gate (IC 7432) – Quantity: X
4. Input pins – Quantity: 3
5. Output pins – Quantity: 2
6. Wires, power source etc.

Truth Table:

Input			Output	
D	**E**	**F**	**R**	**B**
0	**0**	**0**	**0**	**0**
0	**0**	**1**	**1**	**1**
0	**1**	**0**	**1**	**1**
0	**1**	**1**	**0**	**1**
1	**0**	**0**	**1**	**0**
1	**0**	**1**	**0**	**0**
1	**1**	**0**	**0**	**0**
1	**1**	**1**	**1**	**1**

K-map for **R**:

		00	01	11	10
		E'F'	**E'F**	**EF**	**EF'**
0	**D'**	**0**	**1**	**0**	**1**
1	**D**	**1**	**0**	**1**	**0**

From the K-map,

R = DE'F'+D'E'F+DEF+D'EF'
= DEF+D'E'F+D'EF'+DE'F' [***Commutative Law***]
= (DE+D'E')F+(D'E+DE')F' [***Distributive Law***]
= (D XNOR E)F+(D XOR F)F' [***A'B+AB'=A XOR B and AB+A'B'= A XNOR B***]
= (D XOR E)'F+(D XOR E)F' [***A XNOR B = (A XOR B)'***]
= (D XOR E) XOR F

K-map for **B**:

		00	01	11	10
		E'F'	**E'F**	**EF**	**EF'**
0	**D'**	**0**	**1**	**1**	**1**
1	**D**	**0**	**0**	**1**	**0**

From the K-map,

B = D'F+D'E+EF

= D'E+D'F+EF [*Distributive Law*]

<u>Circuit Diagram</u>:

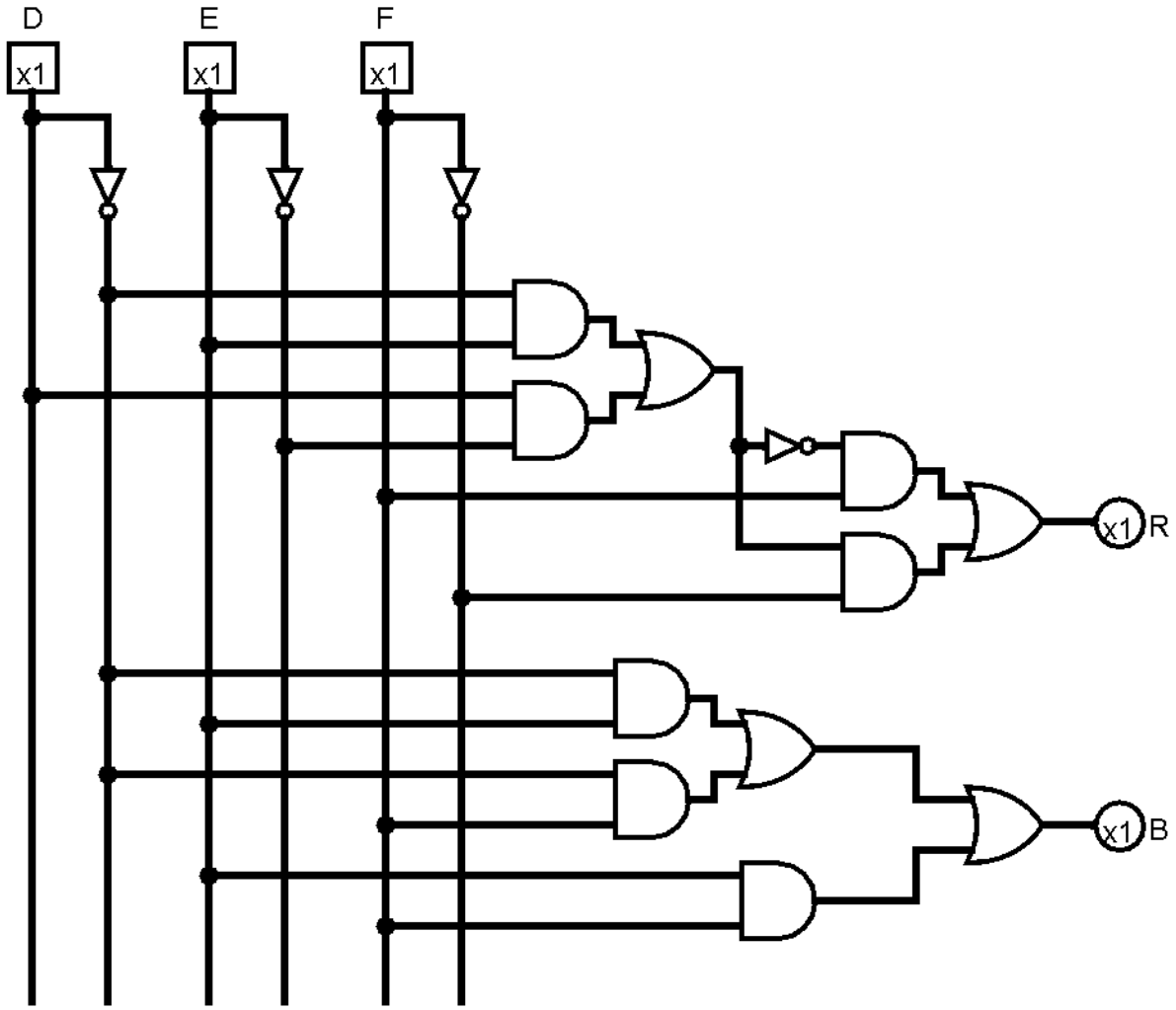

Fig: Logic Circuit Diagram for 1-bit Subtractor