Bangladesh University of Engineering and Technology

Department of Computer Science and Engineering

Sections: A2 & B2

Course: CSE 206
Title: Digital Logic Design Sessional

Experiment No. 4
Topic: Comparator, adder / subtractor

Implement the following problems:

1. Design using basic gates, a 2-bit comparator to compare 2-bit numbers P and Q. The circuit should provide 3 output lines to indicate P>Q, P=Q and P<Q.
2. Design a 1-bit full sub tractor circuit using basic logic gates. Inputs are D, E and F denoting minuend, subtrahend and previous borrow respectively. The outputs are R and B representing the difference and output borrow.

Report:
For each of the problems, prepare report as follows:

a. Required instruments, ICs, software etc.
b. Truth table
c. Required equation in minimized form showing necessary steps
d. Circuit diagram.