## **Bangladesh University of Engineering and Technology**

Department of Computer Science and Engineering

Sections: A1 & B1

Course: CSE 206

Title: Digital Logic Design Sessional

Experiment No. 4

Topic: Comparator, adder / subtractor

## **Implement the following problems:**

- 1. Design using basic gates, a 2-bit comparator to compare 2-bit numbers X and Y. The circuit should provide 3 output lines to indicate X>Y, X=Y and X<Y.
- 2. Design a 1-bit full sub tractor circuit using basic logic gates. Inputs are P, Q and R denoting minuend, subtrahend and previous borrow respectively. The outputs are D and B representing the difference and output borrow.

## Report:

For each of the problems, prepare report as follows:

- a. Required instruments, ICs, software etc.
- b. Truth table
- c. Required equation in minimized form showing necessary steps
- d. Circuit diagram.