Quantum supremacy using a programmable superconducting processor

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The tantalizing promise of quantum computers is that certain computational tasks might be executed exponentially faster on a quantum processor than on a classical processor. A fundamental challenge is to build a high-fidelity processor capable of running quantum algorithms in an exponentially large computational space. Here, we report using a processor with programmable superconducting qubits to create quantum states on 53 qubits, occupying a state space $2^{53} \sim 10^{16}$. Measurements from repeated experiments sample the corresponding probability distribution, which we verify using classical simulations. While our processor takes about 200 seconds to sample one instance of the quantum circuit 1 million times, a state-of-the-art supercomputer would require approximately 10,000 years to perform the equivalent task. This dramatic speedup relative to all known classical algorithms provides an experimental realization of quantum supremacy on a computational task and heralds the advent of a much-anticipated computing paradigm.

In the early 1980s, Richard Feynman proposed that a quantum computer would be an effective tool to solve problems in physics and chemistry, as it is exponentially costly to simulate large quantum systems with classical computers [1]. Realizing Feynman's vision poses significant experimental and theoretical challenges. First, can a quantum system be engineered to perform a computation in a large enough computational (Hilbert) space and with low enough errors to provide a quantum speedup? Second, can we formulate a problem that is hard for a classical computer but easy for a quantum computer? By computing a novel benchmark task on our superconducting qubit processor [2–7], we tackle both questions. Our experiment marks a milestone towards full scale quantum computing: quantum supremacy [8].

In reaching this milestone, we show that quantum speedup is achievable in a real-world system and is not precluded by any hidden physical laws. Quantum supremacy also heralds the era of Noisy Intermediate-Scale Quantum (NISQ) technologies. The benchmark task we demonstrate has an immediate application in generating certifiable random numbers [9]; other initial uses for this new computational capability may include optimization optimization [10–12], machine learning [13–15], materials science and chemistry [16–18]. However, realizing the full promise of quantum computing (e.g. Shor's algorithm for factoring) still requires technical leaps to engineer fault-tolerant logical qubits [19–23].

To achieve quantum supremacy, we made a number of technical advances which also pave the way towards error correction. We developed fast, high-fidelity gates that can be executed simultaneously across a two-dimensional qubit array. We calibrated and benchmarked the processor at both the component and system level using a powerful new tool: cross-entropy benchmarking (XEB). Finally, we used component-level fidelities to accurately predict the performance of the whole system, further showing that quantum information behaves as expected when scaling to large systems.

A COMPUTATIONAL TASK TO DEMONSTRATE QUANTUM SUPREMACY

To demonstrate quantum supremacy, we compare our quantum processor against state-of-the-art classical computers in the task of sampling the output of a pseudo-random quantum circuit [24–26]. Random circuits are a suitable choice for benchmarking since they do not possess structure and therefore allow for limited guarantees of computational hardness [24, 25, 27, 28]. We design the circuits to entangle a set of quantum bits (qubits) by repeated application of single-qubit and two-qubit logical operations. Sampling the quantum circuit's output produces a set of bitstrings, e.g. $\{0000101, 1011100, \dots\}$. Due to quantum interference, the probability distribution of the bitstrings resembles a speckled intensity pattern produced by light interference in laser scatter, such that some bitstrings are much more likely to occur than others. Classically computing this probability distribution becomes exponentially more difficult as the number of qubits (width) and number of gate cycles (depth) grows.

We verify that the quantum processor is working properly using a method called cross-entropy benchmarking (XEB) [24, 26], which compares how often each bitstring is observed experimentally with its corresponding ideal probability computed via simulation on a classical computer. For a given circuit, we collect the measured bitstrings $\{x_i\}$ and compute the linear XEB fidelity [24–26, 29], which is the mean of the simulated probabilities of the bitstrings we measured:

$$\mathcal{F}_{\mathrm{XEB}} = 2^n \langle P(x_i) \rangle_i - 1 \tag{1}$$

where n is the number of qubits, $P(x_i)$ is the probability of bitstring x_i computed for the ideal quantum circuit, and the average is over the observed bitstrings. Intuitively, $\mathcal{F}_{\mathrm{XEB}}$ is correlated with how often we sample high probability bitstrings. When there are no errors in the quantum circuit, sampling the probability distribution will produce $\mathcal{F}_{\mathrm{XEB}} = 1$. On the other hand, sampling from the uniform distribution will give $\langle P(x_i) \rangle_i = 1/2^n$ and produce $\mathcal{F}_{\mathrm{XEB}} = 0$. Values of $\mathcal{F}_{\mathrm{XEB}}$ between 0 and
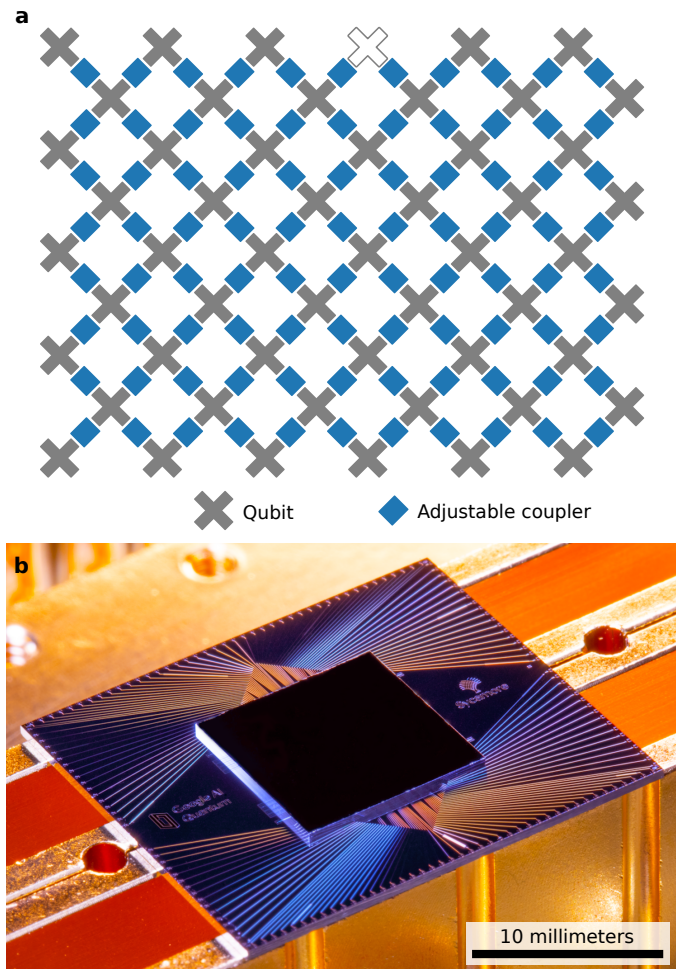
FIG. 1. **The Sycamore processor. a,** Layout of processor showing a rectangular array of 54 qubits (gray), each connected to its four nearest neighbors with couplers (blue). Inoperable qubit is outlined. **b,** Optical image of the Sycamore chip.

BUILDING AND CHARACTERIZING A HIGH-FIDELITY PROCESSOR

We designed a quantum processor named "Sycamore" which consists of a two-dimensional array of 54 transmon qubits, where each qubit is tunably coupled to four nearest-neighbors, in a rectangular lattice. The connectivity was chosen to be forward compatible with error-correction using the surface code [20]. A key systems-engineering advance of this device is achieving high-fidelity single- and two-qubit operations, not just in isolation but also while performing a realistic computation with simultaneous gate operations on many qubits. We discuss the highlights below; extended details can be found in the supplementary information.

In a superconducting circuit, conduction electrons condense into a macroscopic quantum state, such that currents and voltages behave quantum mechanically [2, 30]. Our processor uses transmon qubits [6], which can be thought of as nonlinear superconducting resonators at 5 to 7 GHz. The qubit is encoded as the two lowest quantum eigenstates of the resonant circuit. Each transmon has two controls: a microwave drive to excite the qubit, and a magnetic flux control to tune the frequency. Each qubit is connected to a linear resonator used to read out the qubit state [5]. As shown in Fig. 1, each qubit is also connected to its neighboring qubits using a new adjustable coupler [31, 32]. Our coupler design allows us to quickly tune the qubit-qubit coupling from completely off to 40 MHz. Since one qubit did not function properly the device uses 53 qubits and 86 couplers.

The processor is fabricated using aluminum for metalization and Josephson junctions, and indium for bump-bonds between two silicon wafers. The chip is wire-bonded to a superconducting circuit board and cooled to below 20 mK in a dilution refrigerator to reduce ambient thermal energy to well below the qubit energy. The processor is connected through filters and attenuators to room-temperature electronics, which synthesize the control signals. The state of all qubits can be read simultaneously by using a frequency-multiplexing technique [33, 34]. We use two stages of cryogenic amplifiers to boost the signal, which is digitized (8 bits at 1 GS/s) and demultiplexed digitally at room temperature. In total, we orchestrate 277 digital-to-analog converters (14 bits at 1 GS/s) for complete control of the quantum processor.

We execute single-qubit gates by driving 25 ns microwave pulses resonant with the qubit frequency while the qubit-qubit coupling is turned off. The pulses are shaped to minimize transitions to higher transmon states [35]. Gate performance varies strongly with frequency due to two-level-system (TLS) defects [36, 37], stray microwave modes, coupling to control lines and the readout resonator, residual stray coupling between qubits, flux noise, and pulse distortions. We therefore
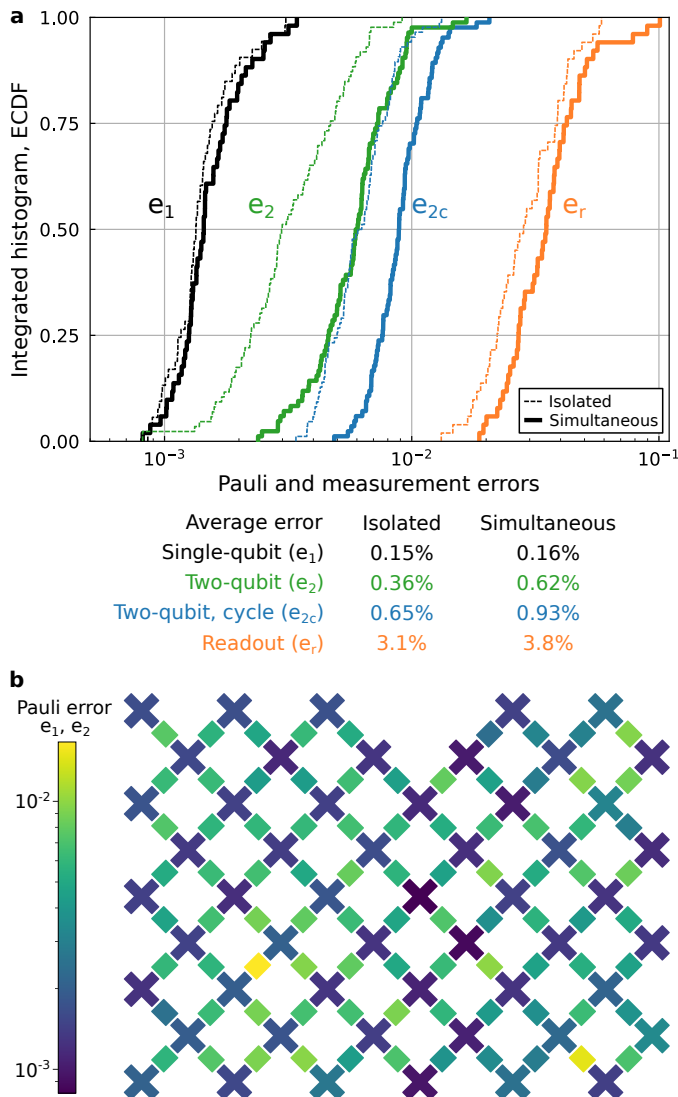
1 correspond to the probability that no error has occurred while running the circuit. The probabilities $P(x_i)$ must be obtained from classically simulating the quantum circuit, and thus computing $\mathcal{F}_{\text{XEB}}$ is intractable in the regime of quantum supremacy. However, with certain circuit simplifications, we can obtain quantitative fidelity estimates of a fully operating processor running wide and deep quantum circuits.

Our goal is to achieve a high enough $\mathcal{F}_{\text{XEB}}$ for a circuit with sufficient width and depth such that the classical computing cost is prohibitively large. This is a difficult task because our logic gates are imperfect and the quantum states we intend to create are sensitive to errors. A single bit or phase flip over the course of the algorithm will completely shuffle the speckle pattern and result in close to 0 fidelity [24, 29]. Therefore, in order to claim quantum supremacy we need a quantum processor that executes the program with sufficiently low error rates.

FIG. 2. **System-wide Pauli and measurement errors. a,** Integrated histogram (empirical cumulative distribution function, ECDF) of Pauli errors (black, green, blue) and readout errors (orange), measured on qubits in isolation (dotted lines) and when operating all qubits simultaneously (solid). The median of each distribution occurs at 0.50 on the vertical axis. Average (mean) values are shown below. **b,** Heatmap showing single- and two-qubit Pauli errors e_1 (crosses) and e_2 (bars) positioned in the layout of the processor. Values shown for all qubits operating simultaneously.

optimize the single-qubit operation frequencies to mitigate these error mechanisms.

We benchmark single-qubit gate performance by using the XEB protocol described above, reduced to the single-qubit level ($n = 1$), to measure the probability of an error occurring during a single-qubit gate. On each qubit, we apply a variable number m of randomly selected gates and measure $\mathcal{F}_{\text{XEB}}$ averaged over many sequences; as m increases, errors accumulate and average $\mathcal{F}_{\text{XEB}}$ decays.

We model this decay by $[1 - e_1/(1 - 1/D^2)]^m$ where e_1 is the Pauli error probability. The state (Hilbert) space dimension term, $D = 2^n = 2$, corrects for the depolarizing model where states with errors partially overlap with the ideal state. This procedure is similar to the more typical technique of randomized benchmarking [21, 38, 39], but supports non-Clifford gatesets [40] and can separate out decoherence error from coherent control error. We then repeat the experiment with all qubits executing single-qubit gates simultaneously (Fig. 2), which shows only a small increase in the error probabilities, demonstrating that our device has low microwave crosstalk.

We perform two-qubit iSWAP-like entangling gates by bringing neighboring qubits on resonance and turning on a 20 MHz coupling for 12 ns, which allows the qubits to swap excitations. During this time, the qubits also experience a controlled-phase (CZ) interaction, which originates from the higher levels of the transmon. The two-qubit gate frequency trajectories of each pair of qubits are optimized to mitigate the same error mechanisms considered in optimizing single-qubit operation frequencies.

To characterize and benchmark the two-qubit gates, we run two-qubit circuits with m cycles, where each cycle contains a randomly chosen single-qubit gate on each of the two qubits followed by a fixed two-qubit gate. We learn the parameters of the two-qubit unitary (e.g. the amount of iSWAP and CZ interaction) by using $\mathcal{F}_{\text{XEB}}$ as a cost function. After this optimization, we extract the per-cycle error e_{2c} from the decay of $\mathcal{F}_{\text{XEB}}$ with m, and isolate the two-qubit error e_2 by subtracting the two single-qubit errors e_1. We find an average e_2 of 0.36%. Additionally, we repeat the same procedure while simultaneously running two-qubit circuits for the entire array. After updating the unitary parameters to account for effects such as dispersive shifts and crosstalk, we find an average e_2 of 0.62%.

For the full experiment, we generate quantum circuits using the two-qubit unitaries measured for each pair during simultaneous operation, rather than a standard gate for all pairs. The typical two-qubit gate is a full iSWAP with $1/6$ of a full CZ. In principle, our architecture could generate unitaries with arbitrary iSWAP and CZ interactions, but reliably generating a target unitary remains an active area of research.

Finally, we benchmark qubit readout using standard dispersive measurement [41]. Measurement errors averaged over the 0 and 1 states are shown in Fig 2a. We have also measured the error when operating all qubits simultaneously, by randomly preparing each qubit in the 0 or 1 state and then measuring all qubits for the probability of the correct result. We find that simultaneous readout incurs only a modest increase in per-qubit measurement errors.

Having found the error rates of the individual gates and readout, we can model the fidelity of a quantum circuit as the product of the probabilities of error-free opera-
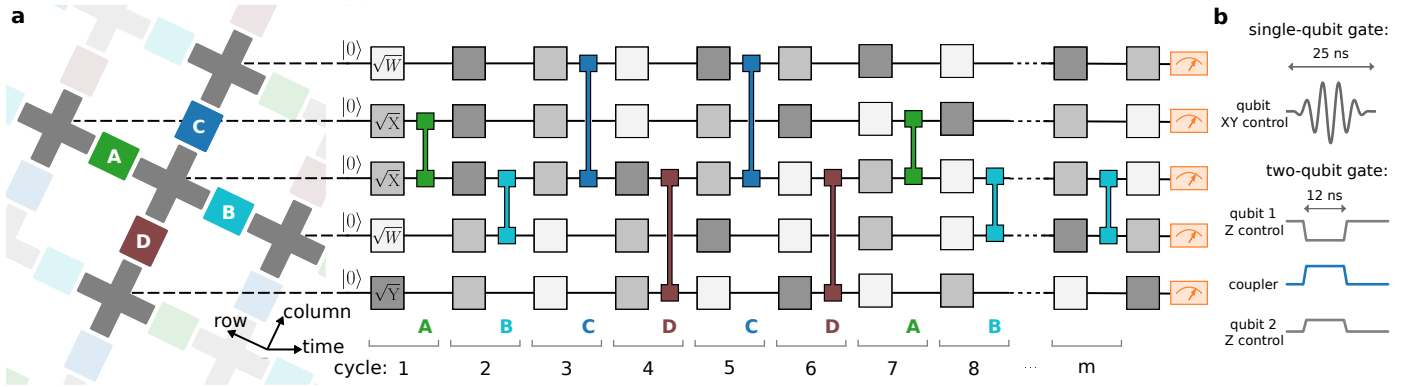
FIG. 3. **Control operations for the quantum supremacy circuits. a,** Example quantum circuit instance used in our experiment. Every cycle includes a layer each of single- and two-qubit gates. The single-qubit gates are chosen randomly from $\{\sqrt{X}, \sqrt{Y}, \sqrt{W}\}$. The sequence of two-qubit gates are chosen according to a tiling pattern, coupling each qubit sequentially to its four nearest-neighbor qubits. The couplers are divided into four subsets (ABCD), each of which is executed simultaneously across the entire array corresponding to shaded colors. Here we show an intractable sequence (repeat ABCDCDAB); we also use different coupler subsets along with a simplifiable sequence (repeat EFGHEFGH, not shown) that can be simulated on a classical computer. **b,** Waveform of control signals for single- and two-qubit gates.

tion of all gates and measurements. Our largest random quantum circuits have 53 qubits, 1113 single-qubit gates, 430 two-qubit gates, and a measurement on each qubit, for which we predict a total fidelity of 0.2%. This fidelity should be resolvable with a few million measurements, since the uncertainty on $\mathcal{F}_{\mathrm{XEB}}$ is $1/\sqrt{N_s}$, where N_s is the number of samples. Our model assumes that entangling larger and larger systems does not introduce additional error sources beyond the errors we measure at the single- and two-qubit level — in the next section we will see how well this hypothesis holds.

FIDELITY ESTIMATION IN THE SUPREMACY REGIME

The gate sequence for our pseudo-random quantum circuit generation is shown in Fig. 3. One cycle of the algorithm consists of applying single-qubit gates chosen randomly from $\{\sqrt{X}, \sqrt{Y}, \sqrt{W}\}$ on all qubits, followed by two-qubit gates on pairs of qubits. The sequences of gates which form the "supremacy circuits" are designed to minimize the circuit depth required to create a highly entangled state, which ensures computational complexity and classical hardness.

While we cannot compute $\mathcal{F}_{\mathrm{XEB}}$ in the supremacy regime, we can estimate it using three variations to reduce the complexity of the circuits. In "patch circuits", we remove a slice of two-qubit gates (a small fraction of the total number of two-qubit gates), splitting the circuit into two spatially isolated, non-interacting patches of qubits. We then compute the total fidelity as the product of the patch fidelities, each of which can be easily calculated. In "elided circuits", we remove only a fraction of the initial two-qubit gates along the slice, allowing for entanglement between patches, which more closely mimics the full experiment while still maintaining simulation

feasibility. Finally, we can also run full "verification circuits" with the same gate counts as our supremacy circuits, but with a different pattern for the sequence of two-qubit gates which is much easier to simulate classically [29]. Comparison between these variations allows tracking of the system fidelity as we approach the supremacy regime.

We first check that the patch and elided versions of the verification circuits produce the same fidelity as the full verification circuits up to 53 qubits, as shown in Fig. 4a. For each data point, we typically collect $N_s = 5 \times 10^6$ total samples over ten circuit instances, where instances differ only in the choices of single-qubit gates in each cycle. We also show predicted $\mathcal{F}_{\mathrm{XEB}}$ values computed by multiplying the no-error probabilities of single- and two-qubit gates and measurement [29]. Patch, elided, and predicted fidelities all show good agreement with the fidelities of the corresponding full circuits, despite the vast differences in computational complexity and entanglement. This gives us confidence that elided circuits can be used to accurately estimate the fidelity of more complex circuits.

We proceed now to benchmark our most computationally difficult circuits. In Fig. 4b, we show the measured $\mathcal{F}_{\mathrm{XEB}}$ for 53-qubit patch and elided versions of the full supremacy circuits with increasing depth. For the largest circuit with 53 qubits and 20 cycles, we collected $N_s = 30 \times 10^6$ samples over 10 circuit instances, obtaining $\mathcal{F}_{\mathrm{XEB}} = (2.24 \pm 0.21) \times 10^{-3}$ for the elided circuits. With 5σ confidence, we assert that the average fidelity of running these circuits on the quantum processor is greater than at least 0.1%. The full data for Fig. 4b should have similar fidelities, but are only archived since the simulation times (red numbers) take too long. It is thus in the quantum supremacy regime.
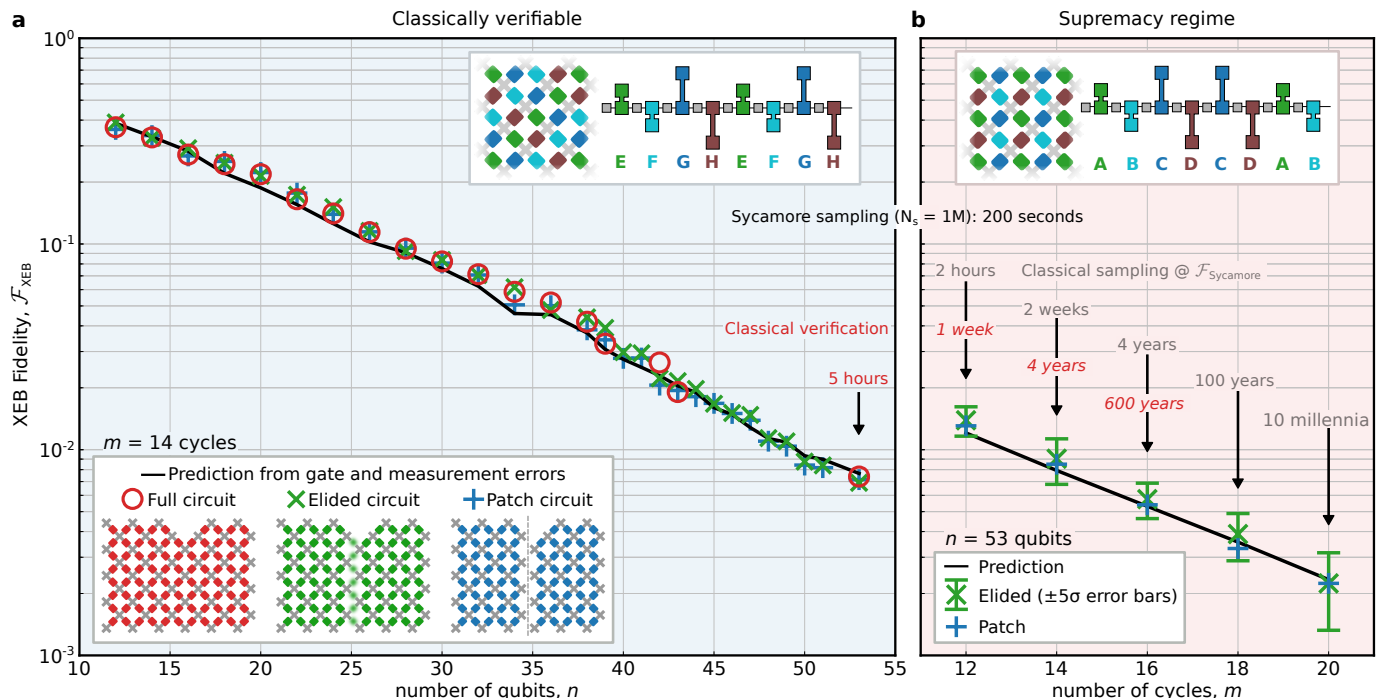
FIG. 4. **Demonstrating quantum supremacy**. **a,** Verification of benchmarking methods. $\mathcal{F}_{\mathrm{XEB}}$ values for patch, elided, and full verification circuits are calculated from measured bitstrings and the corresponding probabilities predicted by classical simulation. Here, the two-qubit gates are applied in a simplifiable tiling and sequence such that the full circuits can be simulated out to $n = 53$, $m = 14$ in a reasonable amount of time. Each data point is an average over 10 distinct quantum circuit instances that differ in their single-qubit gates (for $n = 39, 42, 43$ only 2 instances were simulated). For each n, each instance is sampled with N_s between 0.5 M and 2.5 M. The black line shows predicted $\mathcal{F}_{\mathrm{XEB}}$ based on single- and two-qubit gate and measurement errors. The close correspondence between all four curves, despite their vast differences in complexity, justifies the use of elided circuits to estimate fidelity in the supremacy regime. **b,** Estimating $\mathcal{F}_{\mathrm{XEB}}$ in the quantum supremacy regime. Here, the two-qubit gates are applied in a non-simplifiable tiling and sequence for which it is much harder to simulate. For the largest elided data ($n = 53$, $m = 20$, total $N_s = 30$ M), we find an average $\mathcal{F}_{\mathrm{XEB}} > 0.1\%$ with 5σ confidence, where σ includes both systematic and statistical uncertainties. The corresponding full circuit data, not simulated but archived, is expected to show similarly significant fidelity. For $m = 20$, obtaining 1M samples on the quantum processor takes 200 seconds, while an equal fidelity classical sampling would take 10,000 years on 1M cores, and verifying the fidelity would take millions of years.

DETERMINING THE CLASSICAL COMPUTATIONAL COST

We simulate the quantum circuits used in the experiment on classical computers for two purposes: verifying our quantum processor and benchmarking methods by computing $\mathcal{F}_{\mathrm{XEB}}$ where possible using simplifiable circuits (Fig. 4a), and estimating $\mathcal{F}_{\mathrm{XEB}}$ as well as the classical cost of sampling our hardest circuits (Fig. 4b). Up to 43 qubits, we use a Schrödinger algorithm (SA) which simulates the evolution of the full quantum state; the Jülich supercomputer (100k cores, 250TB) runs the largest cases. Above this size, there is not enough RAM to store the quantum state [42]. For larger qubit numbers, we use a hybrid Schrödinger-Feynman algorithm (SFA) [43] running on Google data centers to compute the amplitudes of individual bitstrings. This algorithm breaks the circuit up into two patches of qubits and efficiently simulates each patch using a Schrödinger method, before connecting them using an approach reminiscent of

the Feynman path-integral. While it is more memory-efficient, SFA becomes exponentially more computation-ally expensive with increasing circuit depth due to the exponential growth of paths with the number of gates connecting the patches.

To estimate the classical computational cost of the supremacy circuits (gray numbers, Fig. 4b), we ran portions of the quantum circuit simulation on both the Summit supercomputer as well as on Google clusters and extrapolated to the full cost. In this extrapolation, we account for the computational cost scaling with $\mathcal{F}_{\mathrm{XEB}}$, e.g. the 0.1% fidelity decreases the cost by 1000 [43, 44]. On the Summit supercomputer, which is currently the most powerful in the world, we used a method inspired by Feynman path-integrals that is most efficient at low depth [44–47]. At $m = 20$ the tensors do not reasonably fit in node memory, so we can only measure runtimes up to $m = 14$, for which we estimate that sampling 3M bitstrings with 1% fidelity would require 1 year.

On Google Cloud servers, we estimate that performing the same task for $m = 20$ with 0.1% fidelity using the SFA algorithm would cost 50 trillion core-hours and consume 1 petawatt hour of energy. To put this in perspective, it took 600 seconds to sample the circuit on the quantum processor 3 million times, where sampling time is limited by control hardware communications; in fact, the net quantum processor time is only about 30 seconds. The bitstring samples from this largest circuit are archived online.

One may wonder to what extent algorithmic innovation can enhance classical simulations. Our assumption, based on insights from complexity theory, is that the cost of this algorithmic task is exponential in n as well as m. Indeed, simulation methods have improved steadily over the past few years [42–50]. We expect that lower simulation costs than reported here will eventually be achieved, but we also expect they will be consistently outpaced by hardware improvements on larger quantum processors.

VERIFYING THE DIGITAL ERROR MODEL

A key assumption underlying the theory of quantum error correction is that quantum state errors may be considered digitized and localized [38, 51]. Under such a digital model, all errors in the evolving quantum state may be characterized by a set of localized Pauli errors (bit- and/or phase-flips) interspersed into the circuit. Since continuous amplitudes are fundamental to quantum mechanics, it needs to be tested whether errors in a quantum system could be treated as discrete and probabilistic. Indeed, our experimental observations support the validity of this model for our processor. Our system fidelity is well predicted by a simple model in which the individually characterized fidelities of each gate are multiplied together (Fig 4).

To be successfully described by a digitized error model, a system should be low in correlated errors. We achieve this in our experiment by choosing circuits that randomize and decorrelate errors, by optimizing control to minimize systematic errors and leakage, and by designing gates that operate much faster than correlated noise sources, such as $1/f$ flux noise [37]. Demonstrating a predictive uncorrelated error model up to a Hilbert space of size 2^{53} shows that we can build a system where quantum resources, such as entanglement, are not prohibitively fragile.

WHAT DOES THE FUTURE HOLD?

Quantum processors based on superconducting qubits can now perform computations in a Hilbert space of dimension $2^{53} \approx 9 \times 10^{15}$, beyond the reach of the fastest classical supercomputers available today. To our knowledge, this experiment marks the first computation that can only be performed on a quantum processor. Quantum processors have thus reached the regime of quantum supremacy. We expect their computational power will continue to grow at a double exponential rate: the classical cost of simulating a quantum circuit increases exponentially with computational volume, and hardware improvements will likely follow a quantum-processor equivalent of Moore's law [52, 53], doubling this computational volume every few years. To sustain the double exponential growth rate and to eventually offer the computational volume needed to run well-known quantum algorithms, such as the Shor or Grover algorithms [19, 54], the engineering of quantum error correction will have to become a focus of attention.

The "Extended Church-Turing Thesis" formulated by Bernstein and Vazirani [55] asserts that any "reasonable" model of computation can be efficiently simulated by a Turing machine. Our experiment suggests that a model of computation may now be available that violates this assertion. We have performed random quantum circuit sampling in polynomial time with a physically realized quantum processor (with sufficiently low error rates), yet no efficient method is known to exist for classical computing machinery. As a result of these developments, quantum computing is transitioning from a research topic to a technology that unlocks new computational capabilities. We are only one creative algorithm away from valuable near-term applications.

Author contributions The Google AI Quantum team conceived of the experiment. The applications and algorithms team provided the theoretical foundation and the specifics of the algorithm. The hardware team carried out the experiment and collected the data. The data analysis was done jointly with outside collaborators. All authors wrote and revised the manuscript and supplement.

Competing Interests The authors declare that they have no competing financial interests.

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