VLSI Design

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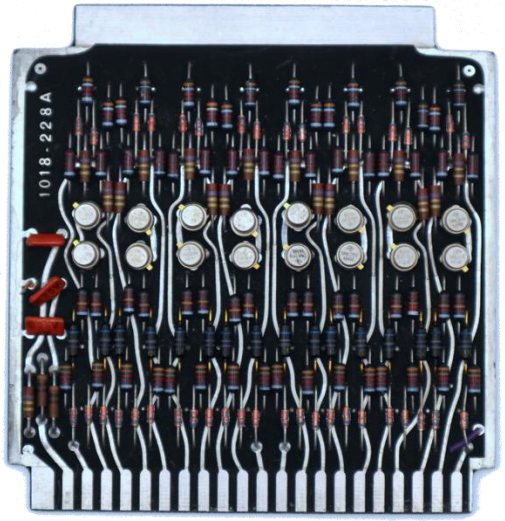
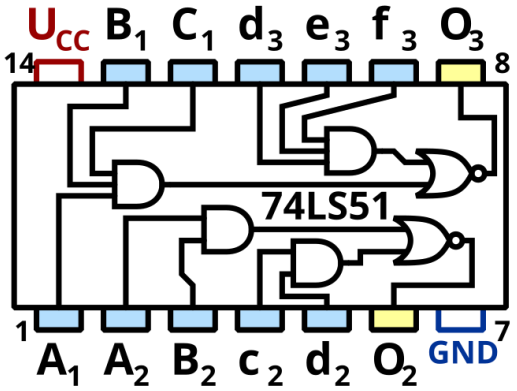
Outline

- Transistor density and scale
- VLSI – Chip Layout and manufacture

Scale Over Time

- Individual transistors connected with other electronics on a "board"
- Integrated circuits with a few transistors or gates



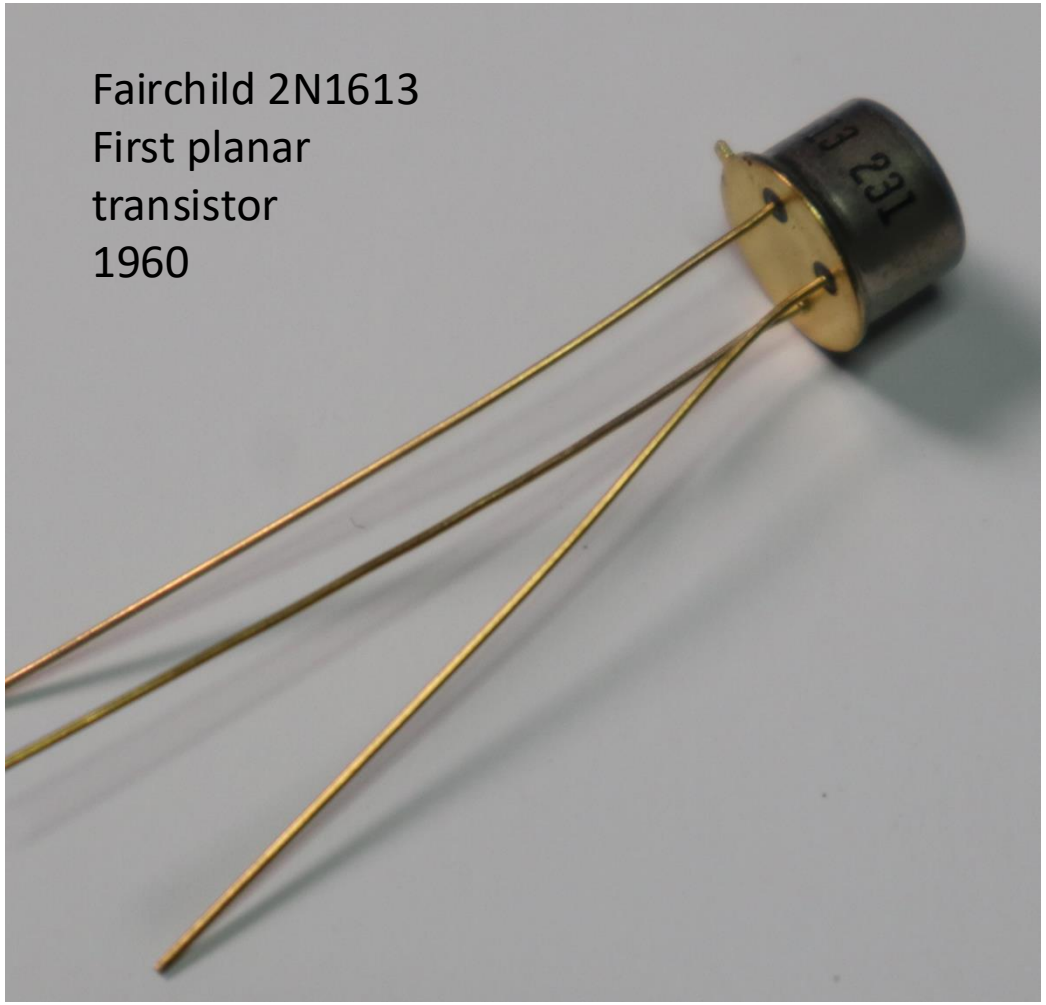


https://en.wikipedia.org/wiki/TO-18
https://en.wikipedia.org/wiki/List_of_7400-series_integrated_circuits

Planar Transistors

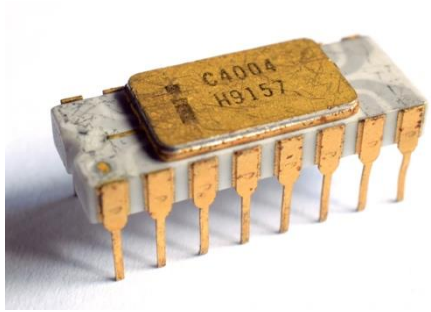
- Prior to 1960, transistor assembly required assembling small crystals and connecting wires to them – they were three dimensional "Lego like" constructions

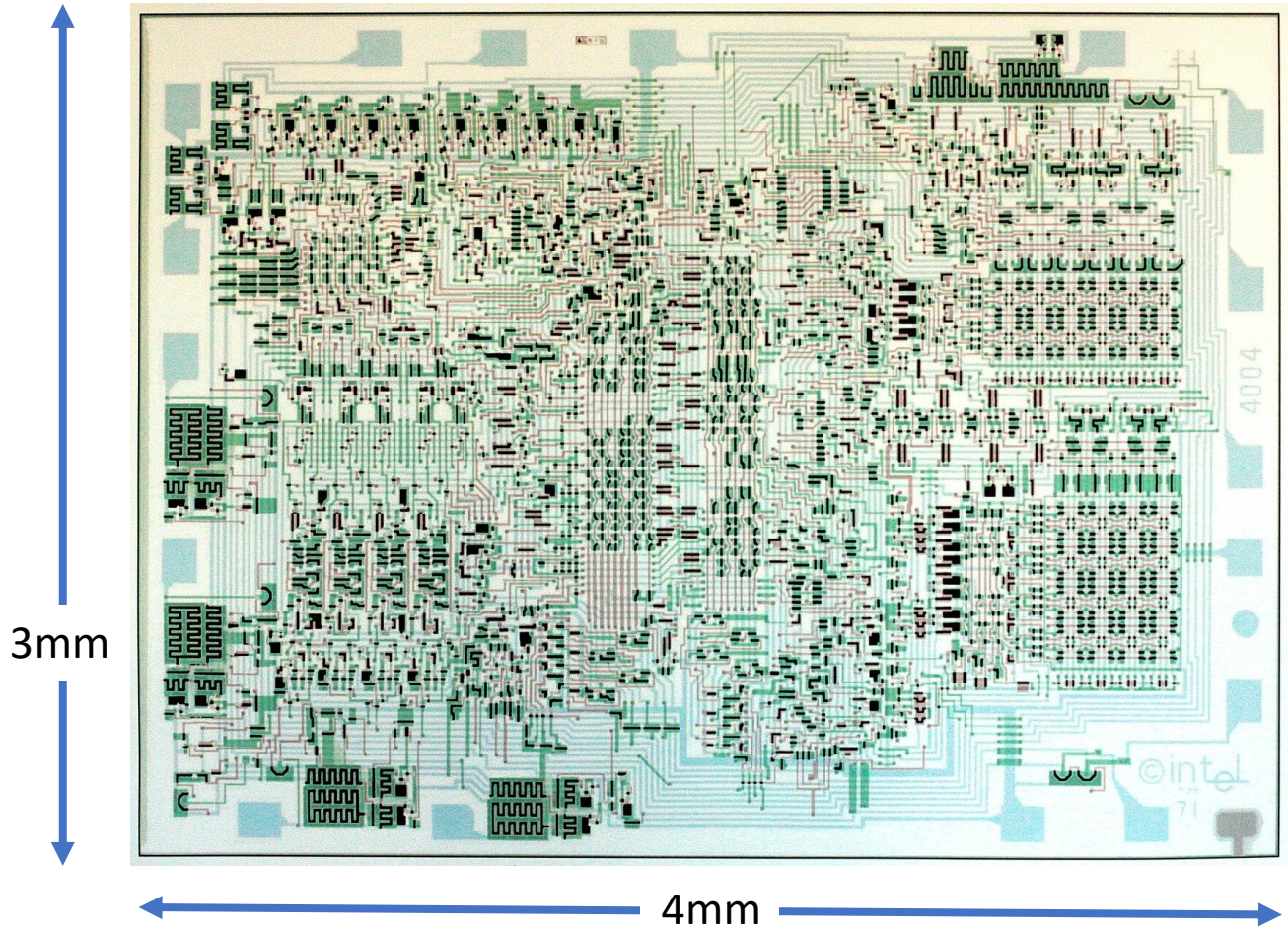
- In 1960 Fairchild introduced the 2N1613 transistor – the first that was manufactured by a two-dimensional process.



Very Large Scale Integration (VLSI)

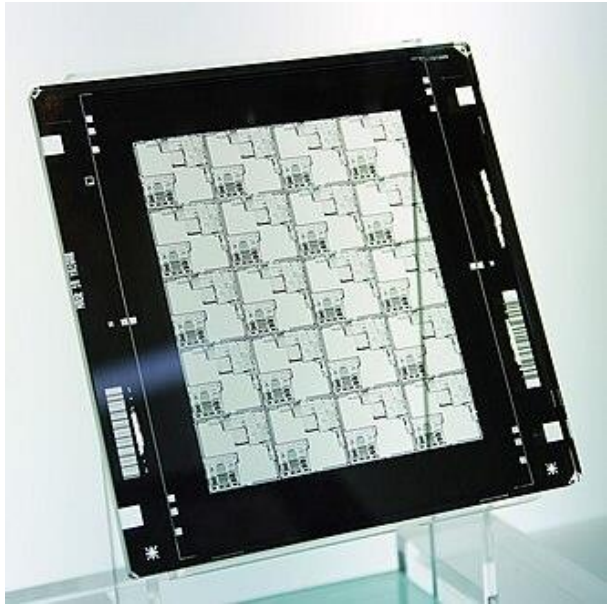
- 2300 PMOS transistors manufactured using photo lithography – 0.01 mm
- The Intel 4004(1971), was the first commercially available single-chip, general-purpose microprocessor

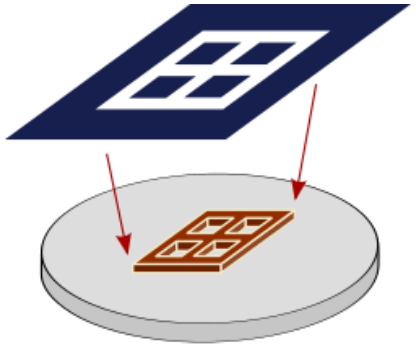




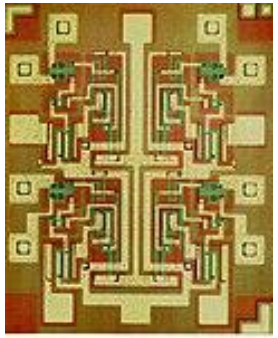
https://en.wikipedia.org/wiki/Intel_4004

Photo Lithography



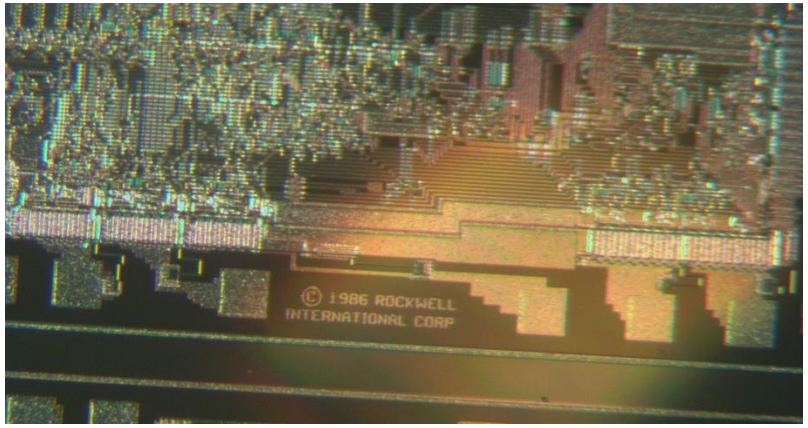


Multiple masks with different chemicals



Four Input NAND
Seven transistors
TI 7420

https://en.wikipedia.org/wiki/Photolithography
https://en.wikipedia.org/wiki/Photomask
https://en.wikipedia.org/wiki/Semiconductor_device_fabrication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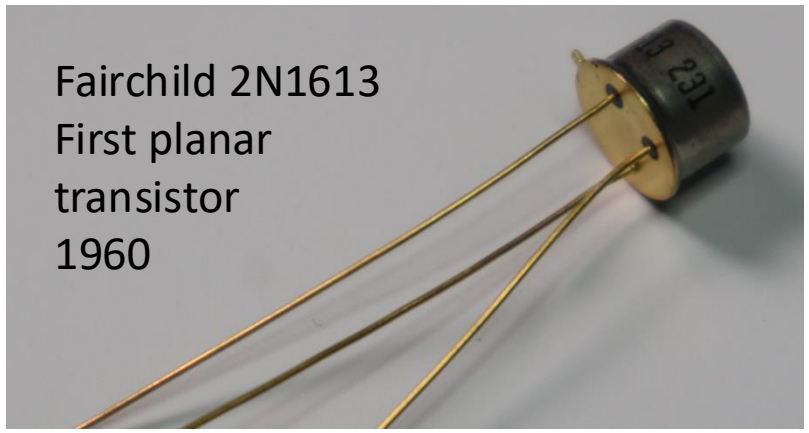
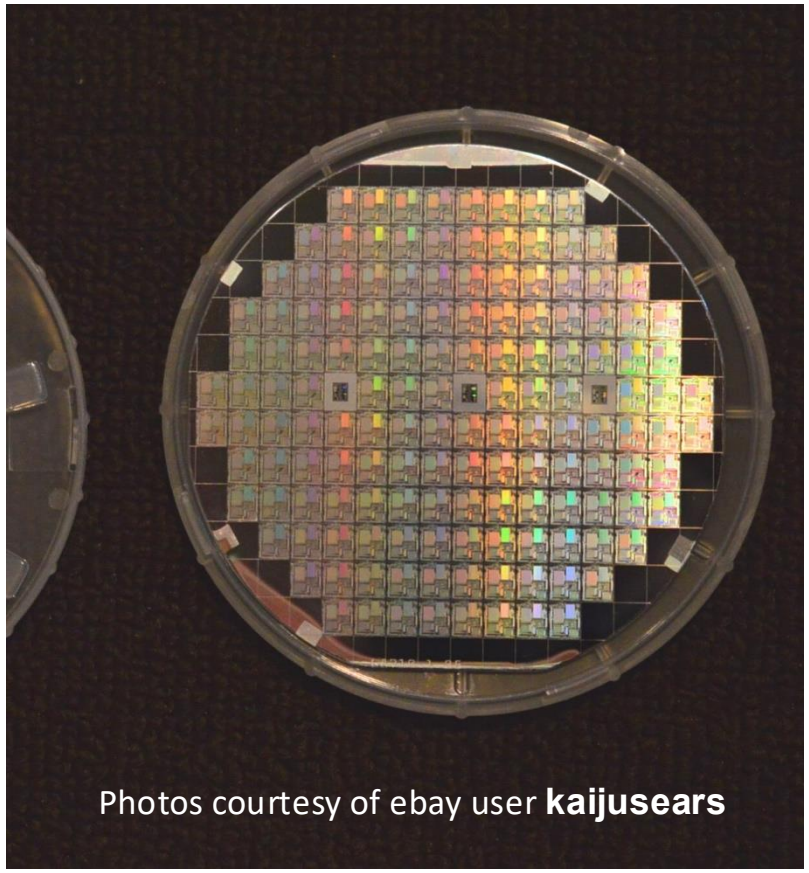
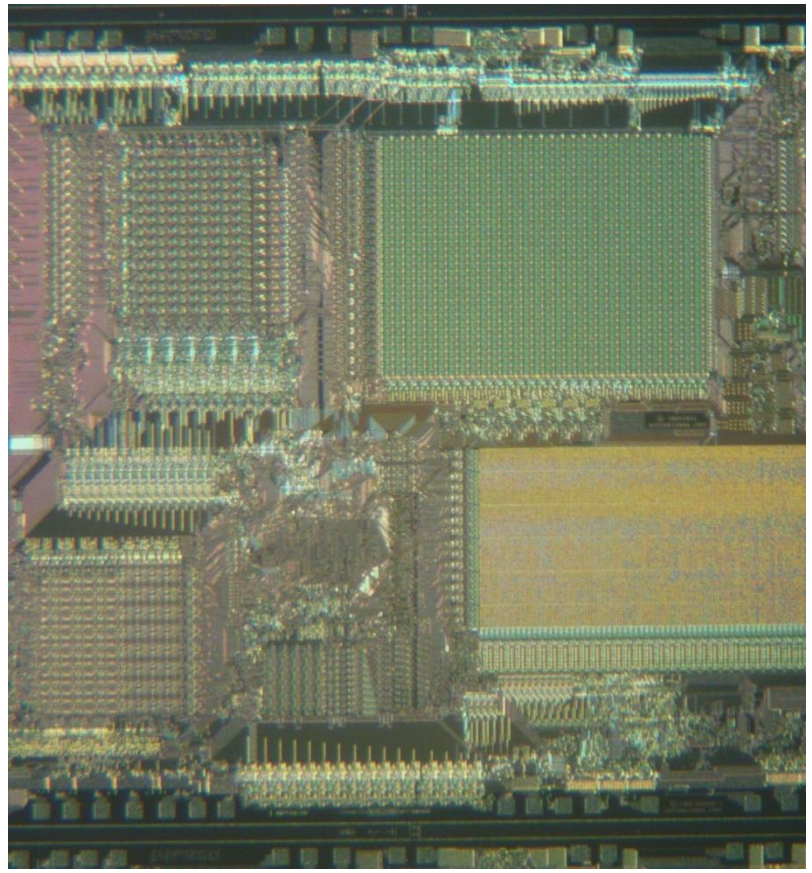
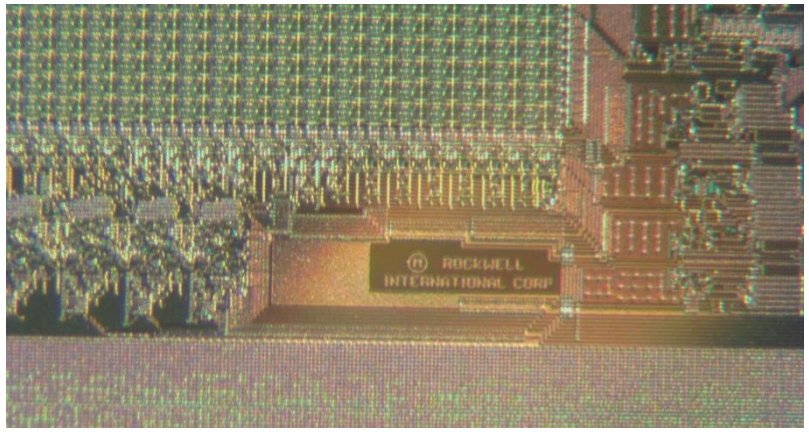

Fairchild 2N1613
First planar
transistor
1960


Photos courtesy of ebay user **kaijusears**

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Growth of transistor count

- The Intel 4004 had 2300 transistors in 1971
- The Intel Itanium was the first billion-transistor chip in 2001
- Nvidia's Blackwell-based B100 GPU with 208 billion MOSFETs in 2024
- Deep learning wafer scale engine by Cerebras has 2.6 trillion MOSFETs 2020

https://en.wikipedia.org/wiki/Transistor_count

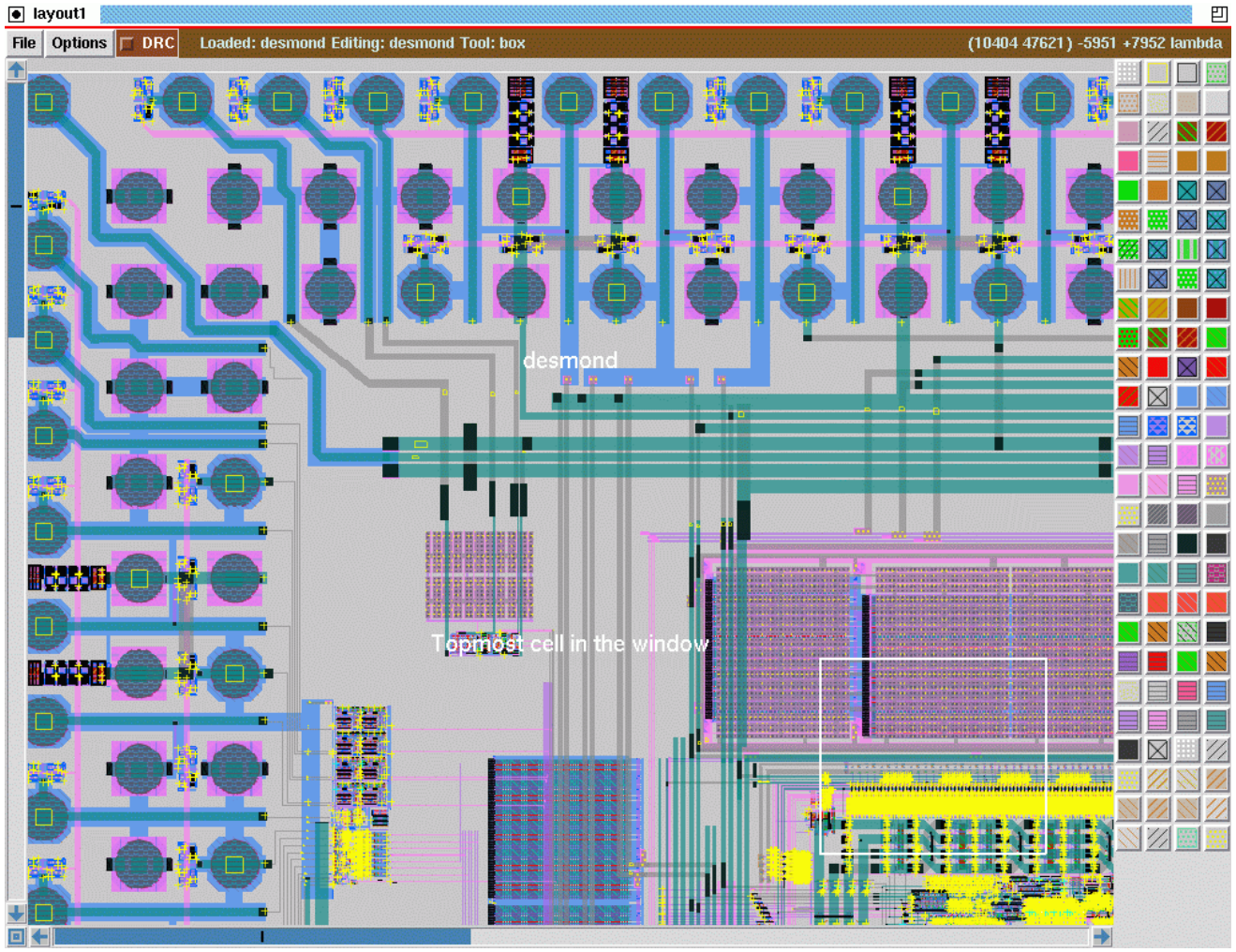
Very Large Scale Integration (VLSI) Layout

Building circuits with millions of transistors through photo lithography

Magic Open Source VLSI Design Tool

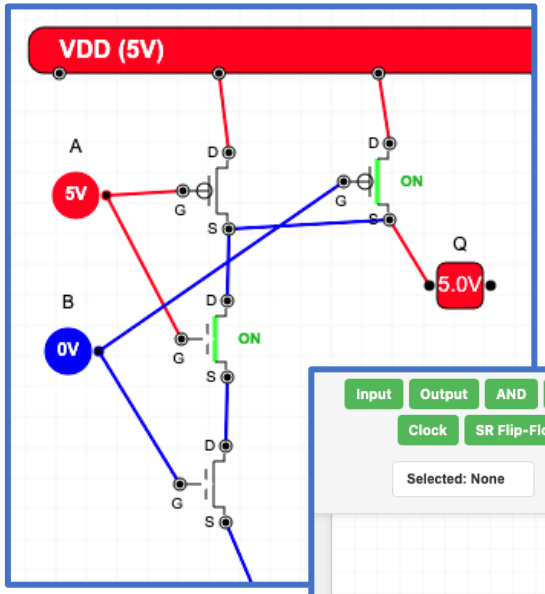
- Created at Berkeley in 1983
- Open source
- Popular in academia
- Many tutorials

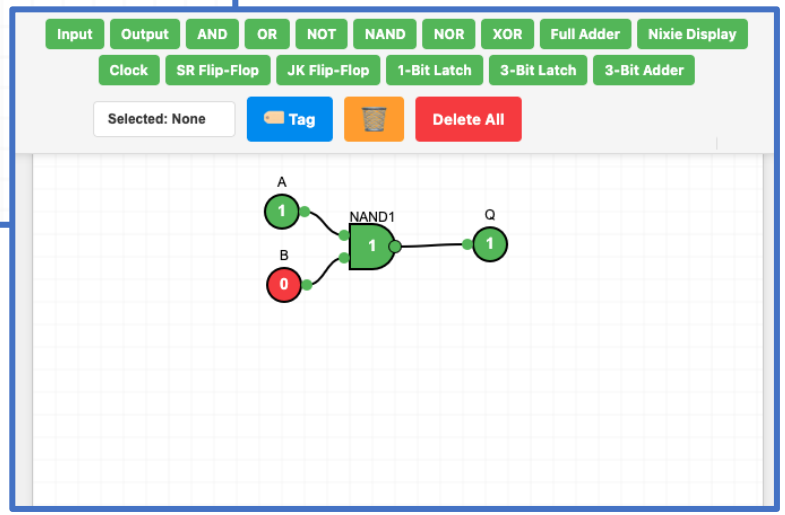
http://opencircuitdesign.com/magic/

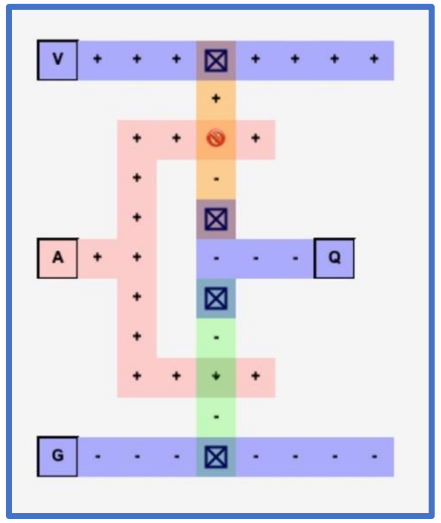


About My Emulators

- My circuit layout and emulation tools are limited
- Focused on learning objectives of the course
- Run in the browser
- They fail if circuits get too complex
- There are many emulators that are more serious and more accurate – just search



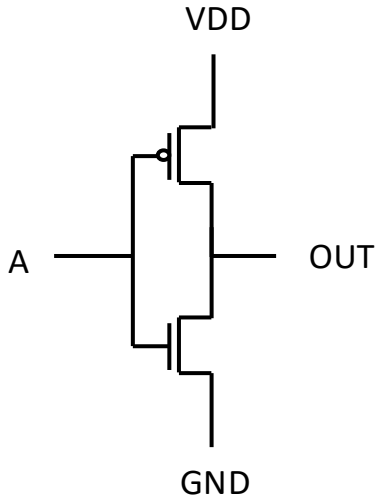




VLSI CMOS Not

Not

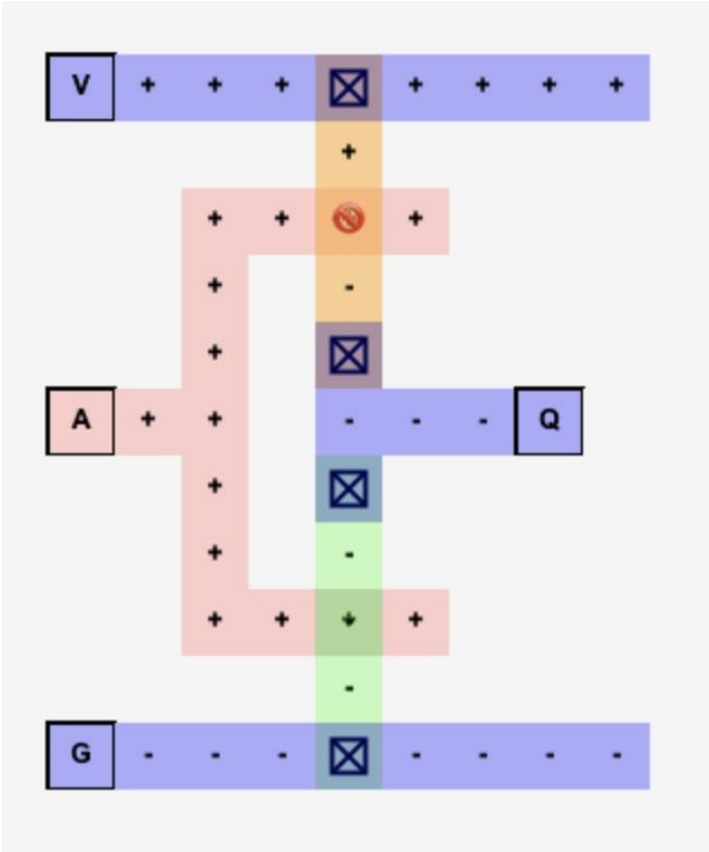
A	Q
0	1
1	0



Mistic VLSI Layout

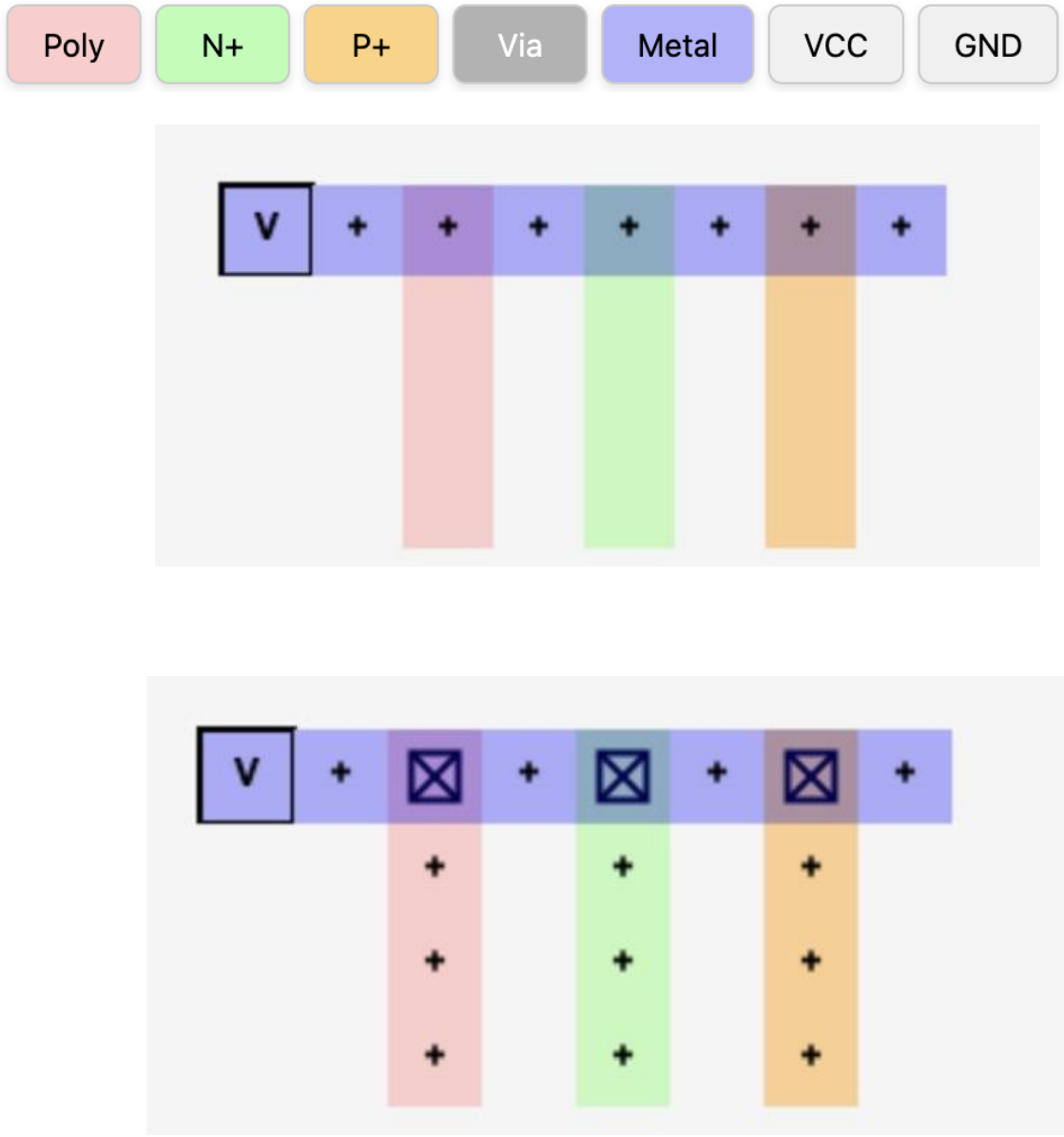
Poly | N+ | P+ | Via | Metal | VCC | GND

Layers



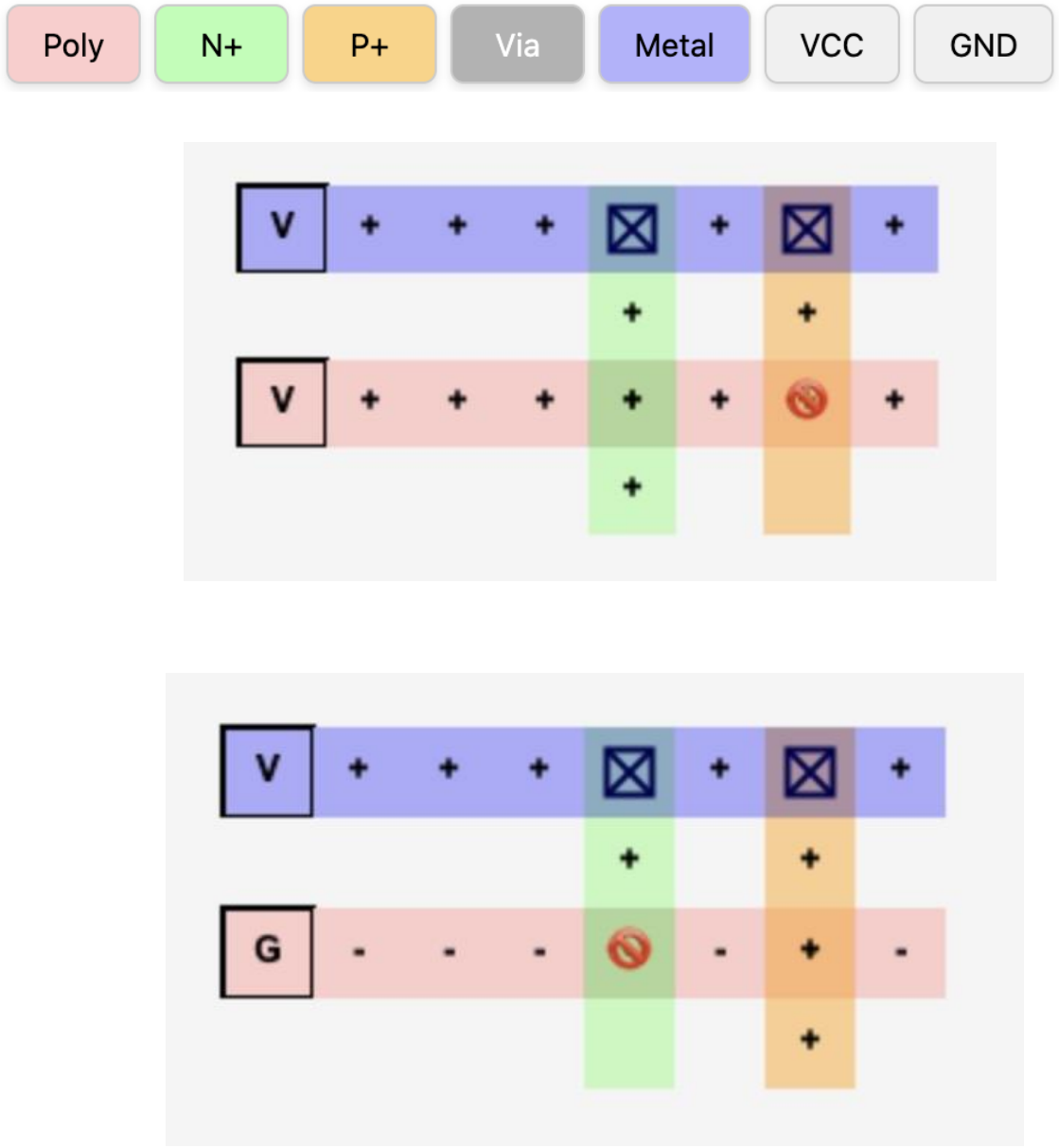
Drawing Layers

- Metal – Conductor
- N-Doped Silicon
- P-Doped Silicon
- Polysilicon
- These are not connected unless you place a "Via" at a connection point
- The Via is a vertical connector between layers



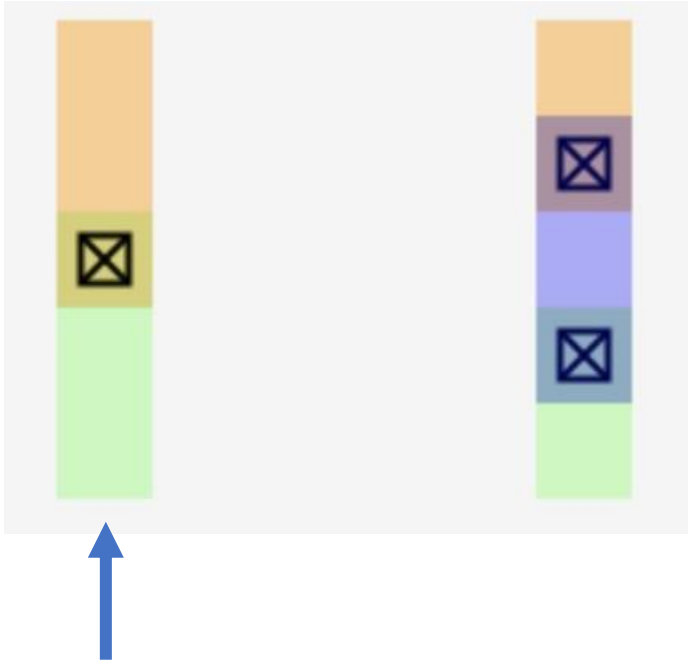
Transistors

- When N-Doped Silicon crosses Polysilicon an NMOS Transistor is created
- When P-Doped Silicon crosses Polysilicon an NMOS Transistor is created
- The voltage on the Polysilicon controls the conductivity of the transistors



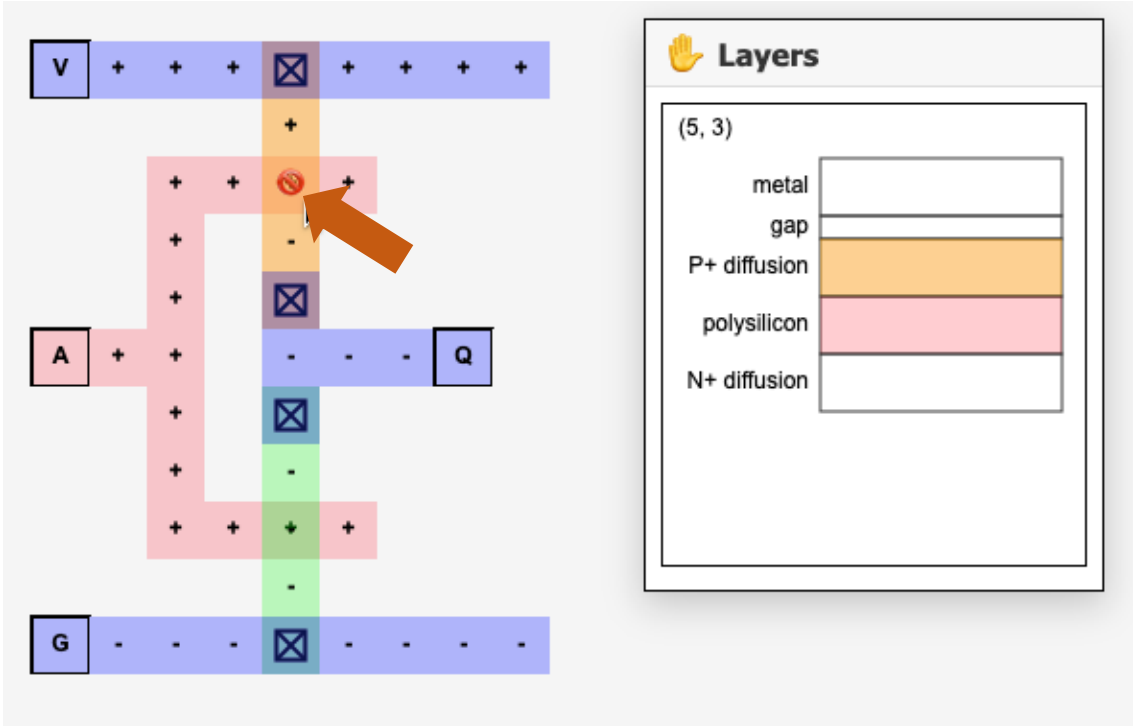
About Layout

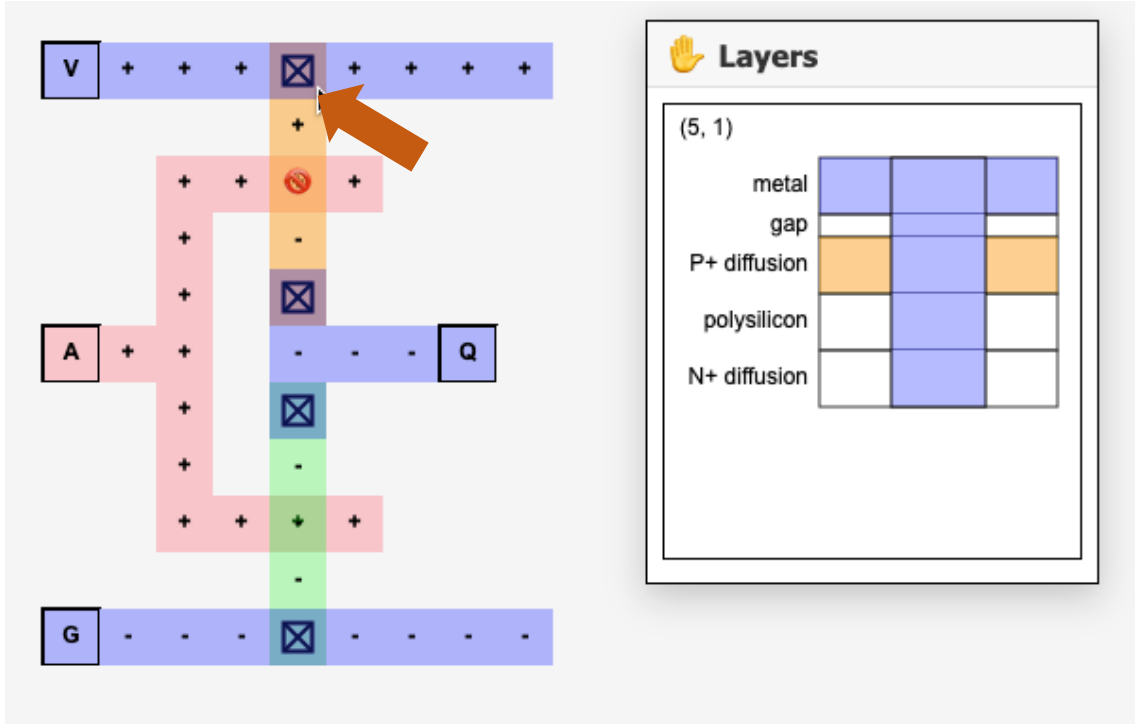
- Mistic is greatly simplified
- Mistic circuit emulation is very simple
- AI: Explain the differences between VLSI layout as might be used in the Magic circuit design tool and the actual construction of chips on silicon wafers
- For example – You can't overlap N+ and P+ due to manufacturing limitations



Cannot be manufactured

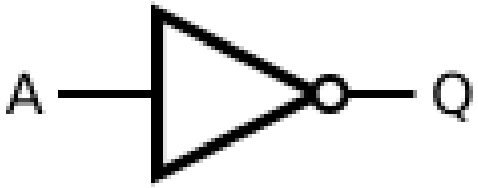
Looking at the Layers

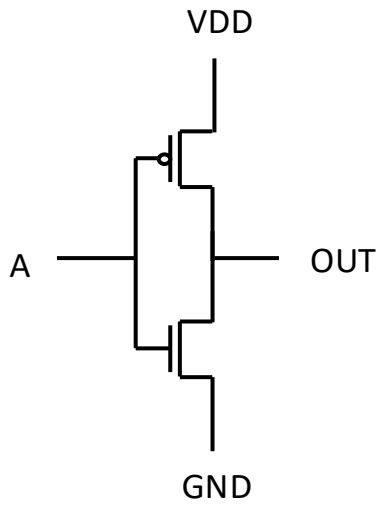




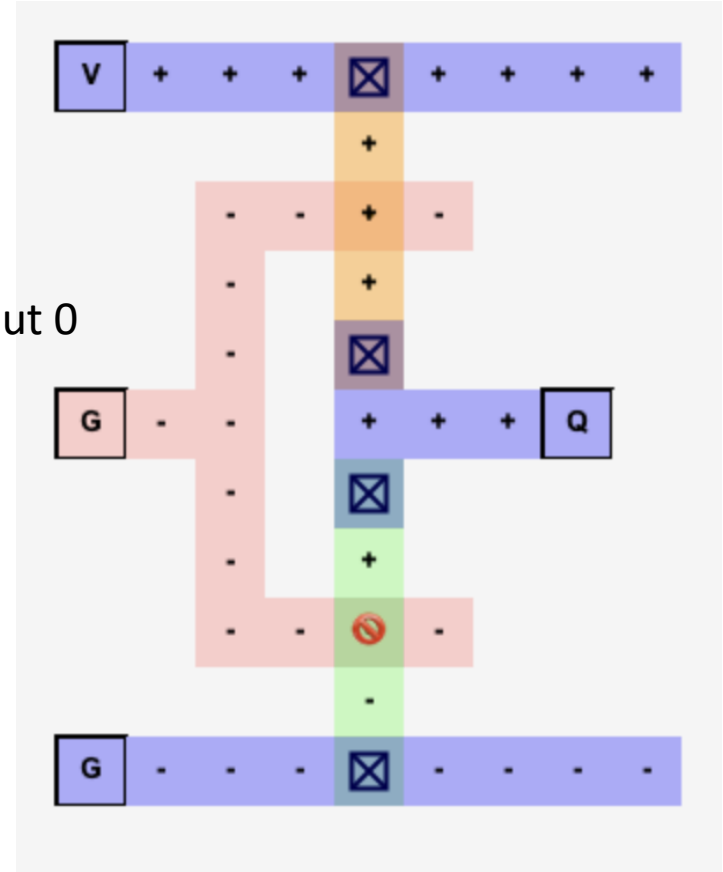
Poly | N+ | P+ | Via | Metal | VCC | GND

VLSI CMOS Not

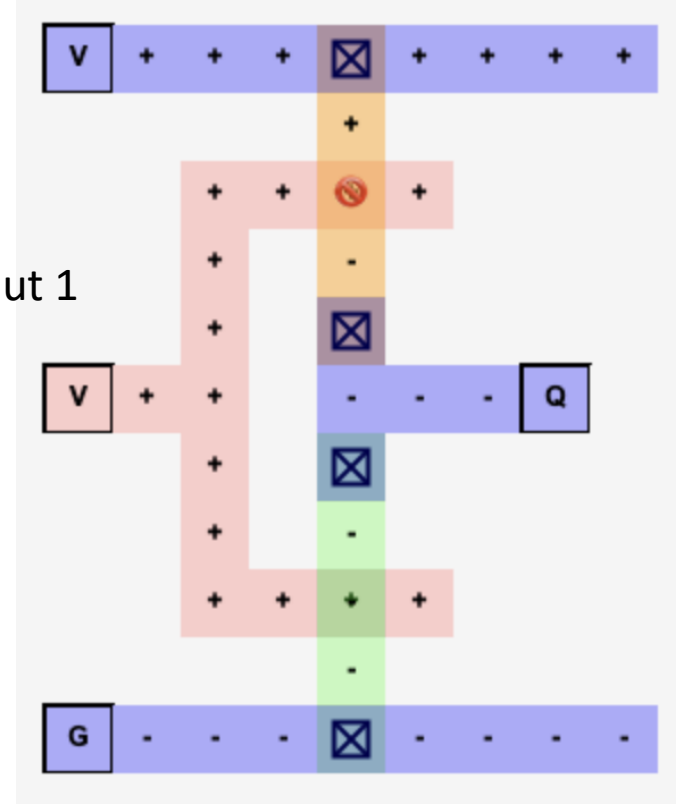




Input 0

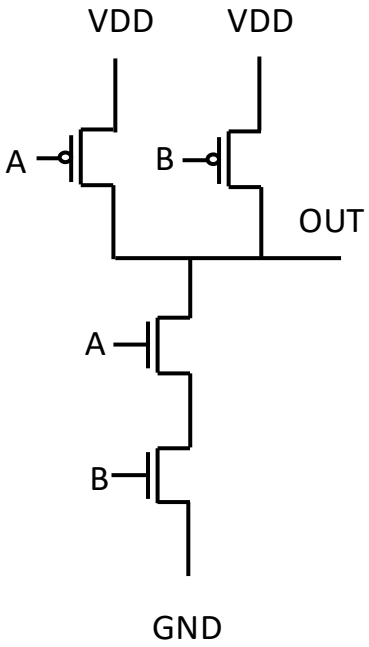


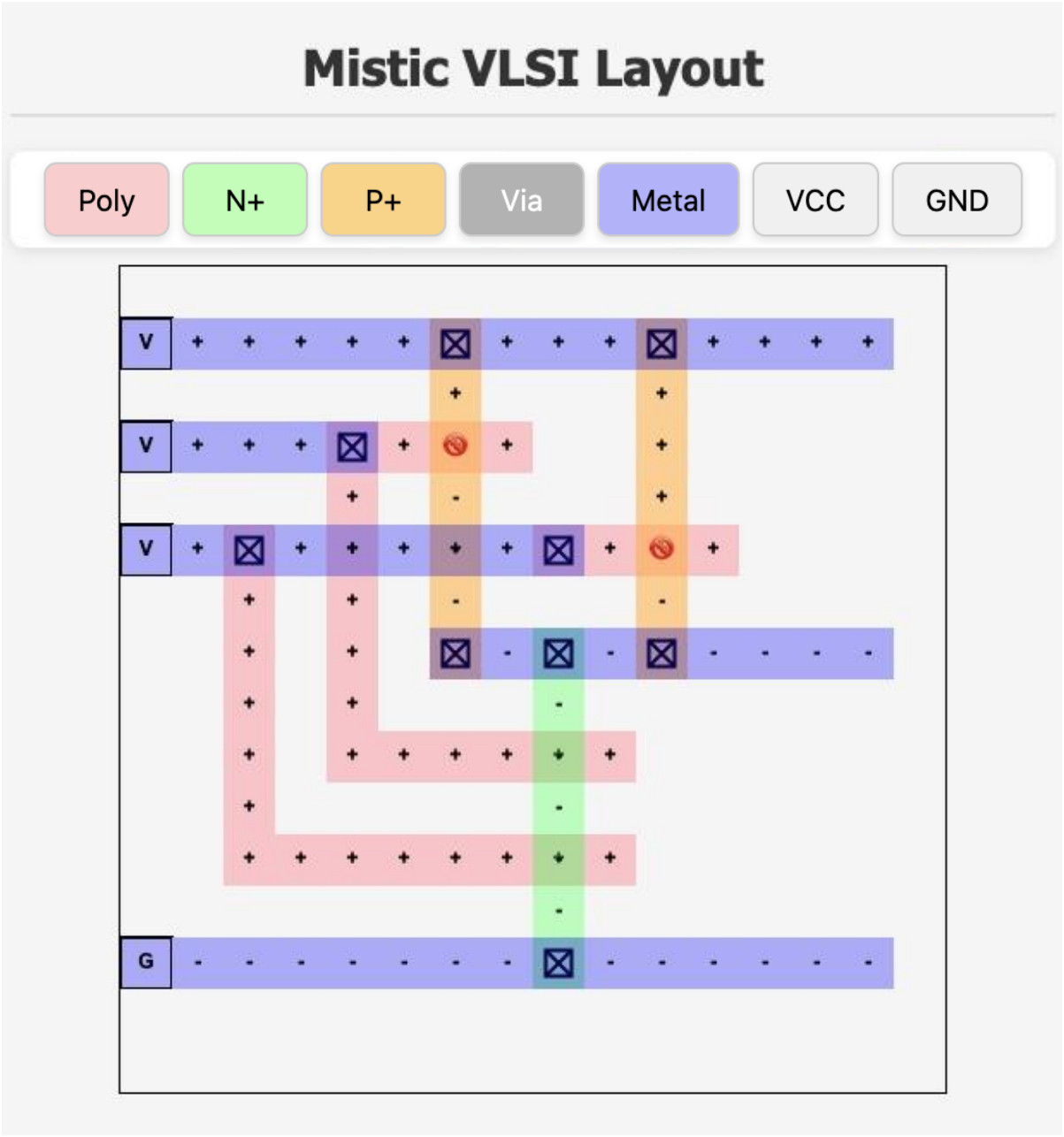
Input 1



VLSI CMOS NAND

A	B	Q
0	0	1
0	1	1
1	0	1
1	1	0





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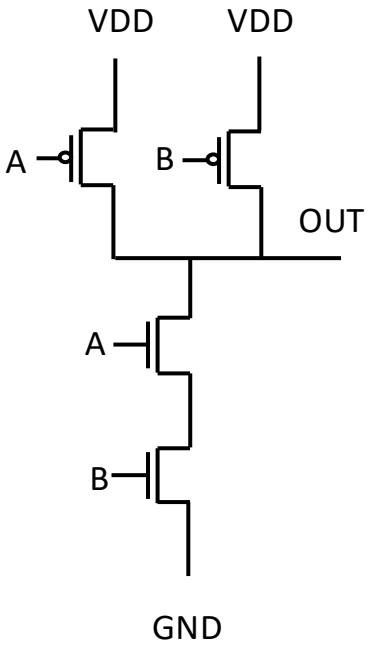

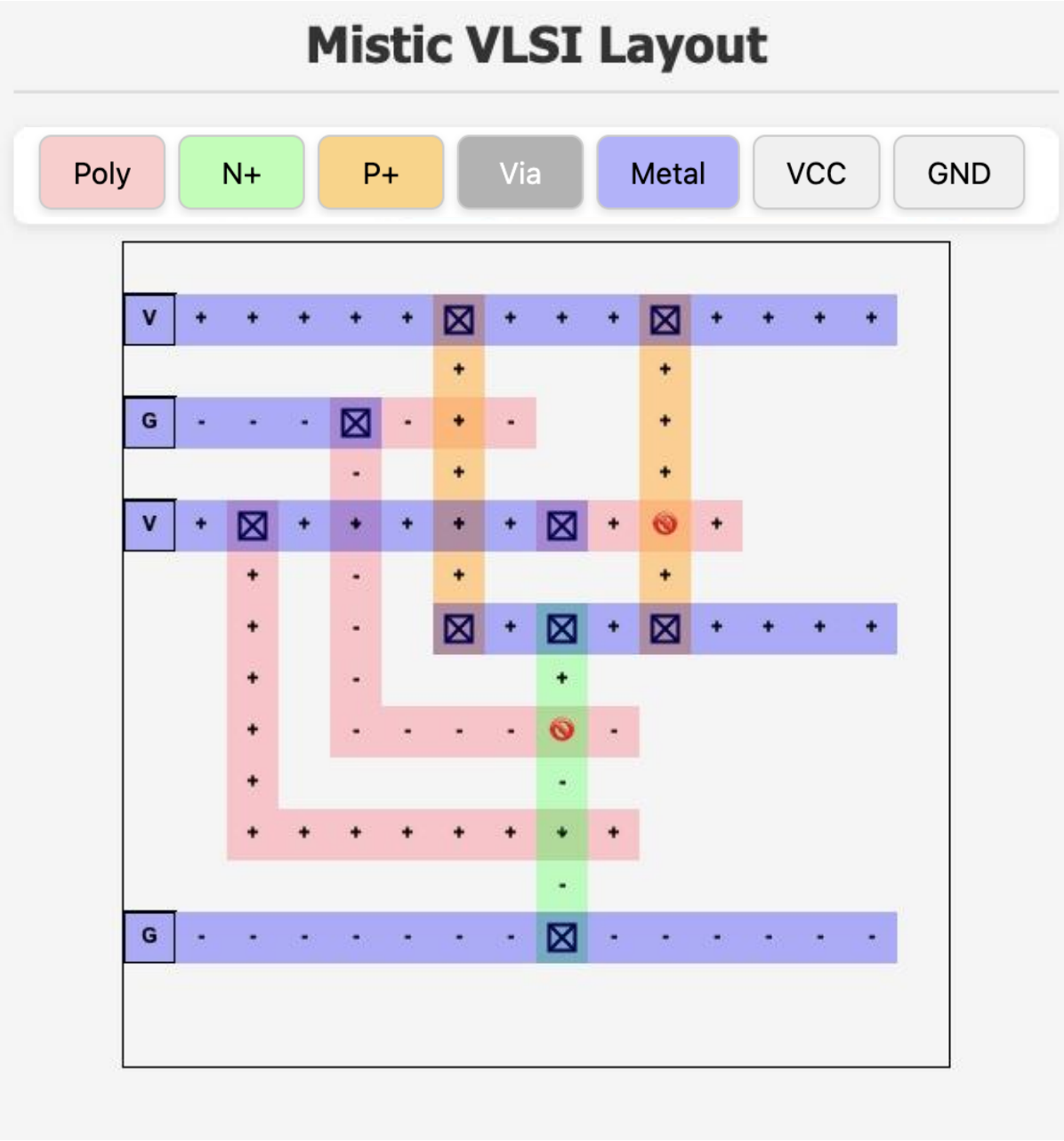

Summary

- Number of transistors on a chip over time
- Photo lithography
- Designing VLSI chips

Acknowledgements / Contributions

Initial Development: Charles Severance, University of Michigan School of Information

Insert new Contributors and Translators here including names and dates

Continue new Contributors and Translators here