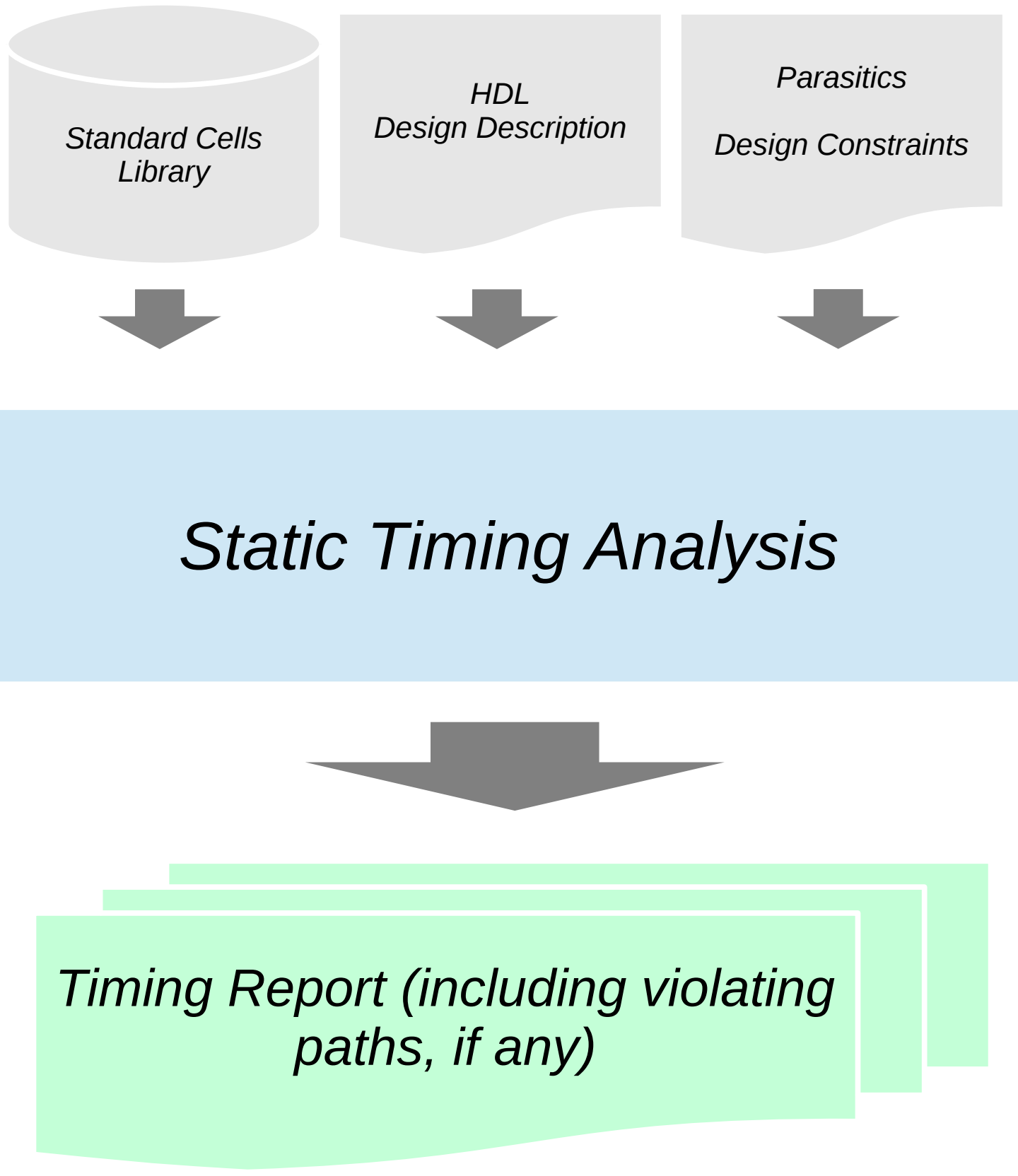
Standard Cells Library
HDL Design Description
Parasitics
Design Constraints
Static Timing Analysis
Timing Report (including violating paths, if any)