

## **LEGENDA**

**u1** = *driver* da interconexão **n1** 

 $\mathbf{a} \rightarrow \mathbf{o}$  e  $\mathbf{b} \rightarrow \mathbf{o} = timing \ arcs$  da porta lógica  $\mathbf{u}\mathbf{1}$ 

