

```
graph TD; A[Standard Cells Library] --> D[Static Timing Analysis]; B[HDL Design Description] --> D; C[Parasitics Design Constraints] --> D; D --> E[Timing Report (including violating paths, if any)];
```

*Standard Cells
Library*

*HDL
Design Description*

*Parasitics
Design Constraints*

Static Timing Analysis

*Timing Report (including violating
paths, if any)*