Overview

SPARK Microsystem's SR1120 is a short-range wireless transceiver that enables low and predictable latency and ultra-low power data communications, capable of reaching PHY rates of up to 40.96 MHz. Operating in the license-free ultra-wideband (UWB) spectrum, the SR1120 facilitates communications that are not only highly robust but also remarkably energy-efficient.

Figure 1: SR1120

The transceiver's architecture includes a RF section with antenna diversity, ensuring reliable signal quality and strength. Integrated digital and baseband logic, along with a power management unit, contribute to its low power consumption. Additionally, the device includes a low power clock input and a sleep counter to further enhance its energy efficiency. Control of the SR1120 is streamlined through a standard SPI or QSPI interface, allowing for seamless integration with an MCU and straightforward management in a variety of applications. This makes the SR1120 an excellent choice for developers seeking a powerful yet energy-conscious solution for their wireless communication needs.

The SR1120 is a highly versatile, digitally programmable UWB wireless transceiver operating within the license-free 6.0-10.2 GHz UWB spectrum. This device leverages short impulses to enable communications that are not only robust but also exceptionally energy-efficient. Designed to dynamically shape its output spectrum, the SR1120 adheres to international UWB emission standards and can be tailored to various spectral masks. Its circuits feature aggressive duty cycling, ensuring ultra-low power consumption during operation. The SR1120 excels in a range of data rates, optimizing power consumption and making it an ideal choice for wireless applications that demand high energy efficiency, minimal latency, flexible operation, and reliable communications.

Features

- Dynamically reconfigurable UWB spectrum
    - 6.7 – 9.2 GHz center frequency
    - Up to 3dBm TX power
    - RX sensitivity of -81 dBm
- Antenna diversity support
- UWB PHY layer
    - Compliant IEEE 802.15.4ab draft-clause 33
    - 20.48, 27.30 and 40.96 MHz PHY rates
    - 256 Bytes transmit and receive buffers
- Standard SPI and Quad-SPI interfaces
- 1.8 to 3.3 V supply
- Industrial operating range: -40 to +85 ℃
- Package
    - 4 x 4 mm 32 pin QFN
    - WLCSP compatible

Key Benefits

- Ultra-low power consumption
    - Outstanding energy efficiency of 0.3 nJ/bit for TX and 0.7 nJ/bit for RX
    - MicroWatt power consumption for sub-Mbps communications
    - Maximum peak output power 4.2 dBm
- Ultra-short latency
    - 50 μs airtime for 1 kbit (20.48MHz)
    - Ideal for real-time data streams such as Headset and HID applications
    - Coexistence and reduced interference with BLE, WiFi (2.4, 5 & 6 GHz) and cellular
- Low-cost BOM
    - 32.768 kHz crystal
    - High-efficiency PCB antenna
- Support for Carrier-Sense (CSMA) stack
- SDK support
- Evaluation Kits available

Contents

1   System Overview

1.1   Block diagram
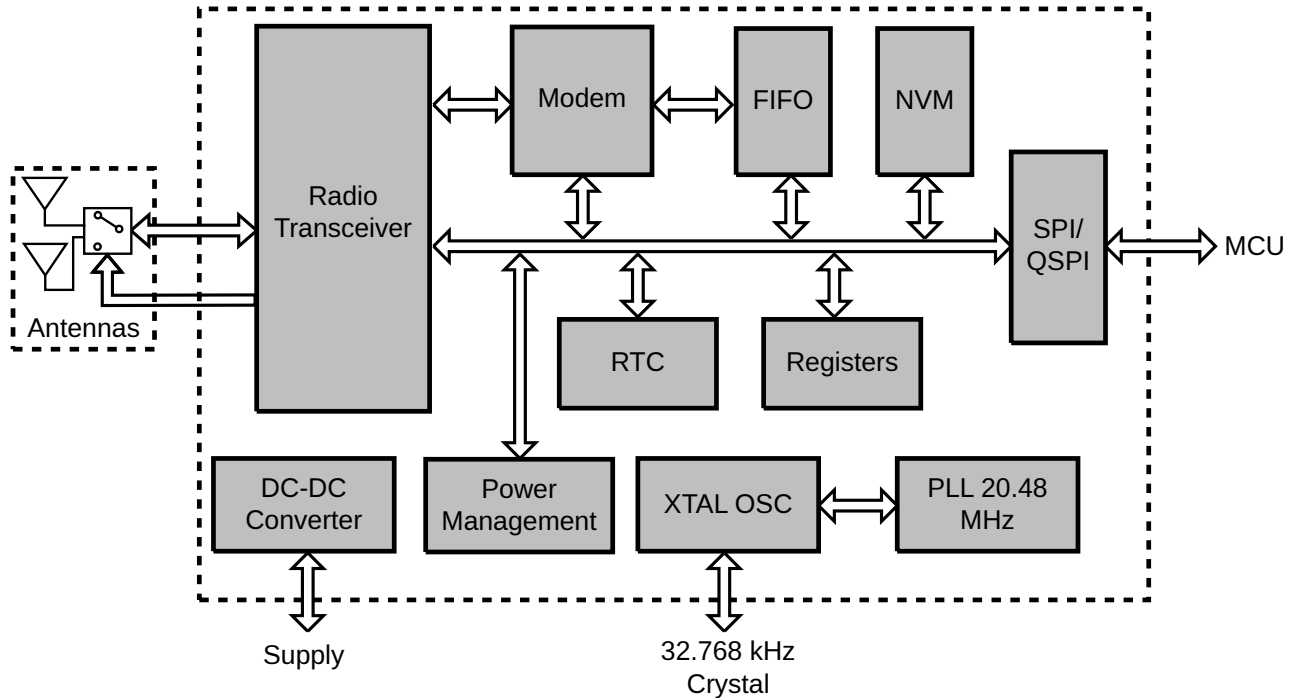
Figure 1.1: Block diagram of the SR1120.

1.2   Radio transceiver description

The radio transceiver support a proprietary impulse radio and a standard IEEE-802.15.4ab draft compliant radio. The transceiver operates in the license-free UWB spectrum. The transmitter is highly flexible and can be adapted to efficiently fill the available RF spectrum, taking into account the realized antenna gains in a specific implementation. The receiver operates in non-coherent mode and is robust to in-band and out-of-band interferers. The transceiver supports multiple PHY rates to enhance applications requirements. On-Off Keying (OOK) is supported by the modem, as well as differential encoding (2bit-PPM) , configurable punctured FEC , variable preamble length, variable sync word and programmable CRC polynomial. A 2kbit receive and transmit buffer are available to buffer the packets. The data rate and available RF spectrum constrains the allowable transmitter parameters. As a result, the link budget is higher for low data rate links and lower for high data rate links. Additionally, the transceiver operates uniquely with only a 32.768 kHz quartz, enabling very low power timing. The transmitter can be programmed to have a variable pulse width via radio control settings. The transmitter can also be controlled to vary the number of pulses used within each symbol. A variable output power setting can fine tuned during each transmission.

1.3   Clocks

A 32.768 kHz clock is generated by the XTAL oscillator using an external crystal. This clock powers the Real Time Clocks (RTC) implementation. A 40.96 MHz clock is synthesized on-chip from the XTAL clock using a PLL. This PLL requires an off-chip loop filter and is power cycled according to the usage profile.

1.4   Power modes

The SR1120 supports several power modes. Accurate power cycling is key to reaching high energy efficiencies. The sleep controller contains automatic sleep and wake-up conditions.

Function	Shutdown	Deep Sleep	Shallow Sleep	Idle	Active
Register retention	No	Yes	Yes	Yes	Yes
SPI communication	Off	On	On	On	On
PLL clock	Off	Off	On	On	On
DC-DC output	Off	Off	Off	On	On
Radio	Off	Off	Off	Off	On
Next state	Deep Sleep	Shallow Sleep	Idle	Active	Any

Table 1.2: Power States

1.5   Reset

At system startup, the RSTN pin should be held low until the supply voltage is stable. Normal operation starts after pulling RSTN high.

The Shutdown mode allows minimum current consumption, and can be entered by pulling SHUTDOWN high. Wake-up from Shutdown mode is accomplished by pulling SHUTDOWN low, while keeping RSTN low to reset the SR1120. Normal operation starts after pulling RSTN high.
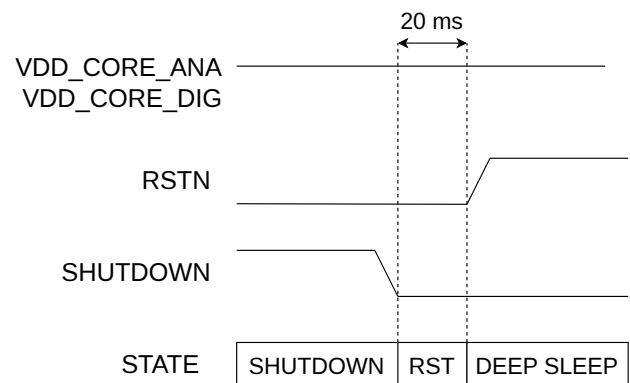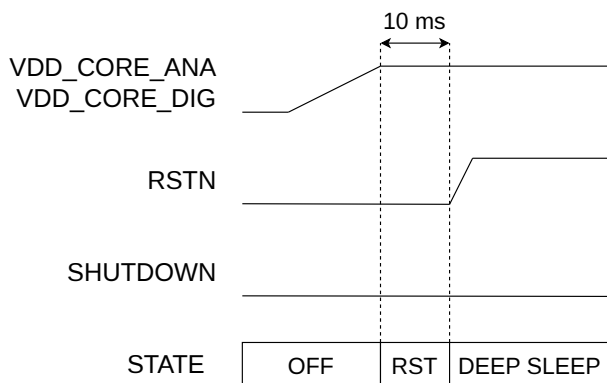
Figure 1.3: Timing sequence during power on (left) and shutdown (right).

Figure 1.3 illustrates the power-on sequence and wake-up out of shutdown. Note that in both sequences the digital core is initialized to the default register state.
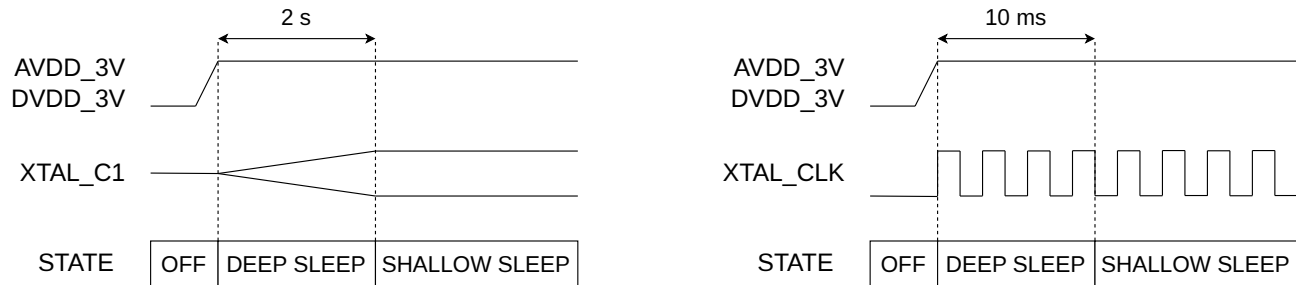
Figure 1.4: XTAL sequence with internal (left) and external (right) 32.768 kHz source.

After power-on or leaving shutdown mode, the XTAL clock source has to provide a stable 32.768 kHz clock before deep sleep can be exited into shallow sleep. An external 32.768 kHz clock source can be used as an input to the XTAL_CLK pin, as shown in Figure 1.4.

1.6 SPI QSPI interface

The SR1120 can be control over a SPI/QSPI protocol. After reset the interface is set to be in SPI mode (SPI mode 0). The following transcations examples are supported in SPI and QSPI mode. A transaction is determine by the CSN signaling. A transaction start with CSN going low and finishes when it goes up. The bit transfer level on SPI is MSB first, see Figure 1.5.
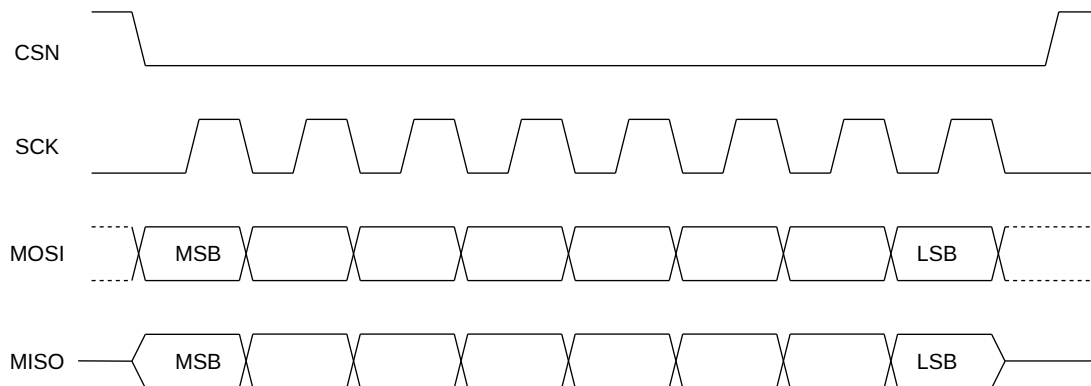
Figure 1.5: Timing of a single byte on the SPI protocol.

The non-burst (normal) read and write register protocol is illustrated in Figure 1.7. Every read and write transaction starts with a command byte, where the bit 7 indicates if a normal (0) or a burst (1) transfer is coming and the bit 6 indicates if the transaction will be a reading (0) or writing (1) operation. The 6 remaining bits constitute the register address to access for that transaction. During the data transfer of a read transaction, the contents at the designated register address is returned on MISO while the MOSI signal values is ignored.

Command bit	Description	Value
7	Mode	*1* burst, *0* normal (non-burst)
6	Operation (Read or Write)	*1* write, *0* read
5:0	Address	Value

Table 1.6: Command bit mapping
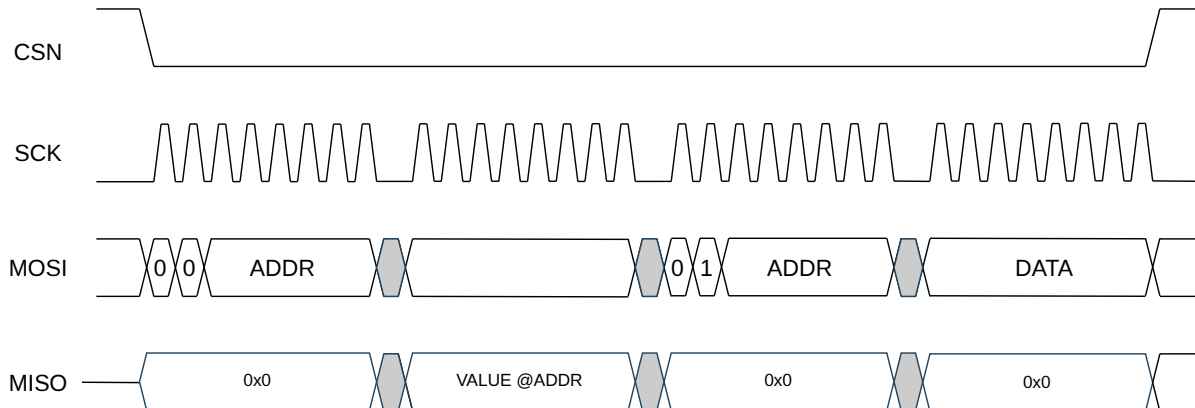
Figure 1.7: SPI read and write register transaction.

During the data transfer of a write transaction, the new value to write at the designated register address is received through the MOSI signal while the MISO signal remains low.
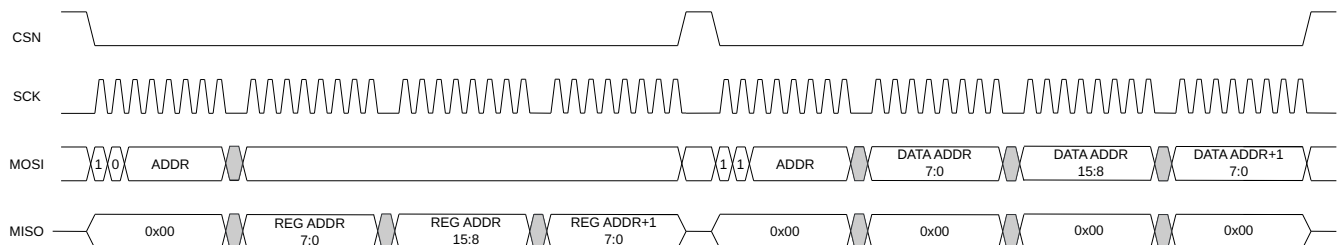
Figure 1.8: SPI burst read and write transaction.

The SPI burst transfers is illustrated in Figure 1.8. SPI burst transfers continuously transfer data bits every SPI clock cycle indefinitely until CSN is raised. The address will be incremented while the transaction is active for every two (2) bytes.

The QSPI uses the same mechanism that offer SPI but instead of using MISO / MOSI, the QSPI uses all four (4) bits for data transmission (IO3,IO2,IO1,IO0) see Figure 1.9. The devices changes IO direction, on the data bytes, depending if a read operation transaction is issued.
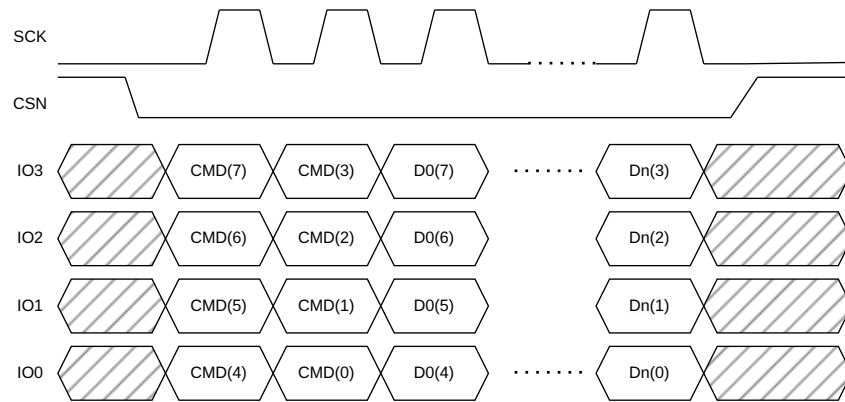
Figure 1.9: QSPI transaction.

1.7 Interrupt controller and RTC

The interrupt controller can be programmed to launch an asynchronous interrupt A on IRQ on certain events. This allows the MCU to sleep. Common interrupt events include packet reception, frame transmit completed, wakeup from sleep, and more.

A low-power Real Time Clock (RTC) is available in every mode except shutdown, which can wake up into higher sleep modes.

2 Pinout

2.1 Package
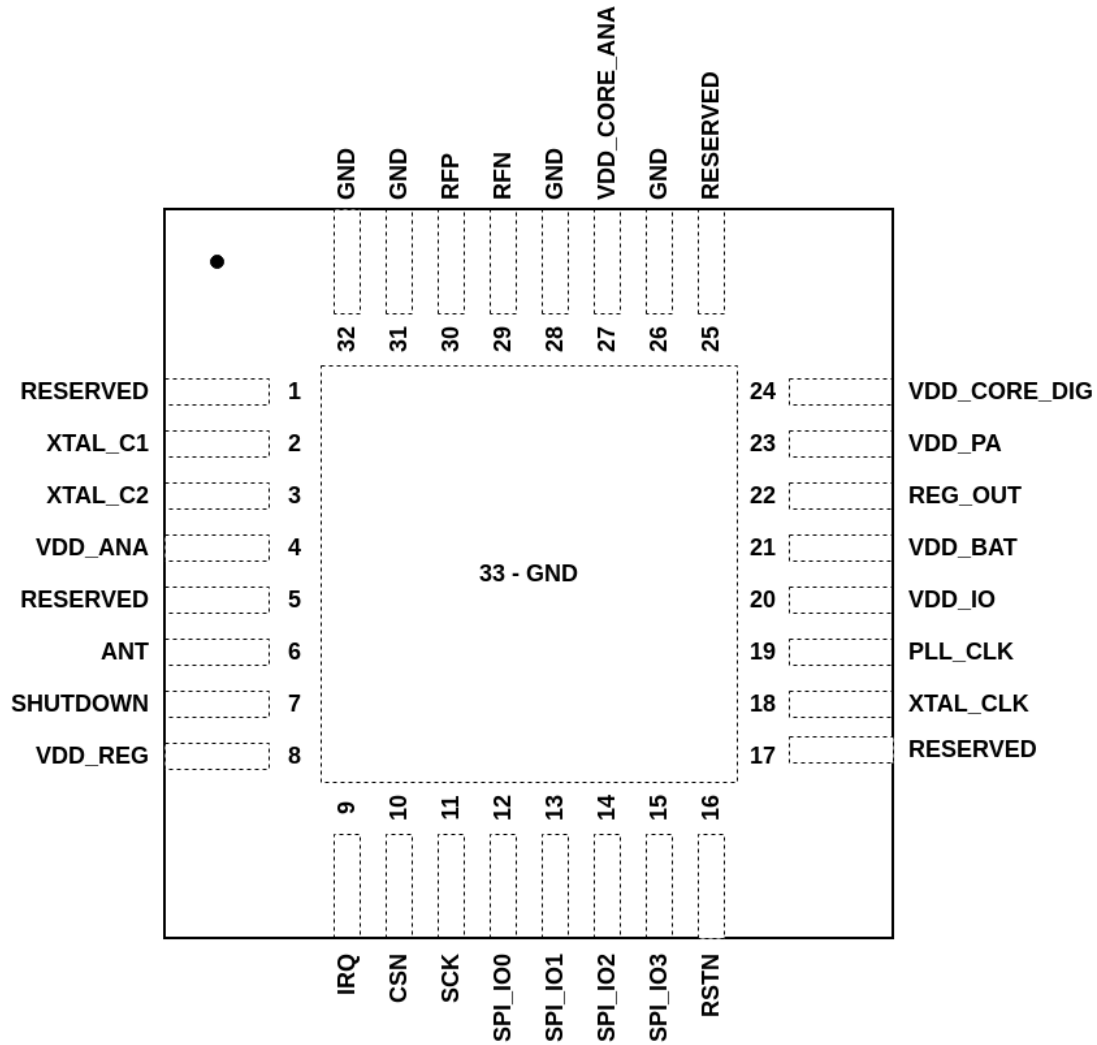
Figure 2.1: QFN32 Package

2.2 Pinouts

Name	Pin	Type	Description
RFP	30	Analog Input/Output	Positive RF input/output.
RFN	29	Analog Input/Output	Negative RF input/output.
CSN	10	Digital Input	SPI Chip Select.
SCK	11	Digital Input	SPI clock.
SPI_IO0/MOSI	12	Digital Input/Output	SPI data 0 or MOSI.
SPI_IO1/MISO	13	Digital Input/Output	SPI data 1 or MISO.
SPI_IO2	14	Digital Input/Output	SPI data 2.
SPI_IO3	15	Digital Input/Output	SPI data 3.
XTAL_C1	2	Analog Input	32.768 kHz crystal oscillator pin 1.
XTAL_C2	3	Analog Output	32.768 kHz crystal oscillator pin 2.
RESERVED	1	No connect	
SYNC_TXEN	5	Digital Output	Multipurpose io, Recommeded test point connection.
ANT	6	Digital Output	Antenna switch driver.
SHUTDOWN	7	Digital Input	Normal operation when pin is low, chip is off when pin is high. Connect to GND if not used.
RSTN	16	Digital Input	Main reset pin; driving it low resets the SR1120.
RESERVED	25	Reserved connect to gnd.	
IRQ	9	Digital Output	Generates user-configurable external interrupt.
PLL_CLK	19	Digital Input/Output	PLL external clock input/output.
XTAL_CLK	18	Digital Input/Output	XTAL external clock input/output.
VDD_ANA	4	Power	Supply for analog circuits, connect to VDD_BAT.
VDD_BAT	21	Power	Supply for switching/digital circuits.
VDD_IO	20	Power	Supply for IO cells.
VDD_CORE_ANA	27	Power	Regulated 1V supply to analog radio PHY.
VDD_CORE_DIG	24	Power	Regulated 1V supply to digital radio PHY.
VDD_REG	8	Power	Connect to decoupling capacitor.
VDD_PA	23	Power	Supply for PA, connect to either VDD_BAT or VDD_CORE.
RESERVED	17	GND	Reserved connect to gnd.
REG_OUT	22	Analog Output	Output of DC-DC regulator.
GND	26,28,31,32,33	Power	All GND pins must be connected together in the lowest impedance possible. Return currents are directed through the QFN thermal pad.

Table 2.2: Pin Descriptions.

3   Application Overview

3.1   Application Circuit
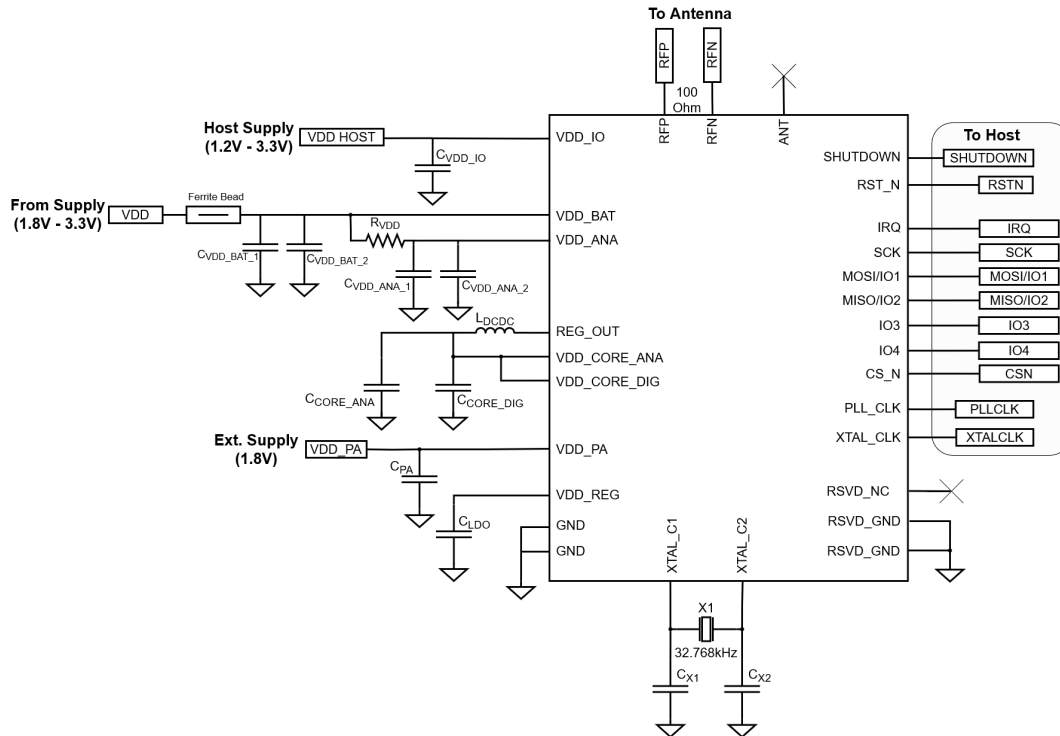
Figure 3.1: Application reference circuit

The schematic of a typical application is given in figure above.

3.2   Application Guidelines

Please observe the following guidelines:

- Connect RFP and RFN to the balun/antenna with a 100 Ohm differential transmission line.
- Connect VDD, VDD_HOST to the supply voltage with a low impedance trace. Place CVDD_BAT_1 and CVDD_BAT_2 as close as possible to VDD_BAT (same rule applies to CVDD_ANA_1 and C_VDD_ANA_2 on VDD_ANA). CVDD_BAT_1 and CVDD_BAT_2 can be increased for better supply noise rejection (same applpies to CVDD_ANA_1 and CVDD_ANA_2).

- Connect VDD_PA to VPA and place C8 as close as possible to VDD_PA pin.
- Place C3 and C4 as close as possible to VDD_CORE_ANA and VDD_CORE_DIG pins.

- Place C9 as close as possible to VDD_REG pin.
- When using SPI interface, connect CS, SCK, SPI_IO0/MOSI, SPI_IO1/MISO, RSTN and IRQ to your MCU. When using QSPI interface, connect all the QSPI_IO0-3 to your MCU.

- Use of SHUTDOWN is optional. If not used, connect SHUTDOWN to GND.

- Connect all GND pins to GND. Connect all GND pads together with low impedance.
- When using XTAL_CLK and/or PLL_CLK as clock inputs, connect to your clock source. Leave unconnected otherwise.
- Minimize the capacitance on the REG_OUT node, including the parallel capacitance of the inductor.
- Adjust C_{x1} and C_{x2} to the specifications of your crystal.
- Inductor L1 Shall be < 0.75 Ω ESR, > 200 mA saturation current, and > 200 MHz self-resonance frequency.

3.2.1   Recommended Part Values

For complete information see SR1120 Hardware Design Guide.

4 Electrical Characteristics

4.1 Maximum Ratings

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Storage Temperature		-50	150	∘C
Pin Voltage (all pins except AVDD_1V, DVDD_1V, DVDD_1V8)		-0.3	3.6	V
Pin Voltage (AVDD_1V, DVDD_1V)		-0.3	1.1	V
Pin Voltage (DVDD_1V8)		-0.3	1.98	V
ESD (Human Body Model)			2000	V
ESD (Charged Device Model)			500	V

Table 4.1: Absolute Maximum Ratings.

4.2 DC characteristics

Parameter	Test Conditions	MIN	TYP	MAX	UNIT
Shutdown Current, VDD BAT	VDD BAT=3.3V		157		nA
	VDD BAT=2.5V		20		nA
	VDD BAT=1.8V		6		nA
Deep Sleep Current, VDD BAT	VDD BAT=3.3V		1.1		uA
	VDD BAT=2.5V		0.77		uA
	VDD BAT=1.8V		0.57		uA
Shallow Sleep Current, VDD BAT	VDD BAT=3.3V		58		uA
	VDD BAT=2.5V		57		uA
	VDD BAT=1.8V		57		uA
Idle Current, VDD BAT	VDD BAT=3.3V		390		uA
	VDD BAT=2.5V		450		uA
	VDD BAT=1.8V		565		uA
DLL On Current, VDD BAT	VDD BAT=3.3V		500		uA
	VDD BAT=2.5V		580		uA
	VDD BAT=1.8V		740		uA
TX Current*, VDD BAT (see below)	VDD BAT=3.3V, phy rate=20.48MHz, 2 pulse/symbol, duty cycle=100%		3.3		mA
	VDD BAT=2.5V, phy rate=20.48MHz, 2 pulse/symbol, duty cycle=100%		4.2		mA
	VDD BAT=1.8V, phy rate=20.48MHz, 2 pulse/symbol, duty cycle=100%		5.7		mA
RX Current, VDD BAT	VDD BAT=3.3V		9.7		mA
	VDD BAT=2.5V		12.1		mA
	VDD BAT=1.8V		16		mA
Shutdown Current, VDD PA	VDD PA=1.8V		125		nA
Deep Sleep Current, V VDD PA	VDD PA=1.8V		0.27		uA
Shallow Sleep Current, VDD PA	VDD PA=1.8V		0.30		uA
Idle Current, VDD PA	VDD PA=1.8V		1.2		uA
DLL On Current, VDD PA	VDD PA=1.8V		1.2		uA
TX Current1, VDD PA	VDD PA=1.8V, phy rate=20.48MHz, 2 pulse/symbol, duty cycle=100%		6		mA
RX Current, VDD PA	VDD PA=1.8V		11		uA

Table 4.2: DC characteristics.

(*)TX Current given for 40.96 Mpulse/s continuous transmission. Current scales with duty cycle, phy_rate and pulse/symbol.

4.3 Internal XTAL Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Crystal oscillator frequency			32.768		kHz
Crystal frequency tolerance		-30		+30	ppm
Startup time		1.5	1.75	2	s

Table 4.3: Internal XTAL characteristics.

4.4 Internal PLL Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PLL Output frequency			40.96		MHz
PLL Startup time			1.5		ms

Table 4.4: Internal PLL characteristics.

4.5 Radio Characteristics

4.5.1 Transmitter

Parameter	Test Conditions	MIN	TYP	MAX	UNIT
TX Power 20.48MHz	VDD_PA=1.8V, num_pulse=1, pulse_width=med, tx_power=max, duty_cycle=100%, phy_rate=20.48MHz		-0.3		dBm/20 MHz
	VDD_PA=1.8V, num_pulse=1, pulse_width=med, tx_power=min, duty_cycle=100%, phy_rate=20.48MHz		-5.0		dBm/20 MHz
	VDD_PA=1.8V, num_pulse=2, pulse_width=med, tx_power=max, duty_cycle=100%, phy_rate=20.48MHz		2.7		dBm/20 MHz
	VDD_PA=1.8V, num_pulse=2, pulse_width=med, tx_power=min, duty_cycle=100%, phy_rate=20.48MHz		-2.0		dBm/20 MHz
	VDD_PA=1.8V, num_pulse=3, pulse_width=med, tx_power=max, duty_cycle=100%, phy_rate=20.48MHz		4.2		dBm/20 MHz
	VDD_PA=1.8V, num_pulse=3, pulse_width=med, tx_power=min, duty_cycle=100%, phy_rate=20.48MHz		-0.5		dBm/20 MHz

Table 4.5: Radio characteristics 20.48MHz

Parameter	Test Conditions	MIN	TYP	MAX	UNIT
TX Power 40.96MHz	VDD_PA=1.8V, num_pulse=1, pulse_width=med, tx_power=max, duty_cycle=100%, phy_rate=40.96MHz		2.7		dBm/40 MHz
	VDD_PA=1.8V, num_pulse=1, pulse_width=med, tx_power=min, duty_cycle=100%, phy_rate=40.96MHz		-2.0		dBm/40 MHz
TX Lower Sidelobe	VDD_PA=1.8V, pulse_width=max		-29		dBc
	VDD_PA=1.8V, pulse_width=min		-24		dBc
TX Upper Sidelobe	VDD_PA=1.8V, pulse_width=max		-22		dBc
	VDD_PA=1.8V, pulse_width=min		-21		dBc
TX Bandwidth -10 dB	VDD_PA=1.8V, pulse_width=max		380		MHz
	VDD_PA=1.8V, pulse_width=min		770		MHz
TX Center Frequency		6.5		8.5	GHz

Table 4.6: Radio characteristics 40.96MHz

Parameter 20.48Mhz	Test Conditions	MIN	TYP	MAX	UNIT
TX Peak Power Density	VDD_PA=1.8V, num_pulse=1, pulse_width=med, tx_power=max, duty_cycle=100%, phy_rate=20.48MHz		-6.2		dBm/MHz
	VDD_PA=1.8V, num_pulse=1, pulse_width=med, tx_power=min, duty_cycle=100%, phy_rate=20.48MHz		-10.9		dBm/MHz
	VDD_PA=1.8V, num_pulse=2, pulse_width=med, tx_power=max, duty_cycle=100%, phy_rate=20.48MHz		-1.5		dBm/MHz
	VDD_PA=1.8V, num_pulse=2, pulse_width=med, tx_power=min, duty_cycle=100%, phy_rate=20.48MHz		-6.2		dBm/MHz
	VDD_PA=1.8V, num_pulse=3, pulse_width=med, tx_power=max, duty_cycle=100%, phy_rate=20.48MHz		0.0		dBm/MHz
	VDD_PA=1.8V, num_pulse=3, pulse_width=med, tx_power=min, duty_cycle=100%, phy_rate=20.48MHz		-4.7		dBm/MHz

Table 4.7: Radio TX peak 20.48MHz

Parameter 40.96MHz	Test Conditions	MIN	TYP	MAX	UNIT
TX Peak Power Density	VDD_PA=1.8V, num_pulse=1, pulse_width=med, tx_power=max, duty_cycle=100%, phy_rate=40.96MHz		-5.6		dBm/MHz
	VDD_PA=1.8V, num_pulse=1, pulse_width=med, tx_power=min, duty_cycle=100%, phy_rate=40.96MHz		-10.3		dBm/MHz

Table 4.8: Radio TX peak 40.96MHz

4.5.2 Receiver

Parameter	Test Conditions	MIN	TYP	MAX	UNIT
RX Sensitivity	modulation=OOK, payload=32 bytes, fec=3, num_pulse=1, phy_rate=20.48MHz		-81.0		dBm/20 MHz
	modulation=OOK, payload=32 bytes, fec=3, num_pulse=2, phy_rate=20.48MHz		-80.0		dBm/20 MHz
	modulation=OOK, payload=32 bytes, fec=3, num_pulse=3, phy_rate=20.48MHz		-79.5		dBm/20 MHz
	modulation=OOK, payload=32 bytes, fec=3, num_pulse=1, phy_rate=40.96MHz		-79.0		dBm/40 MHz

Table 4.9: Radio Receiver characteristics.

5 Register Description

5.1 Register 0x01

Name	Offset	Width	Access	Reset
XTAL_CLK	0	2	rw	0
CHIP_CLK	2	2	rw	0
RESERVED	4	1	rw	0
RESERVED	5	1	rw	0
CHIP_RATE	6	2	rw	0
OUTIMPED	8	2	rw	0
QSPI	10	2	rw	0
FASTMISO	12	1	rw	0
IRQPOLAR	13	1	rw	1
RESERVED	14	1	rw	0
RESERVED	15	1	rw	0

Table 5.1: Address 0x01

`XTAL_CLK`: Controls which clock source is used for the XTAL clock, and the output on the XTAL_CLK pin.

Value	Internal XTAL Osc	XTAL Clock Source	XTAL_CLK Pin State
0	Enabled	Internal	High-Z
1	Enabled	Internal	Output Internal
2	Disabled	External	Input External
3	Enabled	External	Input External

Table 5.2: XTAL_CLK

`CHIP_CLK`: Controls which clock source is used for the chip clock, and the output on the PLL_CLK pin.

Value	Internal PLL Osc	Chip Clock Source	PLL_CLK Pin State
0	Enabled	Internal	High-Z
1	Enabled	Internal	Output Internal
2	Disabled	External	Input External
3	Enabled	External	Input External

Table 5.3: CHIP_CLK

`CHIP_RATE`: Transceiver PHY chip rate.

Value	Chip Rate (MHz)
0	20.48
1	40.96
2	27.33
3	Reserved

Table 5.4: CHIP_RATE

IRQPOLAR: Interrupt ReQuest output pin polarity. 1: the IRQ pin is active high. 0: the IRQ pin is active low.

FASTMISO: Enables faster SPI response on MISO. 0: MISO changes on falling edge of SCK. 1: MISO changes as soon as data is ready.

OUTIMPED: Strength of digital IO driver. 2-bit value from 0 to 3, 0 is weakest driver, 3 is strongest driver.

QSPI: Operating mode of the SPI/QSPI interface. In mode 3, 6 dummy cycles are discarded before the first read byte following an instruction byte, and 8 dummy cycles are discarded before listening for an instruction byte following a data bytes, or a falling edge on the CSN pin.

Value	Mode	Dummy Cycles	SPI_IO0	SPI_IO1	SPI_IO2	SPI_IO3
0	SPI	N/A	Input	Output	High Z	High Z
1	QSPI	0	I/O	I/O	I/O	I/O
2	QSPI	1	I/O	I/O	I/O	I/O
3	QSPI	6 + 8	I/O	I/O	I/O	I/O

Table 5.5: QSPI

5.2   Register 0x02

Name	Offset	Width	Access	Reset
DLTUNING	0	5	rw	0x10
DL_LAGS	5	1	ro	0
IREFPINE	5	1	wo	0
IREFTUNE	6	6	rw	0x20
VREFTUNE	12	4	rw	0x08

Table 5.6: Address 0x02

IREFTUNE: Adjustment of transceiver reference current. Read from chip NVM and copy in this field.

VREFTUNE: Adjustment of transceiver reference voltage. Read from chip NVM and copy in this field.

DLTUNING: 5-bit tuning of transceiver Delay Line. Adjust until DL_LAGS flips from 1 to 0.

`DL_LAGS`: Read-only bit to determine Delay Line locking. 0: Delay Line is early. 1: Delay Line is late.

5.3   Registers 0x04-0x05

Name	Offset	Width	Access	Reset
CCAONTIME	0	4	rw	0x01
MAXRETRY	4	4	rw	0
TXANYWAY	8	1	rw	1
IGNORPKT	9	1	rw	1
CCAINTERV	10	6	rw	0x03

Table 5.7: Address 0x04

Name	Offset	Width	Access	Reset
CCATHRES	0	7	rw	0x50
RESERVED	7	1	rw	0
RESERVED	8	7	rw	0

Table 5.8: Address 0x05

`MAXRETRY`: Maximum number of Clear Channel Assessment retries, 4-bit value.

`CCAONTIME`: Duration of CCA check, 5-bit value, expressed in number of chip cycles = (`CCAONTIME` + 1) X 8.

`CCAINTERV`: Interval in between CCA checks, 6-bit value, expressed in number of chip cycles = (`CCAINTERV` + 1) X 32.

`IGNORPKT`: Block packet reception during CCA checks. 1: Do not trigger on packet during CCA, 0: Attempt to trigger on packet during CCA. Reserved: default to 1.

`TXANYWAY`: Action to be taken after `MAXRETRY` number of CCA checks have failed. 1: Transmit packet anyway. 0: Do not transmit.

`CCATHRES`: Decision threshold for CCA checks. Values range from 0 to 115, with lower values indicating stronger signals, and higher values indicating weaker signals. Each step represents about 0.5 dB in signal power. Recommended value: 70.

5.4   Register 0x07

Name	Offset	Width	Access	Reset
INTEGGAIN	0	4	rw	0x08
RESERVED	4	3	rw	0x04
RESERVED	7	1	rw	0
RESERVED	8	4	rw	0x0C
LNA_FREQ	12	4	rw	0x08

Table 5.9: Address 0x07

INTEGGAIN: Adjust optimal integrator gain before ADC, 4-bit value. Adjust based on PHY chip rate and number of pulses transmitted per symbol by the transmitter.

Chip Rate (MHz)	TX Pulse Count	INTEGGAIN Value
20.48	1	10
20.48	2	8
20.48	3	7
40.96	1	13
40.96	2	10
40.96	3	9
27.33	1	11
27.33	2	9
27.33	3	8

Table 5.10: INTEGGAIN

LNA_FREQ: Frequency tuning of the receiver LNA, 4-bit value. Adjust based on channel center frequency, codes 0xB to 0xF are reserved.

Value	0x0	0x1	0x2	0x3	0x4	0x5	0x6	0x7	0x8	0x9	0xA
Freq (GHz)	9.09	8.60	8.36	7.95	7.70	7.45	7.21	7.05	6.68	6.43	6.31
Band	222	210	204	194	188	182	176	172	163	157	154

Table 5.11: LNA Frequency Tuning

5.5 Registers 0x08-0x09

Name	Offset	Width	Access	Reset
RXBANDFRE	0	6	rw	0x20
CFG1FREQ	8	6	rw	0x20

Table 5.12: Address 0x08

Name	Offset	Width	Access	Reset
CFG2FREQ	0	6	rw	0x20
CFG3FREQ	8	6	rw	0x20

Table 5.13: Address 0x09

`RXBANDFRE`: VCRO code used during reception, tuning the center frequency band, 6-bit value.

`CFG1FREQ`, `CFG2FREQ`, `CFG3FREQ`: VCRO code used during transmission, tuning the center frequency band, 6-bit value. Separate fields for three pulse configuration.

5.6 Registers 0x0A

Name	Offset	Width	Access	Reset
CFG1WIDTH	0	3	rw	0x04
CFG2WIDTH	4	3	rw	0x04
CFG3WIDTH	8	3	rw	0x04
TX_POWER	12	3	rw	0x04
RANDPULS	15	1	rw	1

Table 5.14: Address 0x0A

`CFG1WIDTH`, `CFG2WIDTH`, `CFG3WIDTH`: Control of transmitted pulse width, 3-bit value. Lower value is shorter pulse (wider TX bandwidth), higher value is longer pulse (narrower TX bandwidth). Separate fields for three pulse configuration.

`TX_POWER`: Amplitude control of transmitted pulse, 3-bit value. Lower value is higher amplitude, higher value is lower amplitude.

`RANDPULS`: Randomizes the phase of each pulse. Reserved: default to 1.

5.7 Registers 0x0B

Name	Offset	Width	Access	Reset
POS1PULSE	0	2	rw	0
POS2PULSE	2	2	rw	0x01
POS3PULSE	4	2	rw	0
POS4PULSE	6	2	rw	0x01
POS5PULSE	8	2	rw	0
POS6PULSE	10	2	rw	0
POS7PULSE	12	2	rw	0
POS9PULSE	14	2	rw	0

Table 5.15: Address 0x0B

`POS1PULSE`, `POS2PULSE`, `POS3PULSE`, `POS4PULSE`, `POS5PULSE`, `POS6PULSE`, `POS7PULSE`, `POS9PULSE`: For pulse positions 1-9 (excluding 8) in each transmitted symbol, `POSxPULSE` is a 2-bit value determining the content of that pulse position:

Value	Pulse Positon Content
0	No Pulse
1	Pulse Configuration 1
2	Pulse Configuration 2
3	Pulse Configuration 3

Table 5.16: `POSxPULSE`

5.8 Registers 0x0C-0xD

Name	Offset	Width	Access	Reset
SLPPERIOD[15-0]	0	16	rw	0x07FF

Table 5.17: Address 0x0C

Name	Offset	Width	Access	Reset
SLPPERIOD[23-16]	0	8	rw	0
PWRUPDLAY	8	8	rw	0

Table 5.18: Address 0x0D

`SLPPERIOD`: Length of sleep period, 24 bits, in number of clock cycles of the sleep clock (chip clock in Idle Sleep, XTAL clock in Deep and Shallow sleep.)

`PWRUPDLAY`: Delay after wakeup, before starting the transmitter or receiver, 8 bits. The duration of delay in number of chip cycles is `PWRUPDLAY` X 8.

5.9   Register 0x0E

Name	Offset	Width	Access	Reset
RESERVED	0	2	rw	0
RESERVED	2	1	rw	0
TIMEOUT	3	13	rw	0

Table 5.19: Address 0x0E

`RXTIMEOUT`: Duration of receiver listening period before timing out, 13 bits. The duration length in number of chip cycles is `RXTIMEOUT` X 8 + 1.

5.10   Register 0x0F

Name	Offset	Width	Access	Reset
SYNTIMEO	0	1	rw	0
SYNRXEND	1	3	rw	0
SYNRXSTA	4	1	rw	0
SYNTXEND	5	1	rw	0
SYNWAKUP	6	1	rw	0
AUTOWAKE	7	1	rw	0
SLPTIMEO	8	1	rw	0
SLPRXEND	9	3	rw	0
SLPCCAFA	12	1	rw	0
SLPTXEND	13	1	rw	0
SLPDEPTH_WA	14	2	rw	0x03

Table 5.20: Address 0x0F

`AUTOWAKE`: Automatically wakeup when sleep period is reached on the active sleep timer. 1: Enabled. 0: Disabled.

`SYNWAKUP`: Reset both chip and XTAL sleep timer on wakeup. 1: Enabled. 0: Disabled.

`SYNTXEND`: Reset both chip and XTAL sleep timer on end of packet transmission. 1: Enabled. 0: Disabled.

`SYNRXEND`: Reset both chip and XTAL sleep timer on end of packet reception, 3 bits. 001: Sync on correct CRC match. 000: Disabled all other reserved.

`SLPDEPTH_WAKEONCE`: Determines sleep level used when going to sleep. If `SLPDEPTH_WAKEONCE` > 0, Wake-Once is activated and only one wakeup event is triggered until `SLP_PERIOD` is overwritten again.

Value	Sleep Level	Sleep Timer	Wake-Once
0	Idle sleep	Chip clock	Off
1	Idle sleep	Chip clock	On
2	Shallow sleep	XTAL clock	On
3	Deep sleep	XTAL clock	On

Table 5.21: SLPDEPTH_WAKEONCE

`SLPTXEND`: Go to sleep after packet transmission. 1: Enabled. 0: Disabled.

`SLPRXEND`: Go to sleep after packet reception, 3 bits. 001: Sync on correct CRC match. 000: Disabled all other reserved.

`SLPTIMEO`: Go to sleep after reception timeout. 1: Enabled. 0: Disabled.

5.11   Register 0x10

Name	Offset	Width	Access	Reset
TIMEOUTE	0	1	wo	1
CRCPASSE	1	1	wo	0
BRDCASTE	2	1	wo	0
ADDRMATE	3	1	wo	0
RXENDE	4	1	wo	1
TXENDE	5	1	wo	1
ARRXENDE	6	1	wo	1
ARTXENDE	7	1	wo	1
WAKEUPE	8	1	wo	0
XOTIMERE	9	1	wo	0
CCAFAILE	10	1	wo	1
BUFTHRES	11	5	wo	0
TIMEOUTI	0	1	ro	1
CRCPASSI	1	1	ro	0
BRDCASTI	2	1	ro	0
ADDRMATI	3	1	ro	0
RXENDI	4	1	ro	1
TXENDI	5	1	ro	1
ARRXENDI	6	1	ro	1
ARTXENDI	7	1	ro	1
WAKEUPI	8	1	ro	0
XOTIMERI	9	1	ro	0
CCAFAILI	10	1	ro	1
BUFLOADI	11	1	ro	1
RXUDRFLI	12	1	ro	1
RXOVRFLI	13	1	ro	1
TXUDRFLI	14	1	ro	1
TXOVRFLI	15	1	ro	1

Table 5.22: Address 0x10

Status flags for interrupts, and enable control for interrupts asserting the IRQ pin.

Flag	IRQ Pin Enable	Raised by Event	Cleared by
TXENDI	TXENDE	End of packet transmission	Register read
RXENDI	RXENDE	End of packet reception	Register read
ARTXENDI	ARTXENDE	End of Auto-Reply transmission	Register read
ARRXENDI	ARRXENDE	End of Auto-Reply reception	Register read
CRCPASS	CRCPASS	Succesful CRC pass	Register read
TIMEOUTI	TIMEOUTE	Timeout during reception	Register read
WAKEUPI	WAKEUPE	Wake up from sleep	Register read
XOTIMERI	XOTIMERE	Sleep period on XTAL timer reached	Register read
CCAFAILI	CCAFAILE	CCA check fail	Register read
ADDRMATI	ADDRMATE	Address field match	Register read
BRDCASTI	BRDCASTE	Broadcast field match	Register read
TXOVRFLI	not DISABUFI	TX FIFO overflow	Reset TX FIFO
RXOVRFLI	not DISABUFI	RX FIFO overflow	Reset RX FIFO
TXUDRFLI	not DISABUFI	TX FIFO underflow	Reset TX FIFO
RXUDRFLI	not DISABUFI	RX FIFO underflow	Reset RX FIFO
BUFLOADI	BUFTHRES > 0	RX FIFO filled above threshold	Pull from RX FIFO until below threshold

Table 5.23: IRQ Control

BUFTHRES: RX FIFO threshold, 5 bits. If the number of bytes in the RX FIFO exceeds BUFTHRES X 8, the BUFLOADI interrupt will be raised.

5.12 Register 0x11

Name	Offset	Width	Access	Reset
RESERVED	0	3	wo	0
RESERVED	3	1	rw	0
RESERVED	4	1	rw	0
RSSIONLY	5	1	rw	0
RPLYTXEN	6	1	rw	0
RADIODIR	7	1	rw	1
RESERVED	8	8	ro	0

Table 5.24: Address 0x11

RADIODIR: Selects transmission or reception mode. 1: Reception. 0: Transmission.

RPLYTXEN: Enables Auto-Reply on packets.

RSSIONLY: Enables energy detection mode on reception, tracking energy with RSSI, without packet reception.

5.13 Register 0x12

Name	Offset	Width	Access	Reset
RSSI	0	7	ro	0
RNSI	8	7	ro	0

Table 5.25: Address 0x12

`RSSI`: Signal strength indicator, latched after syncword detection, 7-bits. Values range from 0 to 115, with lower values indicating stronger signals, and higher values indicating weaker signals. Each step represents about 0.5 dB in signal power.

`RNSI`: Noise strength indicator, 7-bits. Values range from 0 to 115, with lower values indicating stronger noise, and higher values indicating weaker noise. Each step represents about 0.5 dB in noise power.

5.14 Register 0x13-0x14-0x15

Name	Offset	Width	Access	Reset
RXSFDTIME	0	16	ro	0

Table 5.26: Address 0x13

Name	Offset	Width	Access	Reset
TXSFDTIME	0	16	ro	0

Table 5.27: Address 0x14

Name	Offset	Width	Access	Reset
IRQTIME	0	16	ro	0
DISABUFI	0	1	wo	0

Table 5.28: Address 0x15

`RXSFDTIME`: Number of chip cycles between receiver wakeup and syncword detection, 16 bits.

`TXSFDTIME`: Number of chip cycles between transmitter wakeup and syncword transmission, 16 bits.

`IRQTIME`: Number of chip cycles between receiver or transmitter wakeup and assertion of the IRQ pin, 16 bits.

`DISABUFI`: Disables the FIFO underflow and overflow interrupts. 1: Disabled. 0: Enabled.

5.15 Register 0x18

Name	Offset	Width	Access	Reset
FEC_RATE0	0	3	rw	0x03
CHIPCODE0	3	3	rw	0x02
CHIPREPE0	6	2	rw	0
ISIMITIG0	8	2	rw	0
RPLYADD0	10	1	rw	0
EXPECRP0	11	1	rw	0
RESERVED	12	3	rw	0x03
RESERVED	15	1	rw	0

Table 5.29: Address 0x18

`CHIPCODE0`: Modulation used during reception and transmission, 3 bits.

Value	Modulation
0	OOK
1	Reserved
2	1BIT-PPM
3	2BIT-PPM
4	Reserved
5	Reserved
6	Reserved
7	Reserved

Table 5.30: CHIPCODE0

`FEC_RATE0`: Forward Error Coding rate, 3 bits.

Value	FEC Redundancy
0	Disable
1	1.25
2	1.375
3	1.5
4	1.625
5	1.75
6	1.875
7	2.0

Table 5.31: FEC_RATE0

`ISIMITIG0`: Number of ISI mitigation symbols.

Value	Preamble Pauses	Payload Pauses
0	0	0
1	1	0
2	2	1
3	3	2

<div align="center">**Table 5.32: ISIMITIG0**</div>

`RPLYADD0`: Copy address of received packet into address field of auto-reply. 1: Enabled. 0: Disabled.

`EXPECRP0`: Wait for auto-reply after packet transmission. 1: Enabled. 0: Disabled.

5.16   Register 0x2F

Name	Offset	Width	Access	Reset
PREAMBLEN	0	6	rw	0x04
SFDLENGTH	6	2	rw	0x02

<div align="center">**Table 5.33: Address 0x2F**</div>

`SFDLENGTH`: Size of Start of Frame Delimiter field. Recommended value: 0.

Value	SFD Format
0	32-bit OOK
1	16-bit 1BIT-PPM
2	32-bit 1BIT-PPM
3	Reserved

<div align="center">**Table 5.34: SFDLENGTH**</div>

`PREAMBLEN`: Size of preamble synchronization field. The length of the synchronization field in chip clock cycles = `PREAMBLEN` X 8 + 48. Recommended value: 16.

5.17 Registers 0x30-0x31

Name	Offset	Width	Access	Reset
SFDPATTRN[15· 0]	0	16	rw	0xC11D

Table 5.35: Address 0x30

Name	Offset	Width	Access	Reset
SFDPATTRN[31· 16]	0	16	rw	0x5EA6

Table 5.36: Address 0x31

`SFDPATTRN`: Pattern used in Start of Frame Delimiter field.

5.18 Registers 0x32-0x33

Name	Offset	Width	Access	Reset
RESERVED	0	1	rc	1
CRC_POLY[15-1]	1	15	rw	0x313A

Table 5.37: Address 0x32

Name	Offset	Width	Access	Reset
CRC_POLY[30-16]	0	15	rw	0x0372

Table 5.38: Address 0x33

`CRC_POLY`: Cyclic Redundancy Code polynomial. Recommended polynomials are given in table below.

Polynomial	CRC field length (bits)
0x0372313b	25 bits
0x8fcc4ac9	31 bits

Table 5.39: SFDLENGTH

5.19 Register 0x34

Name	Offset	Width	Access	Reset
SAVECRC	0	1	rw	0
SAVESIZE	1	1	rw	0
SAVEADDR	2	1	rw	0
SAVEPHS	3	1	rw	0
SAVETIME	4	1	rw	0
SAVERSSI	5	1	rw	0
PHSFIELD	6	1	rw	0
TIMFIELD	7	1	rw	0
OPTRANGI	8	1	rw	0
SIZESRC	9	1	rw	0
SIZEPARI	10	1	rw	0
SIZEHDR	11	1	rw	0
RETRYHDR	12	1	rw	0
ADDRLEN	13	1	rw	0
ADDRFIELD	14	2	rw	0

Table 5.40: Address 0x34

Several packet fields are additionally enabled:

ADDRFIELD: Enables an address field that can be used for address filtering. Control whether address matching gates packet reception, and/or auto reply transmission/

Value	Packet Address Field	Filter Packet Reception	Filter Auto-Reply Transmission
0	Disabled	No	No
1	Enabled	No	No
2	Enabled	No	Yes
3	Enabled	Yes	Yes

Table 5.41: ADDRFIELD

ADDRLEN: Size of the address field. 1: 16 bits. 0: 8 bits.

SIZEHDR: Adds an 8-bit payload size field to the packet during transmission, which is used during reception to determine the payload length. 1: Enabled. 0: Disabled.

SIZEPARI: Adds a 5-bit parity field to the payload size field. 1: Enable. 0: Disable.

SIZESRC: Selects what is used as the payload size for packet transmission. 1: Use TXPKTSIZE. 0: Use number of bytes in TX FIFO.

OPTRANGI: Reserved, set to 0.

Several of the packet fields can be automatically pushed into the RX FIFO during packet reception, in the following order:

SAVETIME: The RXSFDTIME is pushed to the RX FIFO. 1: Enabled. 0: Disabled.

SAVECHRE: The channel impulse response is pushed to the RX FIFO. 1: Enabled. 0: Disabled.

SAVERSSI: The RSSI is pushed to the RX FIFO. 1: Enabled. 0: Disabled.

SAVEADDR: The address field is pushed to the RX FIFO. 1: Enabled. 0: Disabled.

RETRYHDR: The CCA retry counter field is added as a packet field during transmission, and pushed to the RX FIFO during reception. 1: Enabled. 0: Disabled.

SAVESIZE: The payload size field is pushed to the RX FIFO. 1: Enabled. 0: Disabled.

If there is a payload field in the packet, it is saved at this position in the RX FIFO. Afterwards, the following packet fields can be pushed to the RX FIFO:

TIMFIELD: Include RXSFDTIME field in the packet during transmission. 1: Enabled. 0: Disabled.

PHSFIELD: Include RXOFFSET field in the packet during transmission. 1: Enabled. 0: Disabled.

SAVECRC: Save the CRC remainder mismatch pattern to the RX FIFO. 1: Enabled. 0: Disabled.

5.20   Registers 0x35-0x36

Name	Offset	Width	Access	Reset
RXADDRESS	0	16	rw	0xADDB

Table 5.42: Address 0x35

Name	Offset	Width	Access	Reset
TXADDRESS	0	16	rw	0xADDA

Table 5.43: Address 0x36

RXADDRESS: Address used to do address field matching during packet reception.

TXADDRESS: Address used in address field during packet transmission.

5.21 Registers 0x37

Name	Offset	Width	Access	Reset
RXPKTSIZE	0	8	rw	0x10
TXPKTSIZE	8	8	rw	0x10

Table 5.44: Address 0x37

RXPKTSIZE: Size in bytes of payload field read during reception. If SIZESRC is 0, this register determines the maximum size read.

TXPKTSIZE: Size in bytes of payload field during transmission.

5.22 Registers 0x38

Name	Offset	Width	Access	Reset
TXBUFFER	0	8	wo	0
RXBUFFER	0	8	ro	0

Table 5.45: Address 0x38

TXBUFFER: Writing to this register pushes a byte into the TX FIFO.

RXBUFFER: Reading from this register pops a byte from the RX FIFO.

5.23 Registers 0x39-0x3A

Name	Offset	Width	Access	Reset
RXBUFLOAD	0	8	ro	0

Table 5.46: Address 0x39

Name	Offset	Width	Access	Reset
TXBUFLOAD	0	8	ro	0

Table 5.47: Address 0x3A

RXBUFLOAD: Number of bytes in the RX FIFO.

TXBUFLOAD: Number of bytes in the TX FIFO.

5.24 Registers 0x3B

Name	Offset	Width	Access	Reset
SLEEP	0	1	wo	1
INITIMER	1	1	wo	1
FLUSHRX	2	1	wo	1
FLUSHTX	3	1	wo	1
STARTTX	4	1	wo	0
RESERVED	5	1	wo	0
RESERVED	6	1	wo	0
AUTOTX	7	1	rw	0
TXRETRIES	0	4	ro	0

Table 5.48: Address 0x3B

Writing to this register starts the following actions:

AUTOTX: Start transmission every time after waking up from sleep.

STARTTX: Start transmission once after waking up from sleep.

FLUSHTX: Empty and reset the TX FIFO.

FLUSHRX: Empty and reset the RX FIFO.

INITIMER: Reset both XTAL and chip sleep timers.

SLEEP: Controls sleep.

Value	Description
0	Wakeup directly from sleep
1	Go to sleep when modem is no busy transmitting or receiving.

Table 5.49: SLEEP

TXRETRIES: Number of CCA retries received from CCA retry counter field in packet.

5.25 Registers 0x3C

Name	Offset	Width	Access	Reset
REF_EN	0	1	ro	0
PLL_EN	1	1	ro	0
DCDC_EN	2	1	ro	0
PROC_ON	3	1	ro	0
AWAKE	4	1	ro	0
RX_EN	5	1	ro	0
TX_EN	6	1	ro	0
INFRAME	7	1	ro	0

Table 5.50: Address 0x3C

INFRAME: Modem state of reception or transmission of packet. 1: Packet transmission or reception is ongoing, after the SFD. 0: Otherwise.

TX_EN: Transmitter power status. 1: Enabled. 0: Disabled.

RX_EN: Receiver power status. 1: Enabled. 0: Disabled.

AWAKE: Modem is awake. 1: Yes. 0: No.

PROC_ON: Modem power status. 1: Enabled. 0: Disabled.

DCDC_EN: DC-DC Converter power status. 1: Enabled. 0: Disabled.

PLL_EN: PLL power status. 1: Enabled. 0: Disabled.

REF_EN: Bias generator power status. 1: Enabled. 0: Disabled.

5.26 Registers 0x3E

Name	Offset	Width	Access	Reset
COUNTCODE	0	6	wo	0
CODEFREQ	0	8	ro	0

Table 5.51: Address 0x3E

COUNTCODE: VCRO code to be calibrated, 6-bit value. Write once to this register to start calibration.

CODEFREQ: VCRO frequency after calibration, 8-bit value. Frequency is (CODEFREQ + 256) X 20.48 MHz.

5.27 Registers 0x3F

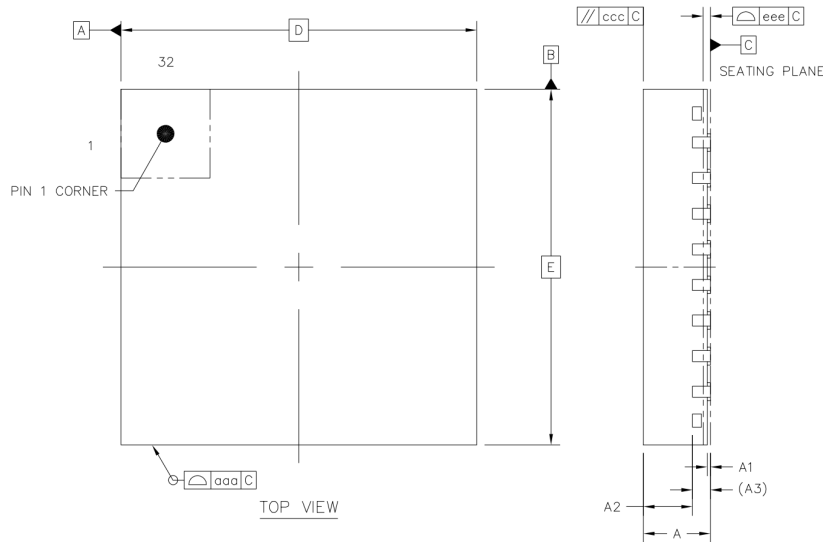| Name	Offset	Width	Access	Reset
ROM_ADDR	0	7	wo	0
ROMPWRSW	7	1	wo	0
ROM_BYTE	0	8	ro	0

Table 5.52: Address 0x3F

ROMPWRSW: Power switch for Non-Volatile Memory (NVM). 1: Enabled. 0: Disabled.

ROM_ADDR: Address of NVM byte to be read, 7-bit value.

ROM_BYTE: Content of NVM at address location, 8-bit value.

6 Package Outline

TOP VIEW

SEATING PLANE

	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	0.7	0.75	0.8
STAND OFF	A1	0	0.035	0.05
MOLD THICKNESS	A2	---	0.55	---
L/F THICKNESS	A3		0.203 REF	
LEAD WIDTH	b	0.15	0.2	0.25
BODY SIZE X	D		4 BSC	
BODY SIZE Y	E		4 BSC	
LEAD PITCH	e		0.4 BSC	
EP SIZE X	J	2.6	2.7	2.8
EP SIZE Y	K	2.6	2.7	2.8
LEAD LENGTH	L	0.25	0.3	0.35
	L1	0.2	0.3	0.35
PACKAGE EDGE TOLERANCE	aaa		0.1	
LEAD OFFSET	bbb		0.1	
MOLD FLATNESS	ccc		0.1	
COPLANARITY	eee		0.08	
EXPOSED PAD OFFSET	fff		0.1	
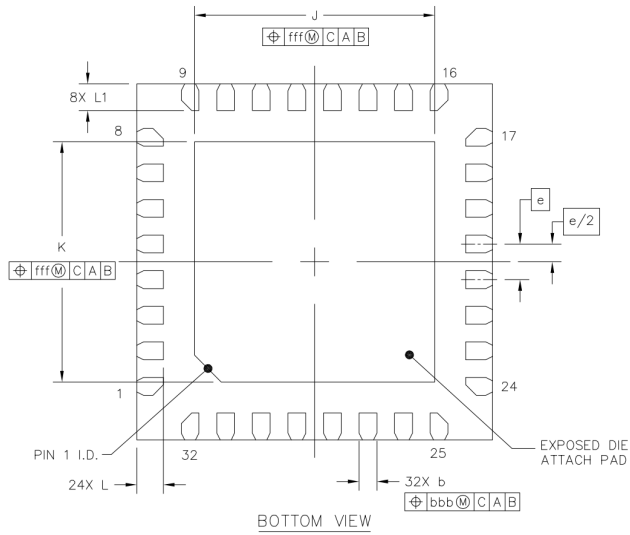
NOTES

1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.
2.0 TOTAL THICKNESS NOT INCLUDE SAW BURR.

BOTTOM VIEW

7   Recommended Footprint

Non solder mask defined pads (NSMD) recommended
Dimensions are in mm

Figure 7.1: Footprint

8   Part Order information

Part Number	Package	Size	Qty
SR1120AA-4Q32-CT	QFN32	4X4	1
SR1120AA-4Q32-TR	QFN32	4X4	5000

Table 8.1: Part order information.

9 Revision

9.1 Revision Table

Revision	Date	Section	Description
1.4	2025/03	1	Minor text change
1.3.3	2025/02	1,6	added data in table dc characteristics. Precise Fc.
1.3	2024/10	6	Added register file description.
1.2	2024/10	4	Updated application reference circuit, fix text.
1.1	2024/09	2,3,4	Minor text fixes, pinout, Added table in 3.2. Added table 4.1, Fix tablenote 4.2. Change min/max representation for tx_power in tables
1.0	2024/03	-	Initial release

Table 9.1: Revisions

10 Notice