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PREMIUM QUALITY Semiconductor

JIANGSU POPPULA SEMICONDUCTOR CO., LTD

QUOTATION

Date : 2023/12/27

Attn to: Arnyl Bill to: Taiwan Semi Ship to :Taiwan Semi

Dear Arnyl

We are pleased to provide you the following quotations per your request.

Looking forward to serving you in the near future.

Item No	Customer Part No.	Package	Description or Equivalent Product	CLC/Kpcs (in USD)	MOQ/Device (Kpcs)	Remark
1	BC846	DFN1110-3	*1x Chips *2x Au 0.8mil wire	7.5	No. of chips in 1 wafer	
2	TQM2N7002K	DFN1110-3	*1x Chips *2x Au 0.8mil wire	7.5	No. of chips in 1 wafer	
3	TESDA24VB30P2	DFN1110-3	*4x Chips(2 Twin Die ,2 Single Die) *2x Au 0.8mil wire	8.7	No. of chips in 1 wafer	
4	BAV99	DFN1110-3	*2x Chips *2x Au 0.8mil wire	8.1	No. of chips in 1 wafer	
5	BC817RA	DFN1412-6	*2x Chips *4x Au 0.8mil wire	11.4	No. of chips in 1 wafer	
6	BAS16	DFN1006-2L	*1x Chips *1x Au 0.8mil wire	6.6	No. of chips in 1 wafer	*AUTOMOTIVE GRADE *CLC is based on the Au market price of USD1,900/ounce and will be reviewed for ups or down adjustment if the Au market price fluctuates over 10%.
7	BC846	DFN1110-3	*1x Chips *2x Au 1mil wire	8.0	No. of chips in 1 wafer	
8	TQM2N7002K	DFN1110-3	*1x Chips *2x Au1mil wire	8.0	No. of chips in 1 wafer	
9	TESDA24VB30P2	DFN1110-3	*4x Chips(2 Twin Die ,2 Single Die) *2x Au 1mil wire	9.3	No. of chips in 1 wafer	
10	BAV99	DFN1110-3	*2x Chips *2x Au 1mil wire	8.6	No. of chips in 1 wafer	
11	BC817RA	DFN1412-6	*2x Chips *4x Au 1mil wire	12.4	No. of chips in 1 wafer	
12	BAS16	DFN1006-2L	*1x Chips *1x Au 1mil wire	6.9	No. of chips in 1 wafer	

NOTE : includes wafer sawing, die & wire bonding, molding, Sn plating, trim & form, TMTR & final pack.

Remarks:

Ordering Quantity	: Multiple of MOQ per device
Shipment	: Surface
Trade Terms	: FOB Shanghai
Payment	: Following month after the receipt of the goods
Lead Time	: 4-6 Weeks
Origin	: China
Validity	: Valid until the next date of negotiation

Standard Packaging

*Follow taiwan Semi Packaging Specification

*Customer to provide free of charge wafers with EGD>99% per wafer DDP Siyang Suqian City Jiangsu.
*Output finished goods from wafers with EGD.99% will be 95% or above.
*Above CLC are based on using Poppula's BOM. processes and speciticabons except chips & finished goods labels.

Prepared By: **Approved By:**

2023.12.27
Hardcopy is signed & filed internally.
No signature in electronic file.
JIANGSU POPPULA SEMICONDUCTOR CO., LTD

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No signature in electronic file.