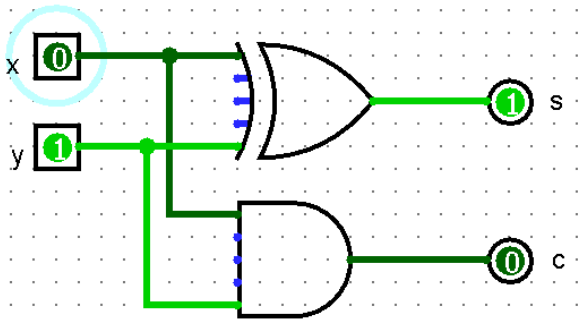
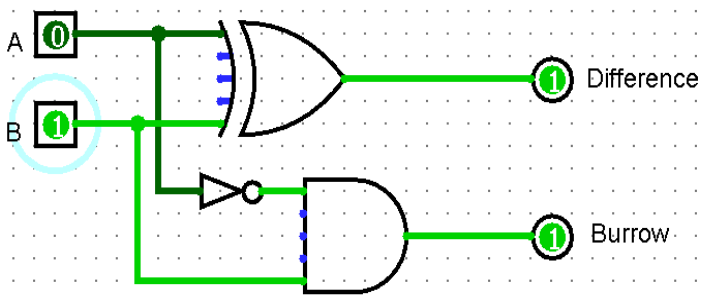
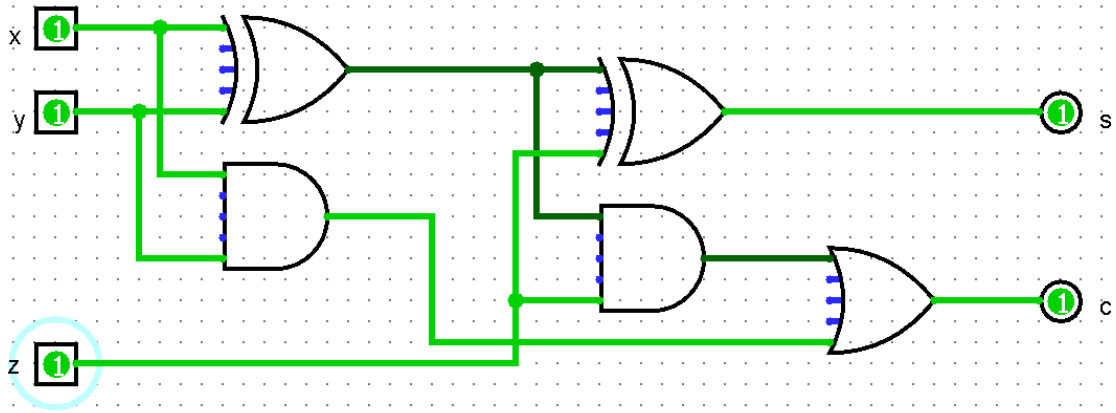


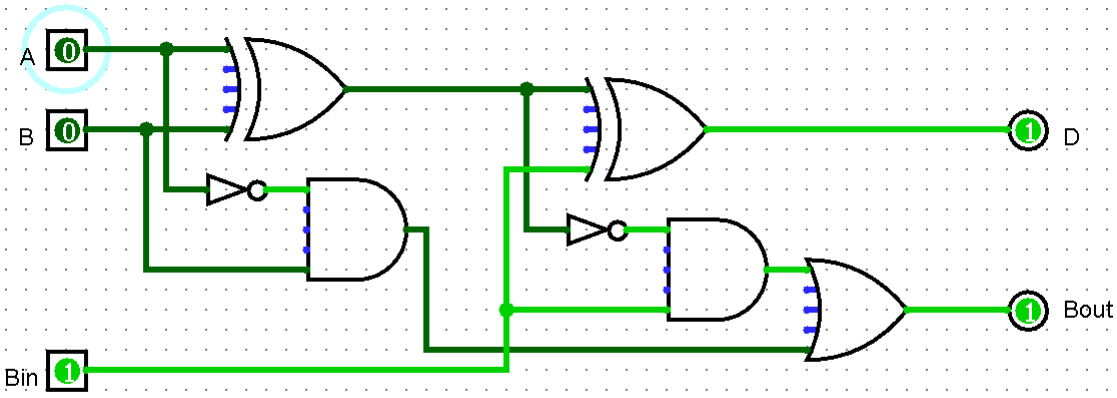
Verification of Inputs for Half Adder



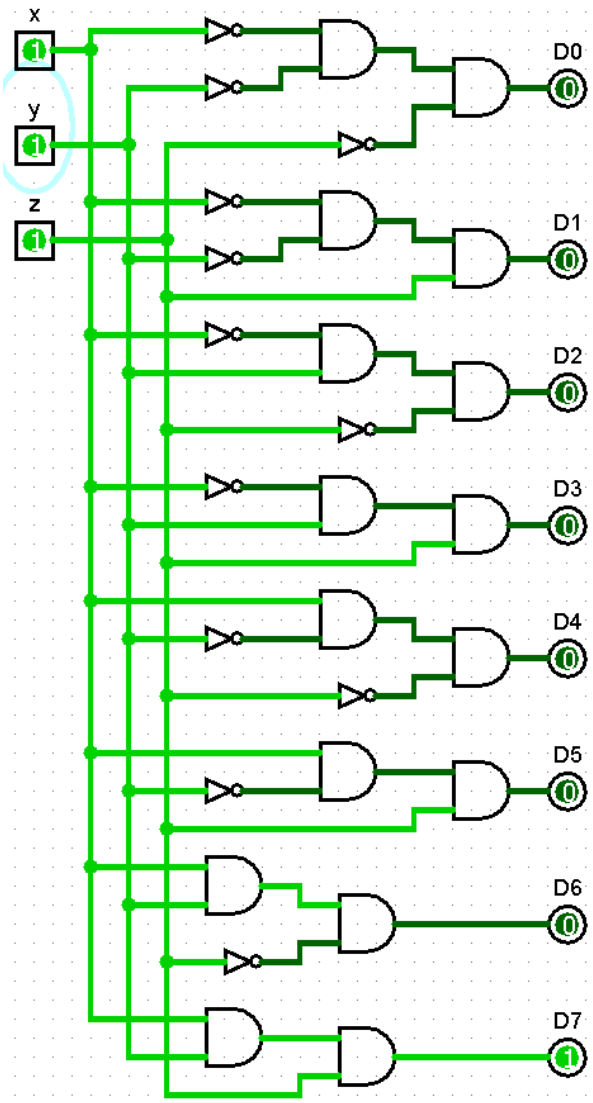
Verification of Inputs for Half Subtractor



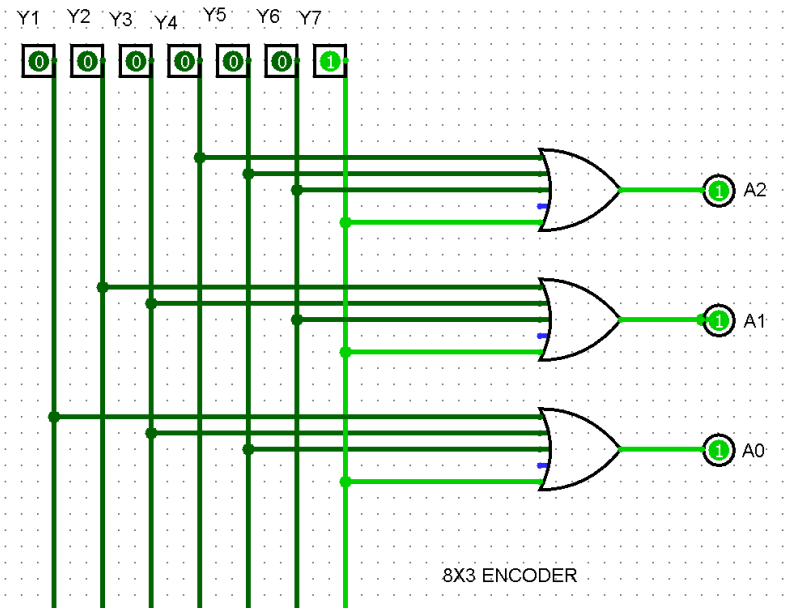
Verification of Inputs for Full Adder

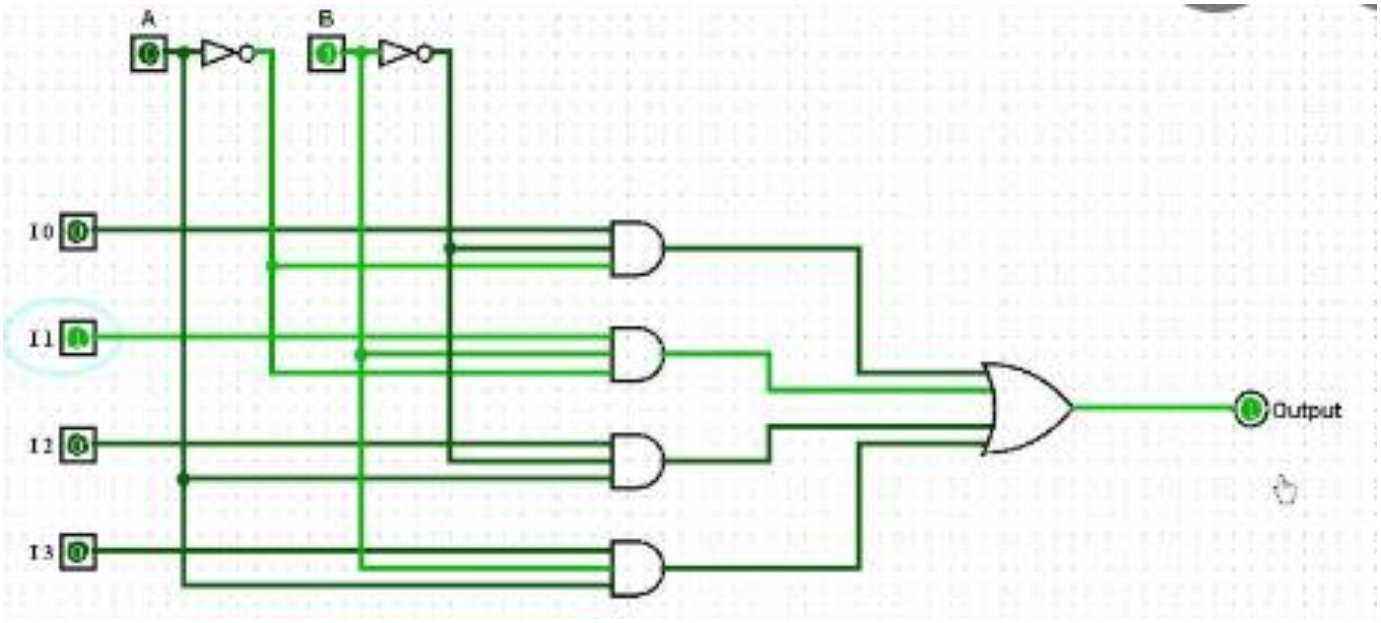


Verification of Inputs for Full Subtractor

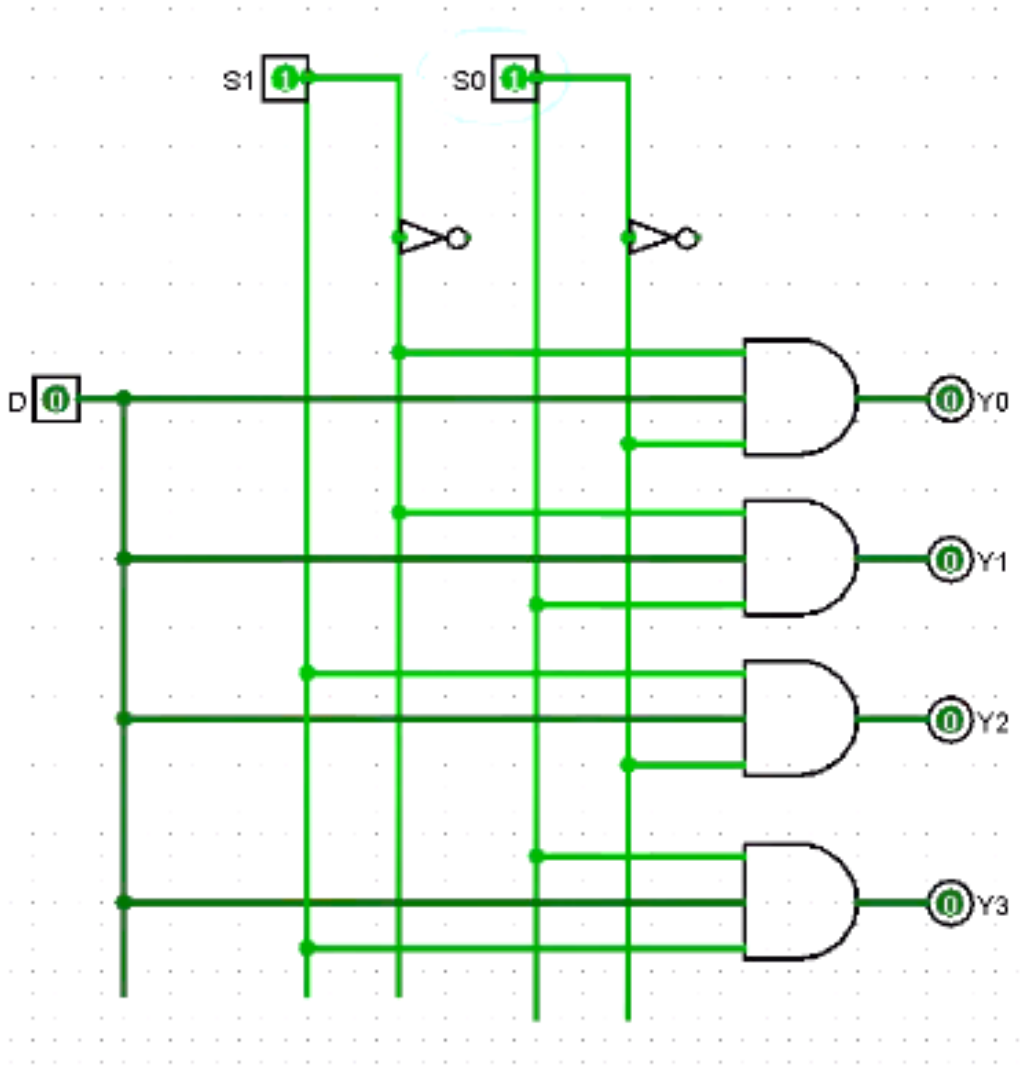


3 - 8 Decoder

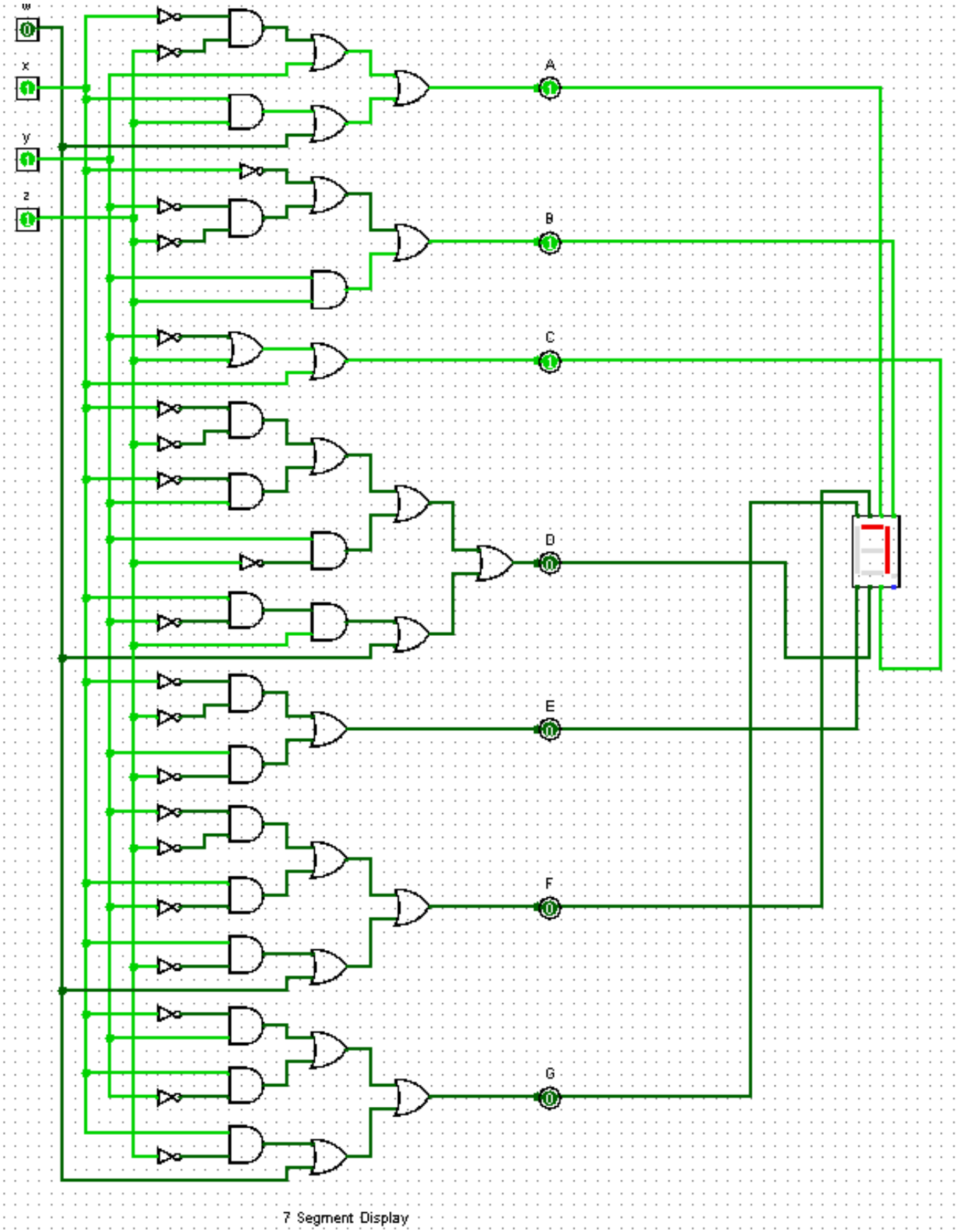


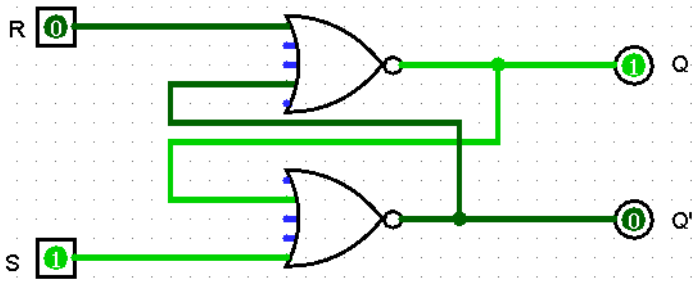


4-1 Mux

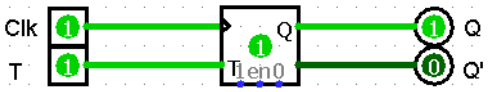


1-4 Demux

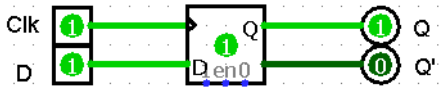

w
x
y
z
A
B
C
D
E
F
G
7 Segment Display



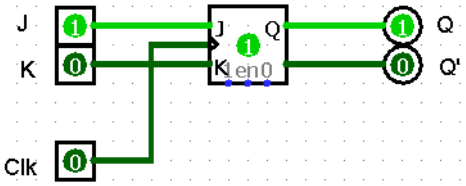
RS Flipflop



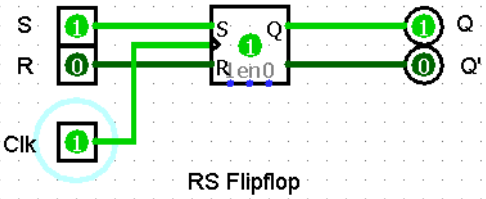
T Flipflop



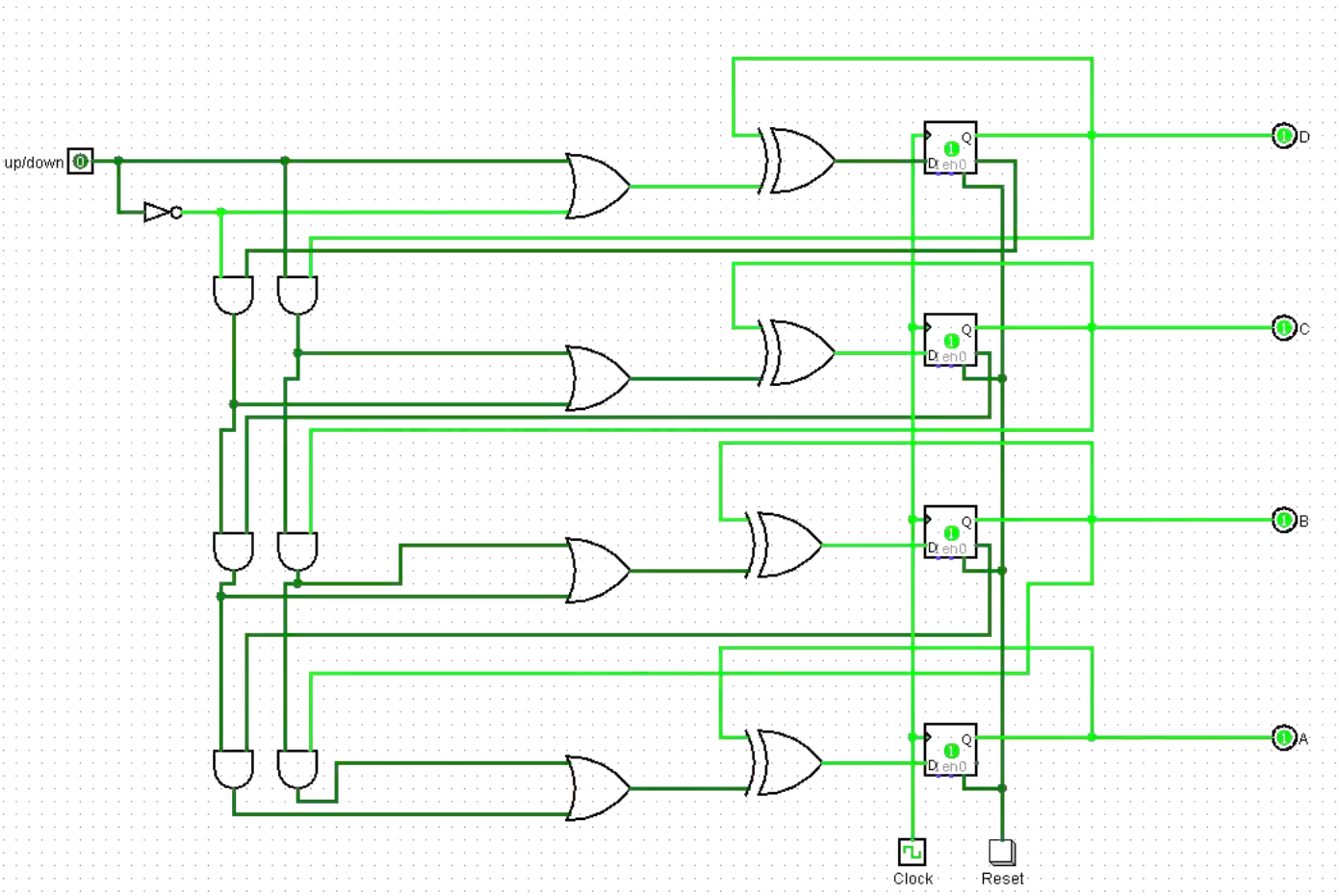
D Flipflop



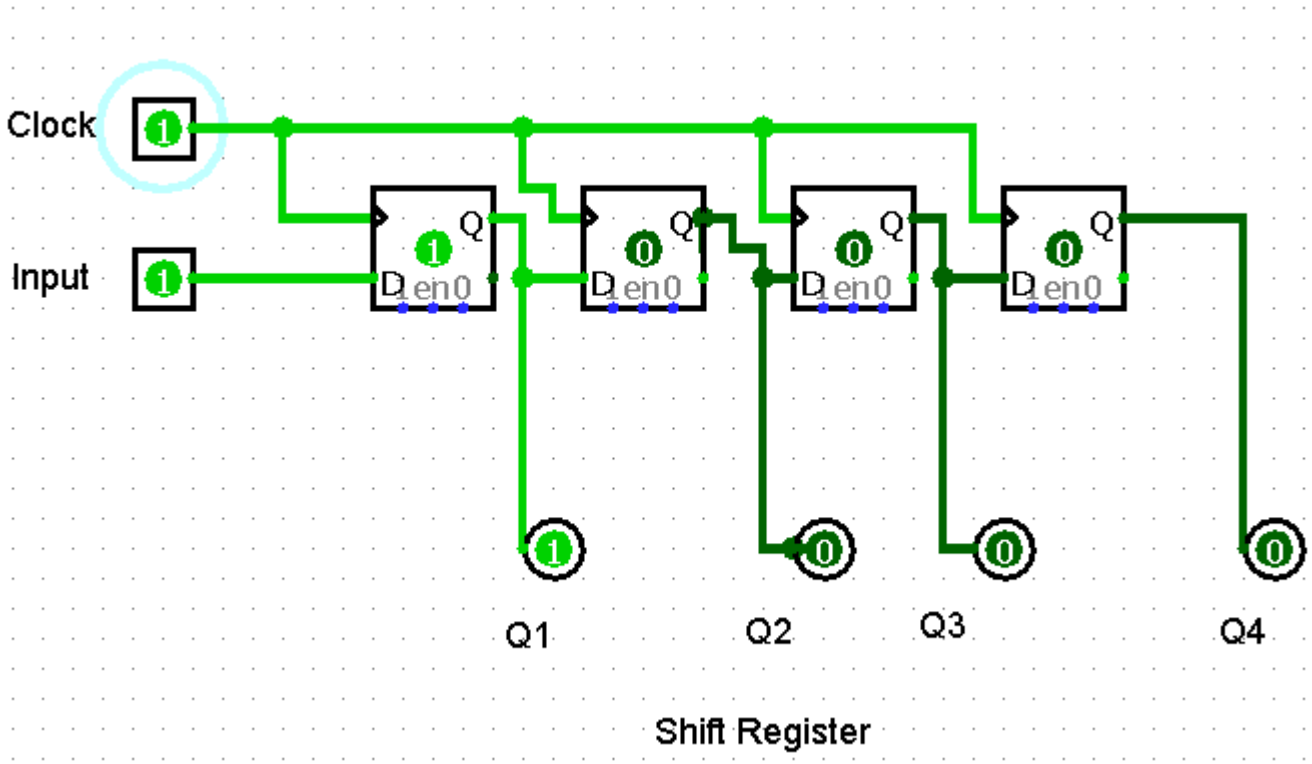
JK Flipflop



RS Flipflop



Up/Down Counter


Clock
Input
1
1
Q
D en 0
1
0
Q
D en 0
0
0
Q
D en 0
0
0
Q
D en 0
0
1
0
0
0
Q1
Q2
Q3
Q4
Shift Register