PHYSICS PRACTICAL

Name of Students:

Exp. No. S.N.	Name of experiment	Initial	Final
1.	TO DETERMINE THE MOMENT OF INERTIA OF GIVEN FLYWHEEL		
2.	TO DESIGN AND STUDY THE LOGIC GATES: NOT, OR, NOR USING TTL		
3.	TO DETERMINE THE MOMENT OF INERTIA OF GIVEN BODY BY USING TORTIONAL PENDULUM		
4.	TO DESIGN AND STUDY THE SERIES LCR CIRCUITS FOR FINDING RESONANCE FREQUENCY AND QUALITY FACTOR OF THE ELEMENTS		
5.	TO DESIGN AND STUDY THE LOGIC GATES: NOT, AND, NAND USING TTL		
6.	TO CONSTRUCT AND TO STUDY THE CHARACTERISTICS OF R-S FLIPFLOP BY USING 7400 OR 7402 IC		

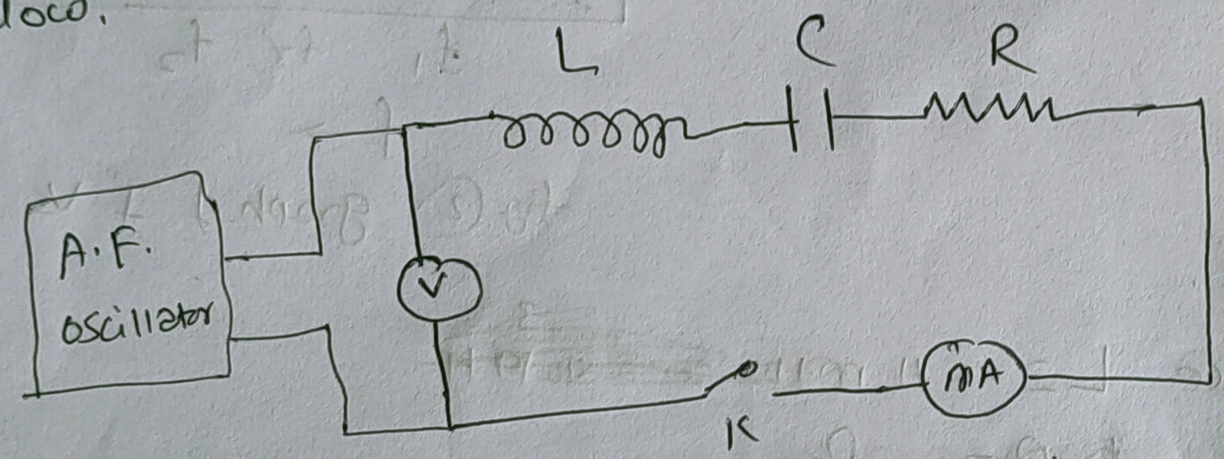
ble for determination of diameter of wire:

	M.S.R. x	C.S.R. a	Value of CSR $y = a \times L.C.$	Total diameter $x+y$	mean diameter	Corrected diameter (d)
1						
2						
3						

Series LCR Circuit

Apparatus Required: An inductor, capacitor, resistor Connecting wires, An audio frequency oscillator (10 Hz - 10 KHz) one way key., voltmeter, Ammeter.

Theory: When the resistor (R), inductor (L) & capacitor (C) are connected in series with a source of emf. 'E', the circuit is called series resonance circuit as shown in fig. below.



fig① Series LCR Circuit.

Under certain conditions, the voltage and current are in phase, even though the circuit consists of L, C & R and the circuit behaves as a pure resistor. This phenomenon is called resonance. This occurs at single frequency known as resonant frequency (f_r). At this frequency, the capacitive reactance ($X_C = \frac{1}{\omega C}$) and inductive reactance ($X_L = \omega L$) are equal and opposite. i.e. $\frac{1}{\omega C} = \omega L \Rightarrow \omega^2 = \frac{1}{LC}$

$$\omega = \frac{1}{\sqrt{LC}} \Rightarrow 2\pi f_r = \frac{1}{\sqrt{LC}} \Rightarrow \boxed{f_r = \frac{1}{2\pi\sqrt{LC}}} \quad -(1)$$

The quality factor of series LCR circuit is given by $\boxed{Q = 2\pi \frac{f_r}{f_2 - f_1}}$ -(2) where f_2 & f_1 are the values of frequency above and below the resonant frequency for which the current in the

S.N.	Value of CSR $y = 2 \times L.C.$	Total diameter $x+y$	mean diameter	diameter (d)
2				

m

circuit is $\frac{I_r}{\sqrt{2}} = 0.707\, I_r$, where '$I_r$' is current at resonance which is obtained by plotting a graph of current (I) versus frequency (f) as shown in fig. below.

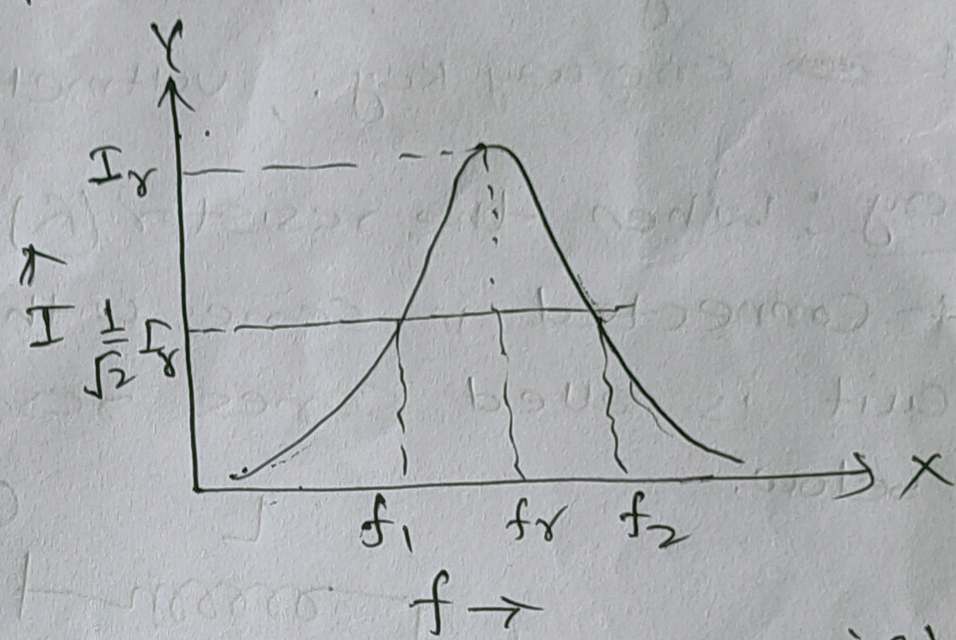


fig ② graph of 'I' vs 'f'.

Observation:

Inductance L = --- H

Resistance R = --- Ω

Capacitance C = --- F

observation table for measurement of current

S.N.	frequency (f) in KHz	current in mA		
		R_1 = --- Ω	R_2 = --- Ω	R_3 = --- Ω

Calculation:

TORSIONAL PENDULUM

(1)

Apparatus Required: Disk, wire, Ring, stopwatch, screw gauge vernier callipers

Theory: Torsional pendulum is a heavy circular disc suspended from one end of a fine wire attached to its centre, the other ends of the wire is fixed in a torsional head. When the disk is turned in a horizontal plane so as to twist the wire and then released, it executes torsional pendulum. The time period of the torsional vibration is given by

$$T = 2\pi\sqrt{\frac{I}{C}} \quad — (1)$$

where, I be the MI of disk about the wire an axis and 'C' is Couple per unit angle of twist or torsional Constant. given by

$$C = \frac{\pi \eta r^4}{2l} \quad — (2)$$

where 'η' is modulus of rigidity of wire
'r' is radius of wire
'l' is length of wire

The whole system (Disk and Ring) oscillates with time Period

$$T_1 = 2\pi\sqrt{\frac{(I+I_1)}{C}} \quad — (2)$$

Where 'I_1' is moment of inertia of Ring.

Now,

$$T_1^2 - T^2 = 4\pi^2\left(\frac{I+I_1}{C}\right) - 4\pi^2\frac{I}{C} = \frac{4\pi^2 I_1}{C}$$

$$\Rightarrow \boxed{I_1 = \frac{C(T_1^2 - T^2)}{4\pi^2}}$$

$$\therefore I_1 = \frac{\pi \eta r^4}{2l}\left(\frac{T_1^2 - T^2}{4\pi^2}\right) \Rightarrow \boxed{I_1 = \frac{\eta r^4 (T_1^2 - T^2)}{8\pi l}}$$

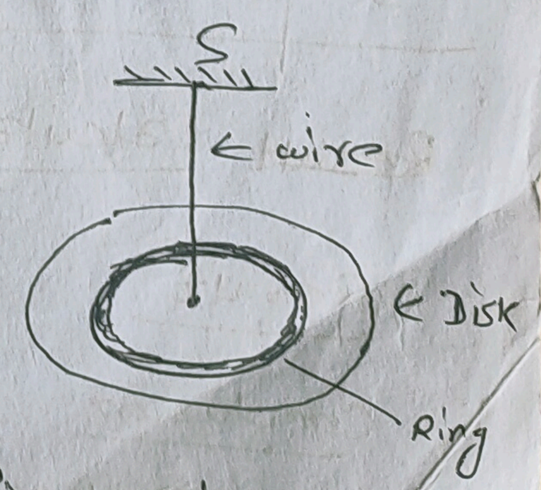


fig. Torsional pendulum

$\frac{1}{\sqrt{LC}} \Rightarrow 2\pi f_r$

The Quality given by

$$\boxed{Q = 2\pi \frac{f_r}{f_2 - f_1}} \quad -(2)$$

the resonant frequency f

(2)

(torsional pendulum)

observations:

Least Count of screw gauge L.C. $= \frac{\text{Pitch}}{N} = \frac{P}{N} = \text{---}$ mm

length of wire $(l) = \text{---}$ m

value of modulus of rigidity of wire $\eta = \text{----}$ N/m^2

Table for determination of diameter of wire:

S.N.	M.S.R. x	C.S.R. a	value of CSR $y = a \times L.C.$	Total diameter $x+y$	mean diameter	Corrected diameter (d)
1						
2						
3						
4						
5						

radius of wire $r = \frac{d}{2} = \text{---}$ m

Table for determination of time period

S.N.	Time for 10 vibration (without ring t	Time period $T = \frac{t}{10}$	Time for 20 vibration with ring t_1	mean Time period $T_1 = \frac{t_1}{10}$	$(T_1^2 - T^2)$	mean $T_1^2 - T^2$
1						
2						
3						
4						
5						

Result calculation:

Result:

Conclusion

precautions

$$\therefore I_1 = \frac{\pi \eta r^4}{2l}\left(\frac{T_1^2 - T^2}{4\pi^2}\right) \Rightarrow \boxed{I = \frac{\eta r^4 (T_1^2 - T^2)}{T l}}$$

FLYWHEEL

Apparatus Required:

A flywheel, a few different masses and a mass provided with a hook, A strong and thin ring, stop watch, meter scale, A vernier callipers and a piece of chalk.

Theory:

A flywheel is simply a heavy wheel with a long axle supported in bearings such that it can rest in any position. C.G. lies on the axis of rotation. The moment of inertia of flywheel about axis of rotation is given by

$$I = \frac{2mgh - mr^2\omega^2}{\omega^2\left(1 + \frac{n}{n_1}\right)}$$

Where, 'm' is the mass attached to axle of wheel

'h' is the height through which the mass has fallen.

'r' is the radius of axle.

$\omega = \frac{4\pi n_1}{t}$ is angular velocity of wheel

n_1 is no. of revolution made by wheel before comming to rest

't' is time taken by wheel before comming to rest.

'n' is no. of turn of cord on the wheel which is also no. of revolution the wheel makes during the descent of mass 'm'.

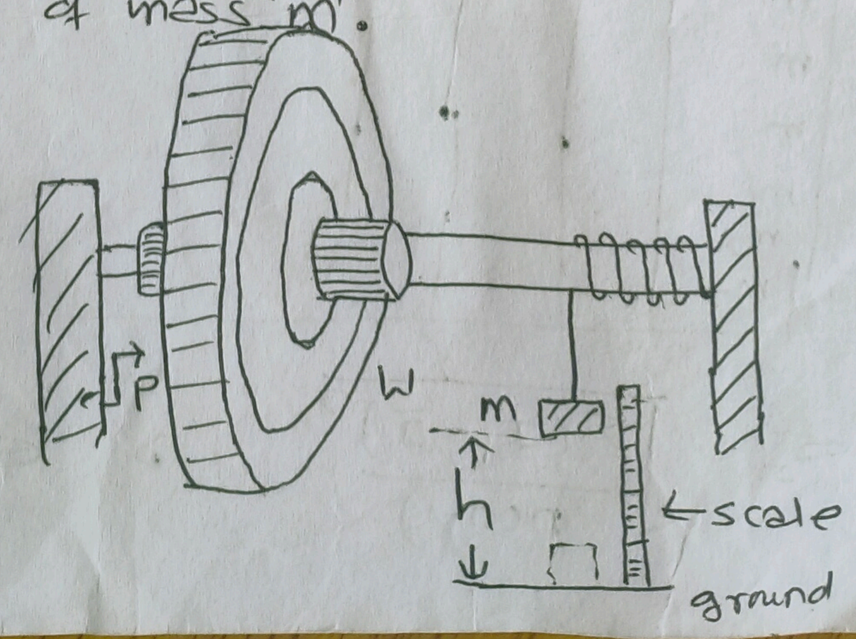


fig. flywheel

$$\therefore I_1 = \frac{\pi \eta r^4}{2l}\left(\frac{T_1^2 - T^2}{4\pi^2}\right) \Rightarrow \boxed{I_1 = \frac{\eta r^4 (T_1^2 - T^2)}{8\pi l}}$$

fig. Tor

Final

Flywheel

4

observations:

vernier Constant of vernier calliper (V.C.) = ---- cm

Least Count of scale = --- cm

observation table for determination of radius of axle:

No. of obs.	M.S.R. 'x'	V.S.R. (V)	value of V $y = V \times V.C.$	Total Diameter $D' = x+y$	mean diameter D
1					
2					
3					

$\therefore$ Radius of axle $r = \frac{D}{2}$ = ------ m

Circumference of wheel C = --- cm

Table for Determination of M.I.

S.N.	height h in metre	mass 'm' in kg	No. of turn 'n'	No. of Complete revolution x	Distance of chalk from pointer d in cm	fraction of revolution $y = \frac{d}{C}$	Total no. of rev. $n = (x+y)$	time taken t
	h_1 = --	m_1 = --						

~~mean~~ -

~~mean~~ -- I_1 = ---- $kg\,m^2$

Similar for I_2 = --- $kg\,m^2$

& I_3 = --- $kg\,m^2$

~~mean n~~	~~mean 't' in sec~~	~~$\omega = \frac{4\pi n}{t}$~~

~~Table for Determination of Angular Acceleration~~

S.N.	no. of turn n	mass in kg	time taken for 'n' revolution (t) i	ii	iii	mean	$\alpha = \frac{4\pi n}{t^2}$	mean α
	n_1	m						
	n_2	m						
	n_3	m						
	n	m_1						
	n	m_2						
	n	m_3						

Result:

Conclusion:

Precautions:

Error $\sigma_I = \sqrt{\frac{\Sigma(I_i - \bar{I})^2}{n(n-1)}}$ & $\sigma_\alpha = \sqrt{\frac{\Sigma(\alpha_i - \bar{\alpha})^2}{n(n-1)}}$

Experiment No.4(b) Date:

TO CONSTRUCT AND TO STUDY THE CHARACTERISTICS OF R-S FLIPFLOP

APPARATUS REQUIRED:

Power supply 5V, IC 7400, 7486, 7402, bread board, connecting wires, multimeter.

THEORY:

RS FLIP-FLOP

A RS flip-flop consists of two input R and S with two output Q and $\bar{Q}$.

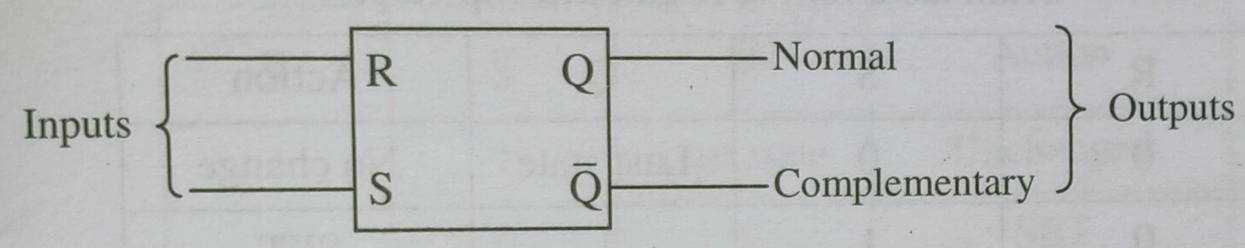


Figure: Logic symbol of RS flip-flop

We can construct RS flip-flop by using NOR gates and NAND gates.

A. RS flip-flop using NOR gate

RS flip-flop can be constructed by cross coupling of two NOR gates as shown in figure 1.

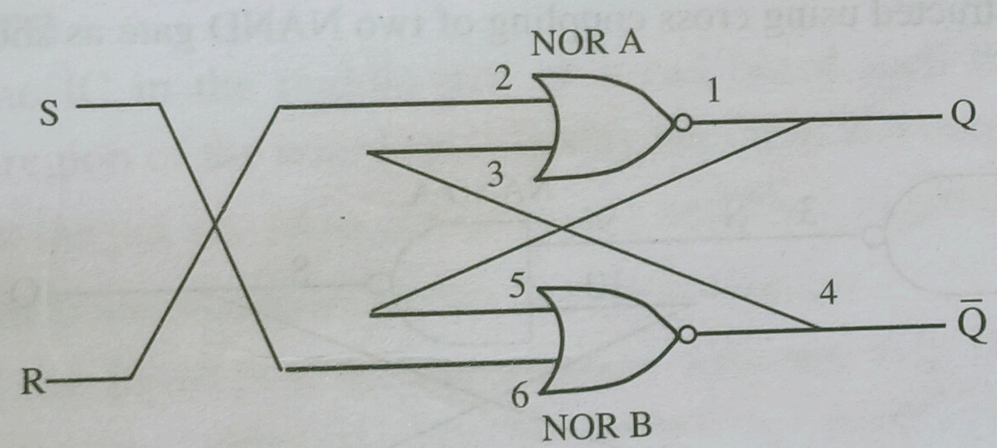


Figure 1: Circuit diagram for RS flip-flop using NOR gates

There are two inputs to the flip-flop defined as R and S and has two outputs Q and $\bar{Q}$.

The input/output possibilities for this RS flip-flop are discussed below:

1. When R = 0 and S = 0

Since the NOR gate is high sensitive. So a '0' at the input of a NOR gate has no effect on its output, the flip-flop simply remains in its present state: that is, Q remains unchanged.

2. When R = 0 and S = 1

In this input condition, the output of NOR gate B is low. Both inputs to NOR gate A are now low, so the output must be high. Thus a 1 at the S input is said to SET the flip-flop, and it switches to the stable state where Q = 1 (or $\bar{Q} = 0$)

3. When R = 1 and S = 0

This condition forces the output of NOR gate, a low, and since both inputs to NOR gate B are low, the output must be high. Thus a '1' at the R input is said to RESET the flip-flop, and it switches to the stable state where Q = 0 (or $\bar{Q} = 1$).

4. When R = 1 and S = 1

This is a forbidden condition, as it forces the outputs of both NOR gates to the low state. Which violates the basic definition of a flip-flop that requires Q and $\bar{Q}$ be complement to each other. If this condition is for some reason imposed, the resulting state of Q is not predictable.

Truth table for NOR-gate RS flip-flop.

R	S	Q	Action
0	0	Last state	No change
0	1	1	SET
1	0	0	RESET
1	1	?	Forbidden

B. RS flip-flop using NAND gate

RS flip-flop also can be constructed using cross coupling of two NAND gate as shown in figure 1.

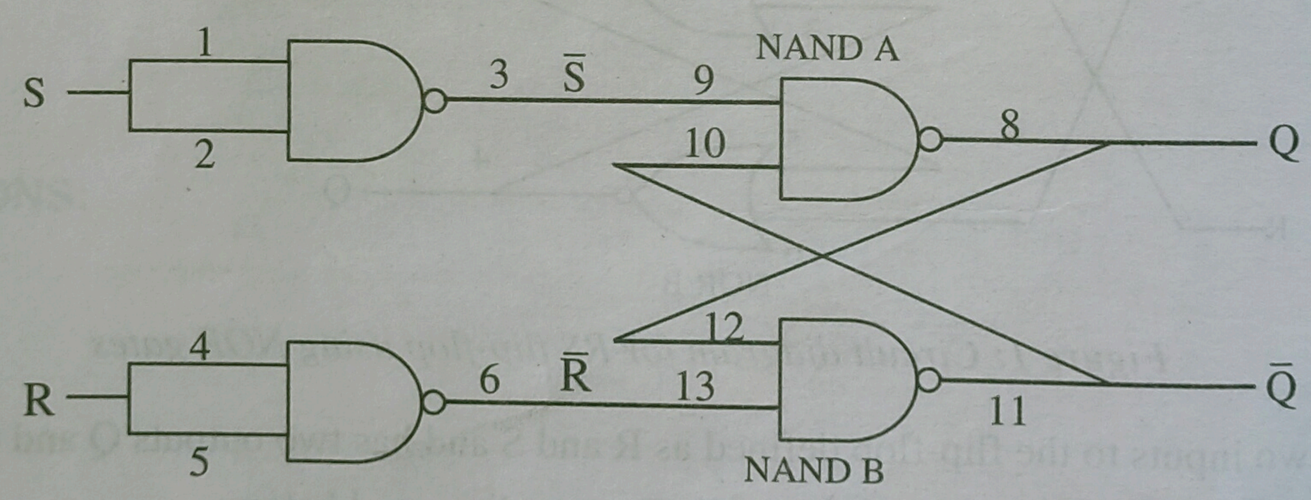


Figure 1: Circuit diagram for RS flip-flop using NAND gate

There are two inputs $\bar{S}$ and $\bar{R}$ complement of S and R respectively and has two outputs Q and $\bar{Q}$. The input/output possibilities for this flip-flop are discussed below.

1. When R = 0 and S = 0 (or $\bar{R} = 1$ and $\bar{S} = 1$)

Since the NAND gate is low sensitive. So a '1' at the input of NAND gate has no effect on its output, the flip-flop simply remains in its previous state that is Q remains unchanged.

2. When R = 0 and S = 1 (or $\bar{R}$ = 1 and $\bar{S}$ = 0)

In this input condition, the output of NAND gate A is high. Both inputs of NAND gate B is high so Q = 1 and $\bar{Q}$ = 0 is the SET state.

3. When R = 1 and S = 0 (or $\bar{R}$ = 0 and $\bar{S}$ = 1)

This condition forces the output of NAND gate B high, and both inputs of NAND gate A are high. Hence Q = 0 and $\bar{Q}$ = 1 is RESET state.

4. When R = 1 and S = 1 (or $\bar{R}$ = 0 and $\bar{S}$ = 0)

This condition is forbidden, as setting both $\bar{R}$ and $\bar{S}$ low this forces Q and $\bar{Q}$ high, which is against the principle of flip-flop as the outputs are not complementing each other.

Truth table for NOR gate RS flip-flop.

$\bar{R}$	$\bar{S}$	Q	Action
1	1	Last state	Unchanged
1	0	1	SET
0	1	0	RESET
0	0	?	Forbidden

Procedure

1. Place the IC in the middle part of bread board such that middle gap lies in the middle region of the board and identify the input and output terminals.
2. Connect the pin no. 14 to power supply and pin 7 to ground to enable the IC.
3. Make the connections as shown in circuit diagram.
4. Record the inputs and output voltages with the help of digital multimeter at the input and output terminals. (Do not write 0 or 1 in observation table.)

OBSERVATIONS:

Least count of multimeter =

Table for NOR gate RS flip-flop.

No. of obs	Inputs		Outputs		Action
	S	R	Q	$\bar{Q}$	
1.					
2.					
3.					
4.					

Table for NAND gate RS flip-flop.

No. of obs	Inputs		Outputs		Action
	S	R	Q	$\bar{Q}$	
1.					
2.					
3.					
4.					

RESULTS:

INTERPRETATION OF RESULTS:

PRECAUTIONS:

Group 5

Experiment No. 5(a)

Date:

TO DESIGN AND STUDY THE LOGIC GATES: NOT, AND, OR, NOR, NAND USING TTL. ALSO STUDY THE POWER LOSS IN NOT GATE.

APPRATUS REQUIRED:

Bread-board, Transistors (BC547C), resistors, Multimeter, Power Supply DC (5V), connecting wires.

THEORY:

Logic gates are the electronic circuits, which operates one or more input signals to produce a standard output. Gates are basic blocks of all digital electronics. There are one or more than one input and only one output and respond only to High voltages (called 1 s) or LOW (ground) voltages (called 0s). The relationship between the input and the output is based on a certain logic. Based on this, logic gates are named as OR gate, AND gate, NOT gate, NOR gate and NAND gate. First three are basic gates whereas last two are universal gates.

(a) OR Gate:

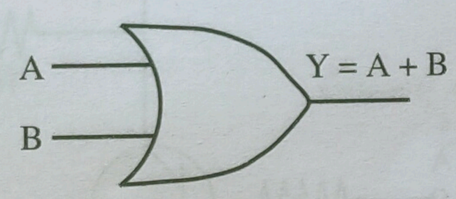
The gate which produces high output (1) if any one of the input is high is known as OR gate. It is the physical representation of logical addition. It can have two or more input signals but only a single output.

Boolean expression for OR gate is

$$Y = A + B$$

Here, A and B are two inputs and Y is output.

Logical symbol



Truth table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Logical symbol

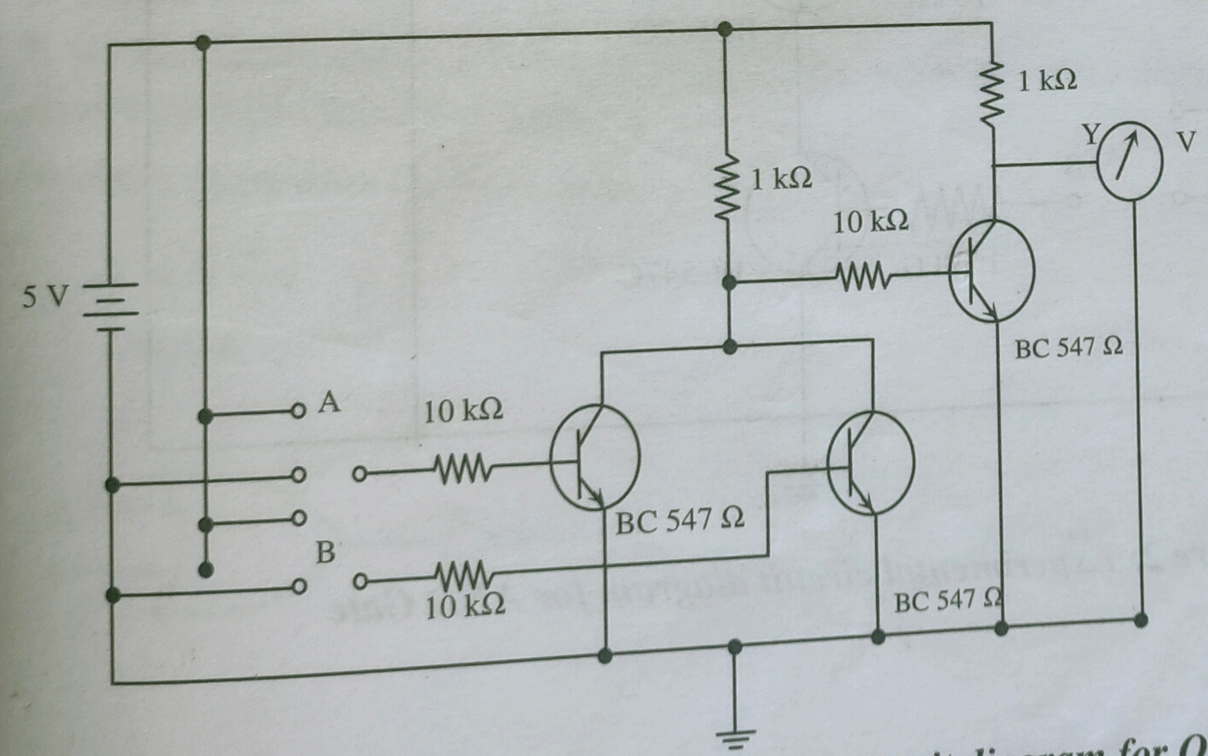


Figure 1: Experimental circuit diagram for OR Gate

(b) AND Gate:

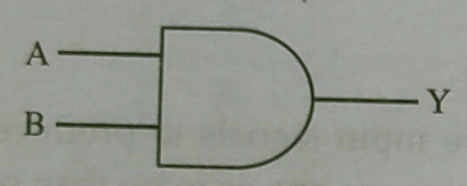
The gate which produce high output if all inputs are high is known as AND gate. It is also known as all or nothing gate. It is the physical representation of logical multiplication. It can have two or more input signals but only one output.

Boolean expression for an AND gate is

$$Y = A.B$$

Here A and B are two inputs and Y is output.

Logical symbol



Truth table

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

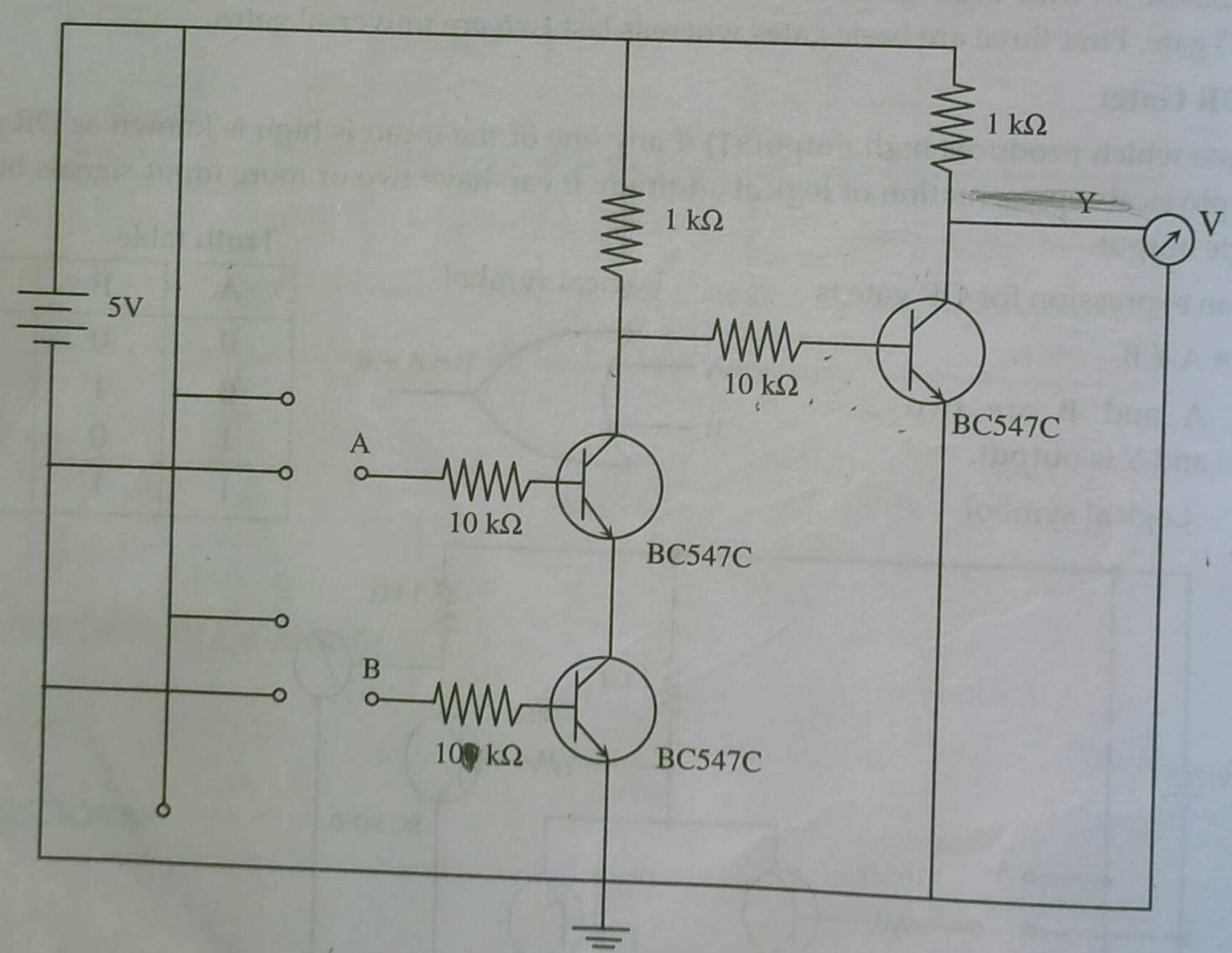


Figure 2: Experimental circuit diagram for AND Gate

(c) NOT Gate

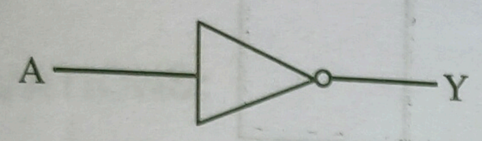
The gate which complements the input is known as NOT gate. It is a gate with only one input and one output. If low input is given then it produces high output and vice versa. It is also known as inverter as it inverts the input.

Boolean expression for a NOT gate is,

$$Y = \overline{A}$$

Here A is input and Y is output.

Logical symbol



Truth Table

A	B
0	1
1	0

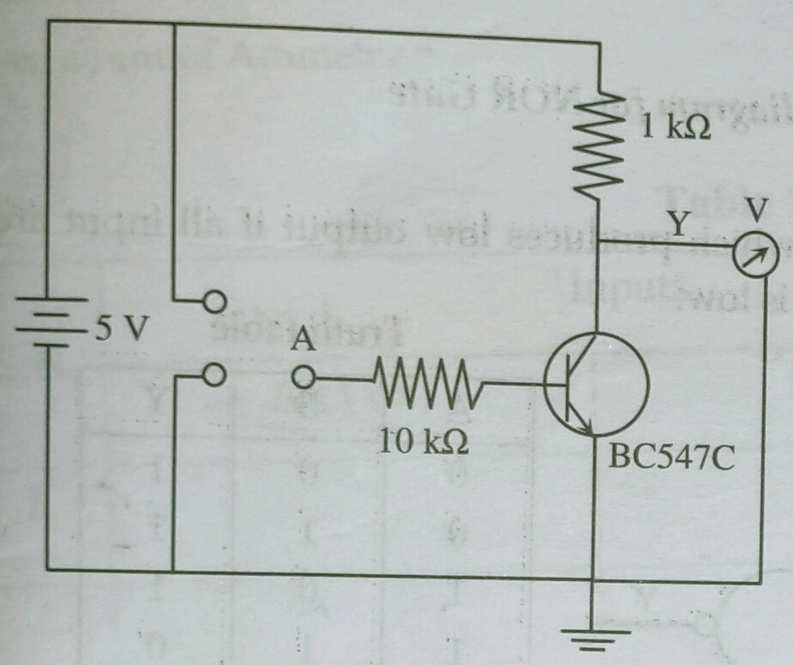


Figure 3: Experimental circuit diagram for NOT Gate

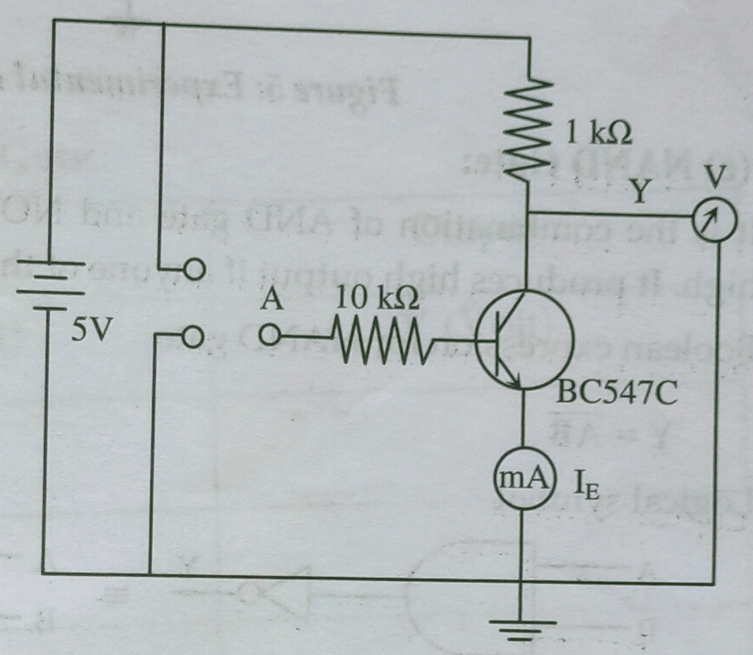


Figure 4: NOT gate for power loss calculations

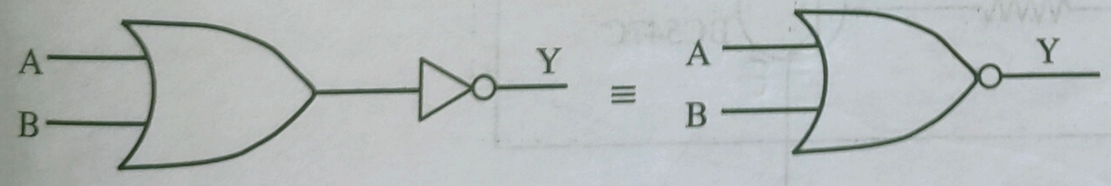
(d) NOR Gate

It is the combination of OR and NOT gates which produces high output if all input are low otherwise it produces low output.

Boolean expression for NOR gate.

$$Y = \overline{A + B}$$

Logical symbol



Truth table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

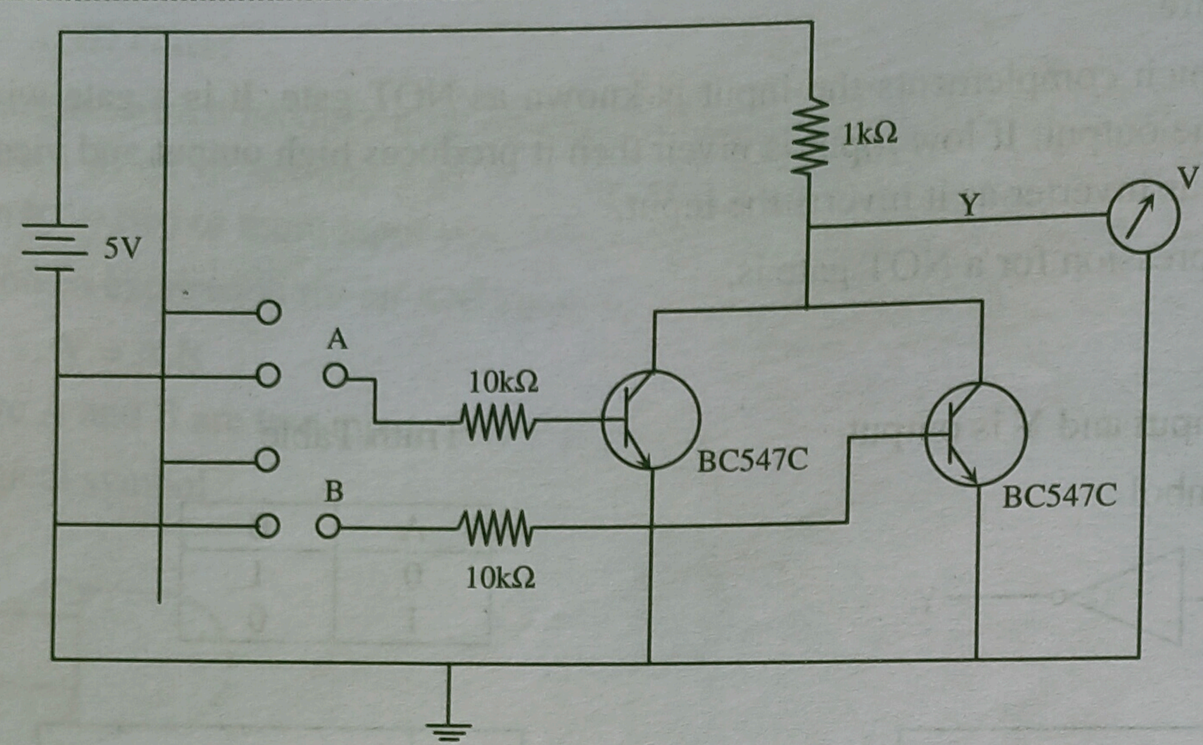


Figure 5: Experimental circuit diagram for NOR Gate

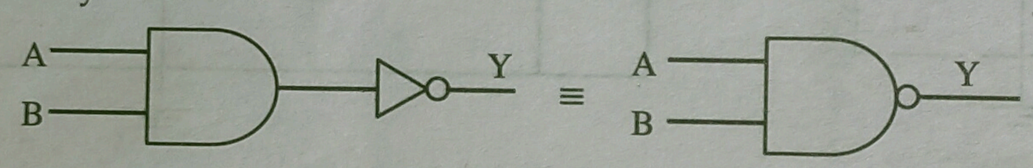
(e) NAND Gate:

It is the combination of AND gate and NOT gate which produces low output if all input are high. It produces high output if anyone of the input is low.

Boolean expression for NAND gate

$$Y = \overline{AB}$$

Logical symbol



Truth table

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

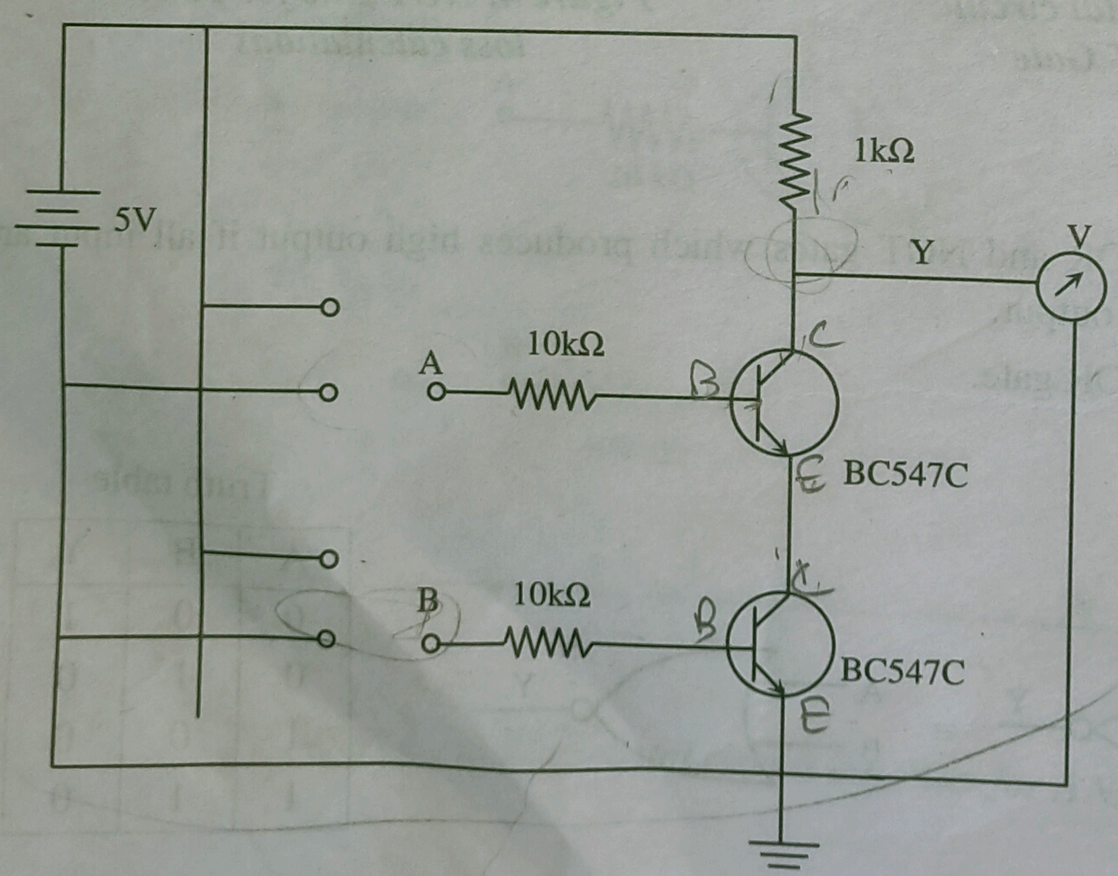


Figure 6: Experimental circuit diagram for NAND Gate

PROCEDURE:

1. Identify the emitter, base and collector of the transistors and make the connections as per circuit diagrams one by one.
2. Apply 0V (ground) at the input for logic '0' and DC 5V at the input for logic '1'.
3. Measure and record the voltage at output Y using voltmeter for different circuit.
4. Now, connect miliammeter to measure emitter current to verify power loss in NOT gate as per NOT gate circuit diagram.

OBSERVATIONS:

Least count of voltmeter =

Least count of Ammeter =

Table 1: OR Gate

S.N.	Inputs		Output
	A (Volt)	B (Volt)	Y (Volt)
1.			
2.			
3.			
4.			

Table 2: AND Gate

S.N.	Inputs		Output
	A (Volt)	B (Volt)	Y (Volt)
1.			
2.			
3.			
4.			

Table 3: NOT Gate

S.N.	Input A (Volt)	Output B (Volt)
1.		
2.		

Table 4: Power Loss in NOT Gate

S.N.	Input A (V)	For transistor		
		Voltage V_0 (V)	Current I_E (mA)	Power $P = V_0 I_E$ (W)
1.				
2.				

Table 5: NOR Gate

S.N.	Inputs		Output
	A (Volt)	B (Volt)	Y (Volt)
1.			
2.			
3.			
4.			

Table 6: NAND Gate

S.N.	Inputs		Output
	A (Volt)	B (Volt)	Y (Volt)
1.			
2.			
3.			
4.			

RESULTS:

INTERPRETATION OF RESULTS:

PRECAUTIONS: