VL502: Analog IC Design, 2024-2025 Final Project

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1. Specifications

Table 1: Specifications Summary

Parameter	Value
Input Voltage (V_{in})	1.4V
Output Voltage (V_{out})	1V
Power Supply Rejection Ratio (PSRR) at heavy load	60dB
Minimum Load Current (I_{load_min})	2mA
Maximum Load Current (I_{load_max})	10mA
Load Capacitance (C_{load})	1nF
Quiescent Current ($I_{quiescent}$)	50μA
Transient Duration	1μs

2. Purpose of an LDO

An LDO (Low Dropout Regulator) is an essential component in analog and digital circuits, primarily used for voltage regulation. It ensures stable and clean power delivery to sensitive electronic components, enhancing their performance and reliability.

1. **Voltage Regulation**: Maintains a steady output voltage despite variations in input voltage or load current, ensuring proper operation of connected components.

2. **Low Dropout Operation**: Operates efficiently with minimal difference between input and output voltage, making it ideal for battery-powered devices.

3. **Power Supply Rejection (PSRR)**: Shields circuits from input power fluctuations, improving signal integrity in precision applications.

In summary, an LDO plays a crucial role in delivering stable, noise-free, and efficient power to various circuit blocks, ensuring optimal performance and protection in electronic systems.

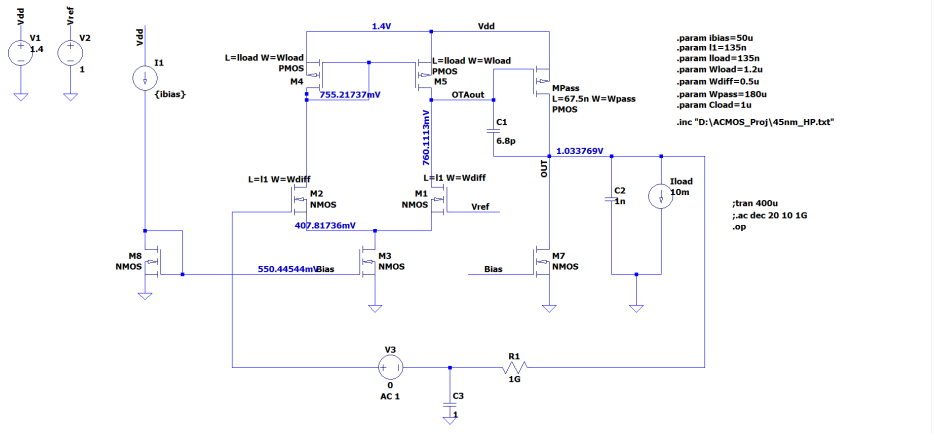

Figure 1: LDO schematic - DC-OP Heavy Load

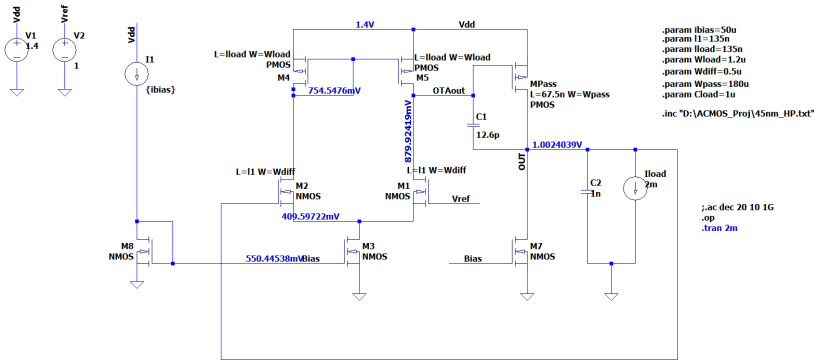

Figure 2: LDO schematic - DC-OP Light Load

3. Relevance of Techplots

Design and Optimization of Low-Dropout Regulators (LDOs) Using Technology Plotting (techplots) methods in contrast to traditional square-law models. This project utilizes the **gpdk 45nm technology node**, leveraging Cadence tools and Python scripting for analysis and visualization.

3.1 Why Techplots Over Square-Law Models?

Square-law models, though widely used in analog circuit design, are approximations that fail to capture short-channel effects, velocity saturation, and other high-field phenomena critical in deep-submicron processes like 45nm. This often leads to discrepancies between design intent and silicon performance.

Techplots bridge this gap by deriving model-independent transistor parameters directly from simulation data. This approach enables more accurate predictions of performance metrics such as:

1. Transconductance (g_m/I_d)
2. Intrinsic gain ($g_m r_o$)
3. Transition frequency (f_t)

GitHub link to our techplots for our chosen technology node of 45 nm

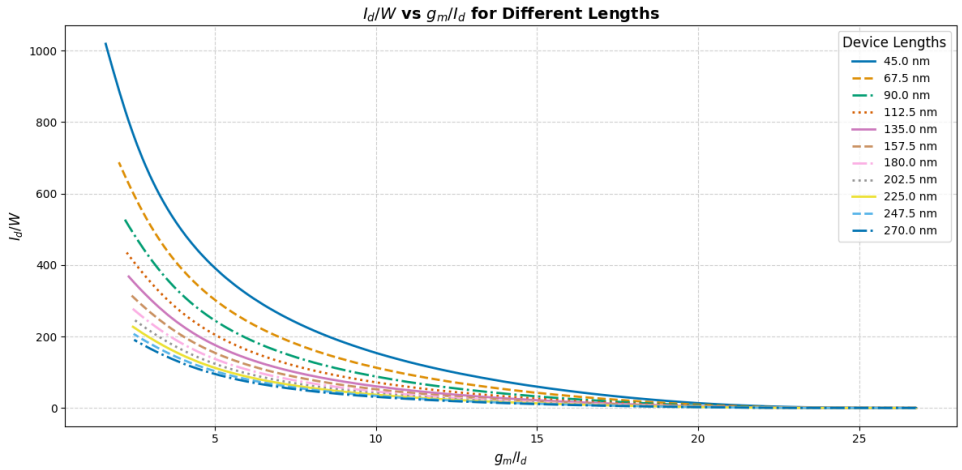

Figure 3: NMOS Techplots after Matlab postprocessing - Id/W

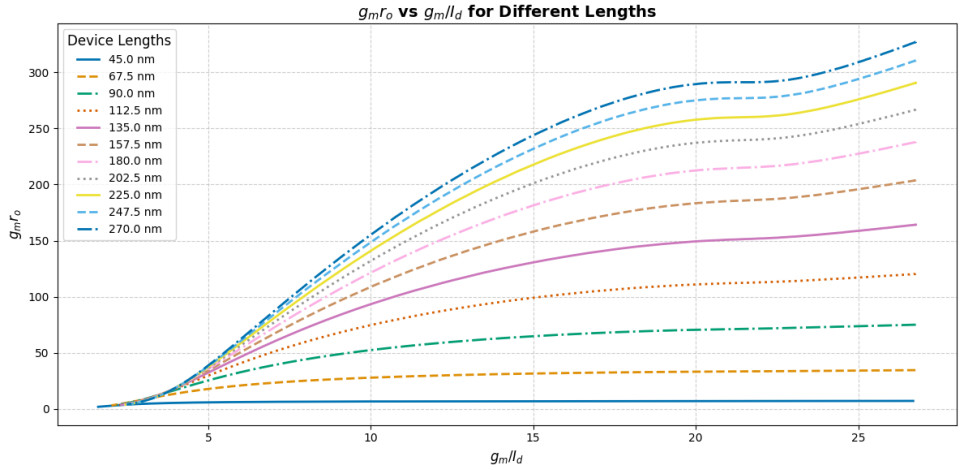

Figure 4: NMOS Techplots after Matlab postprocessing - gmro

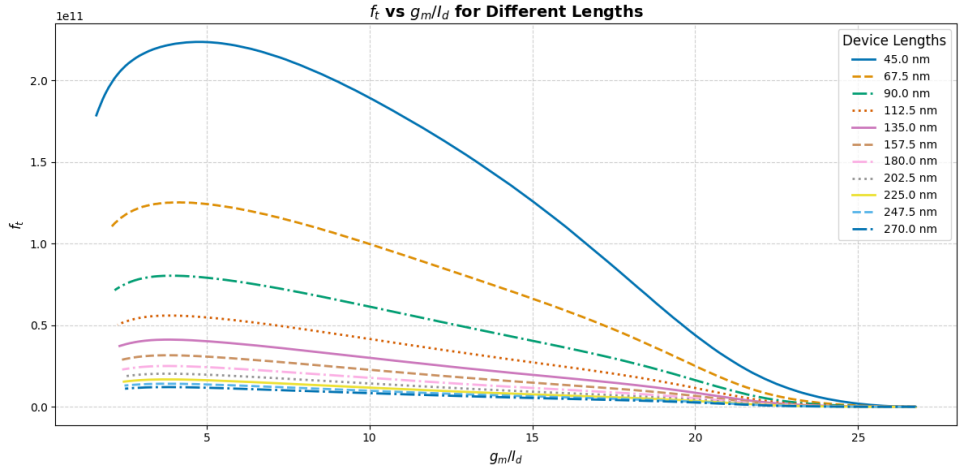

Figure 5: NMOS Techplots after Matlab postprocessing - fT

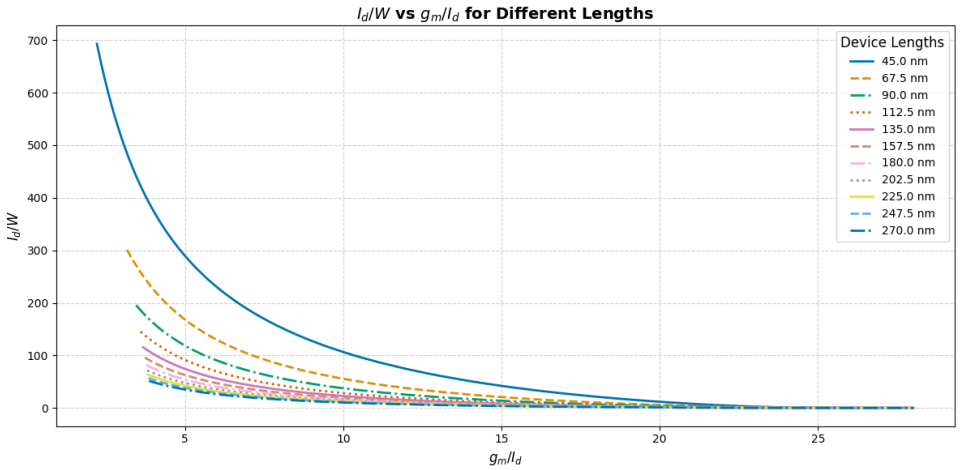

Figure 6: PMOS Techplots after Matlab postprocessing - Id/W

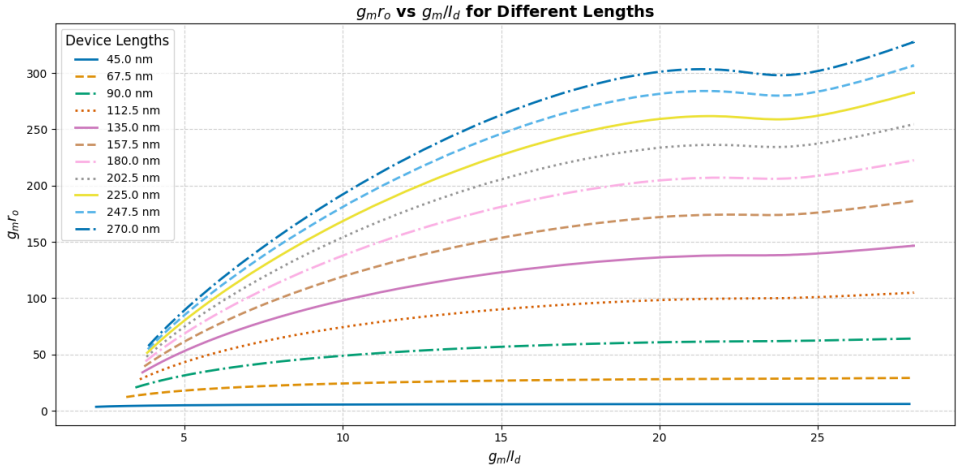

Figure 7: PMOS Techplots after Matlab postprocessing - gmro

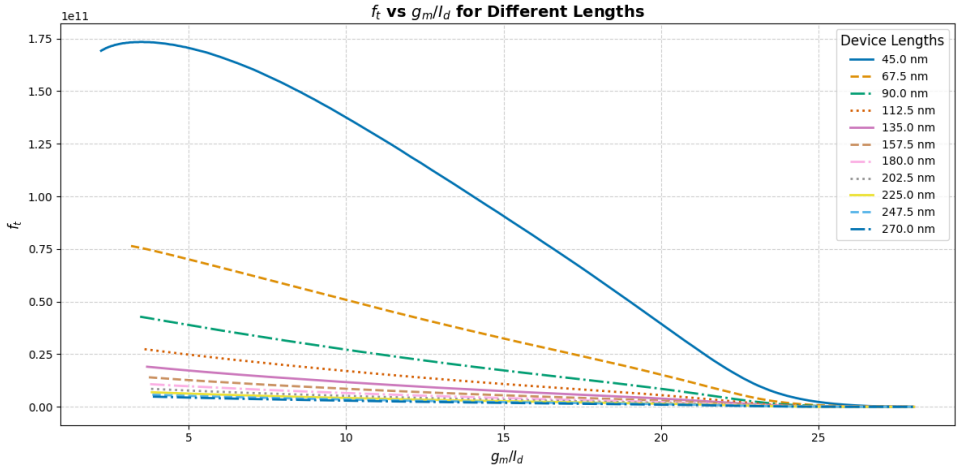

Figure 8: PMOS Techplots after Matlab postprocessing - fT

4. FET Sizes

The FET sizes and parameters were carefully chosen to balance performance metrics such as gain, stability, and efficiency.

1. The pass transistor (180µm/67.5nm) minimized dropout voltage and supported high load currents.
2. OTA transistors were sized for high g_m and adequate loop gain, ensuring stability under all load conditions.
3. The mirror transistors (10µm/1µm) provided robust biasing for consistent performance.

Table 2: FET Sizes and Parameters

Parameter	Pass-FET	OTA-PMOS	OTA-NMOS
Width (W)	180μm	1.2μm	0.5μm
Length (L)	67.5nm	135nm	135nm
g_m	0.1S	0.25mS	0.25mS
r_o	250Ω	320kΩ	320kΩ
g_m/I_d	10	10	10
$g_m r_o$	25	80	80

Table 3: Mirror Transistors Parameters

Width (W)	10μm
Length (L)	1μm

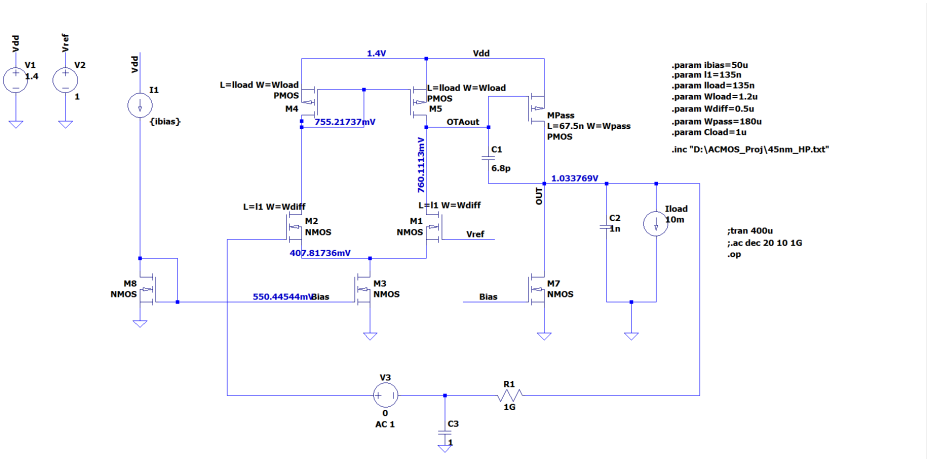

Figure 9: FET sizes and characteristics.

5. Stability Analysis

Stability was a critical focus, with our design achieving phase margins well above the standard 45° threshold.

1. Heavy load conditions yielded a phase margin of 79.04° and a unity gain bandwidth of 3.14MHz.
2. Light load conditions resulted in a phase margin of 64.17° and a bandwidth of 2.8MHz.
3. Poles shifted predictably with load variations, ensuring consistent stability across operating conditions.

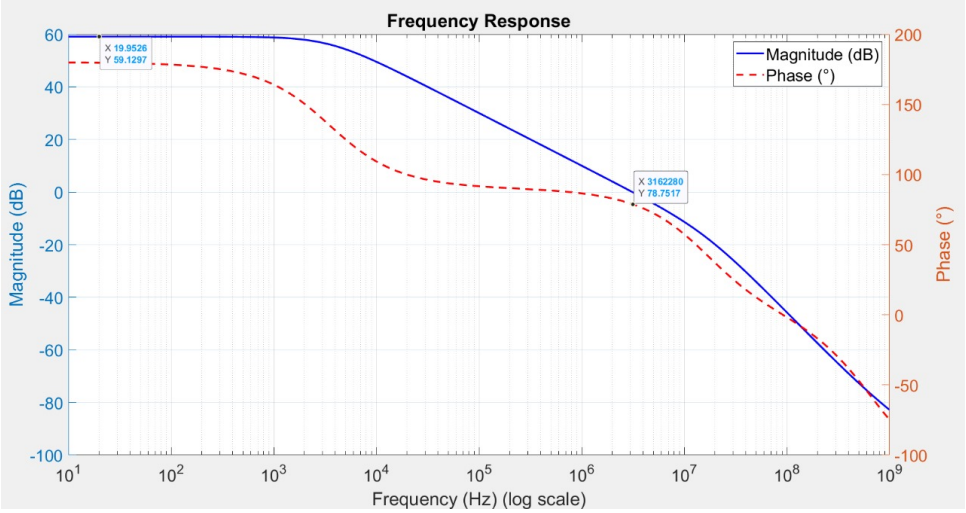

Figure 10: Stability analysis plot. - Heavy Load

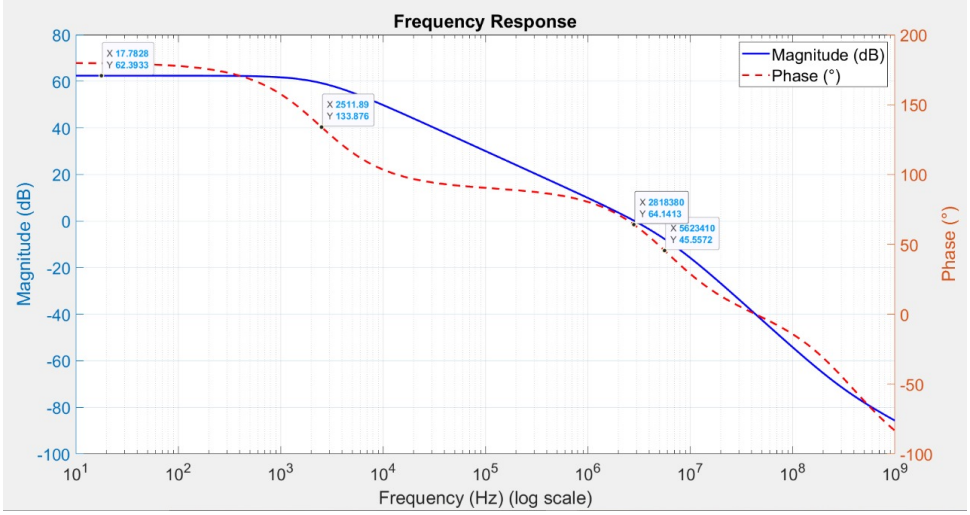

Figure 11: Stability analysis plot.Light Load

Table 4: Key Metrics under Heavy and Light Load Conditions

Parameter	Heavy Load	Light Load
DC Loop Gain (dB)	59.12	62.4
Unity Gain Bandwidth (MHz)	3.14	2.8
Phase Margin (degrees)	79.04	64.17
Pole 1 (KHz)	3.5	2.38
Pole 2 (MHz)	15.26	5.6

6. PSRR Simulation Results

PSRR measures the LDO's ability to suppress variations from the input supply, ensuring a clean and stable output.

1. The PSRR block diagram demonstrates the feedback mechanism mitigating noise transfer.
2. Mathematical representation: PSRR $= 20 \log \left(\frac{V_{\text{out}}}{V_{\text{in}}} \right)$

This analysis highlighted the critical role of feedback and device gain in achieving a PSRR of 60dB under heavy load.

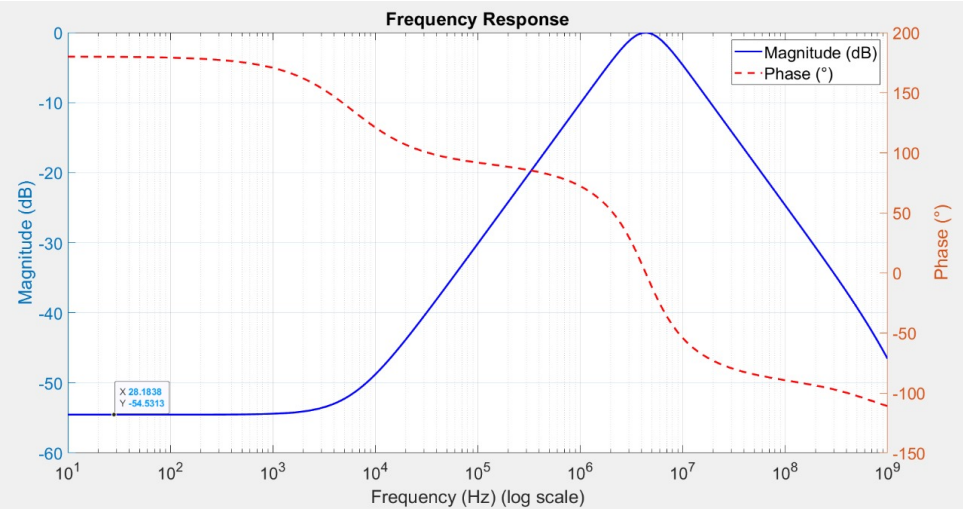

Figure 12: Closed Loop PSRR simulation results - Light load.

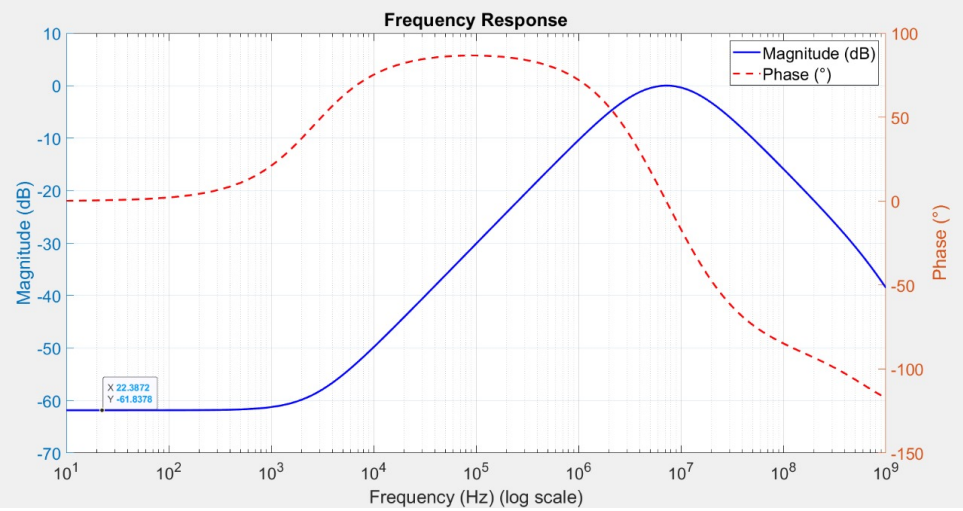

Figure 13: Closed Loop PSRR simulation results - Heavy load.

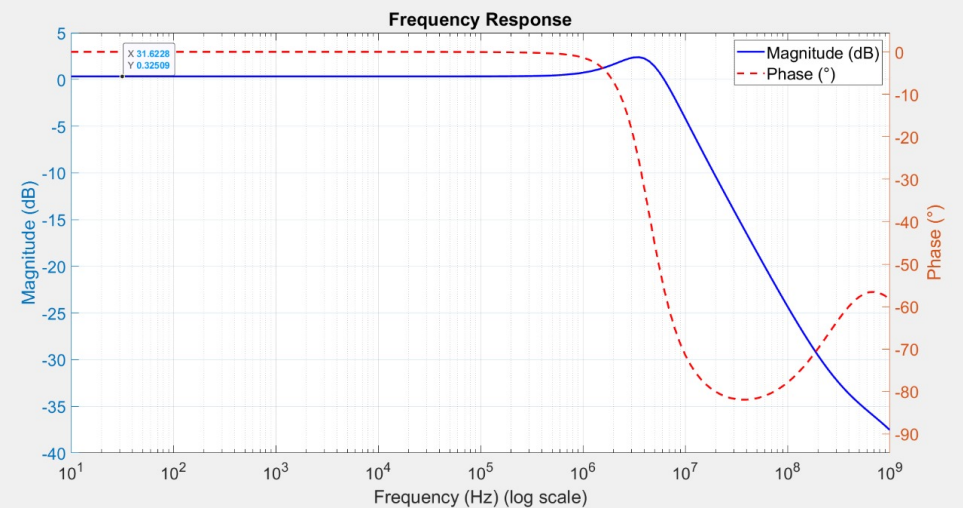

Figure 14: Closed Loop OTA PSRR simulation results - Light load.

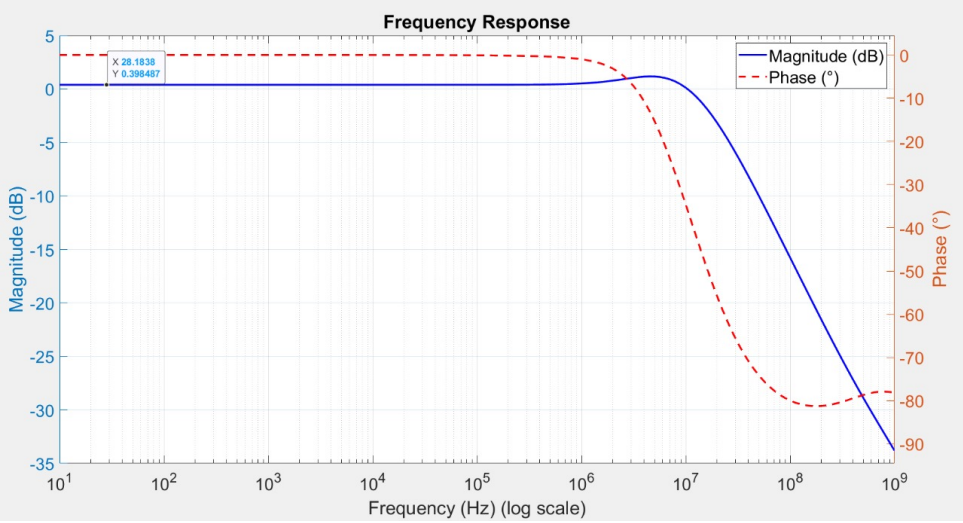

Figure 15: Closed Loop OTA PSRR simulation results - Heavy load.

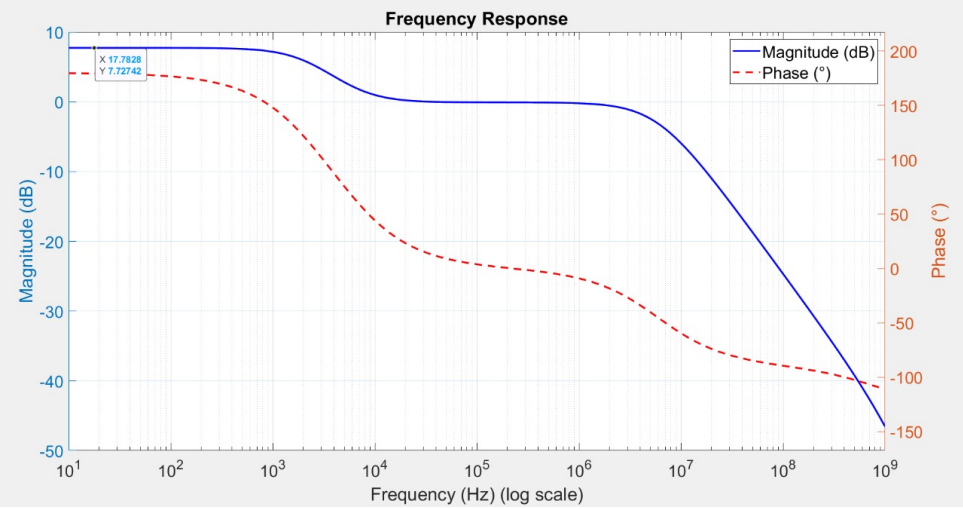

Figure 16: Open Loop PSRR simulation results - Light load.

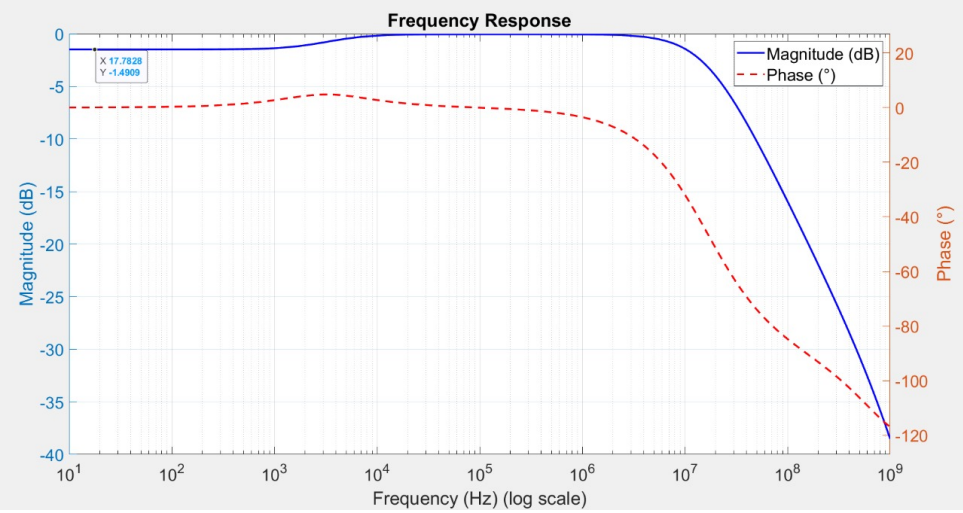

Figure 17: Open Loop PSRR simulation results - Heavy load.

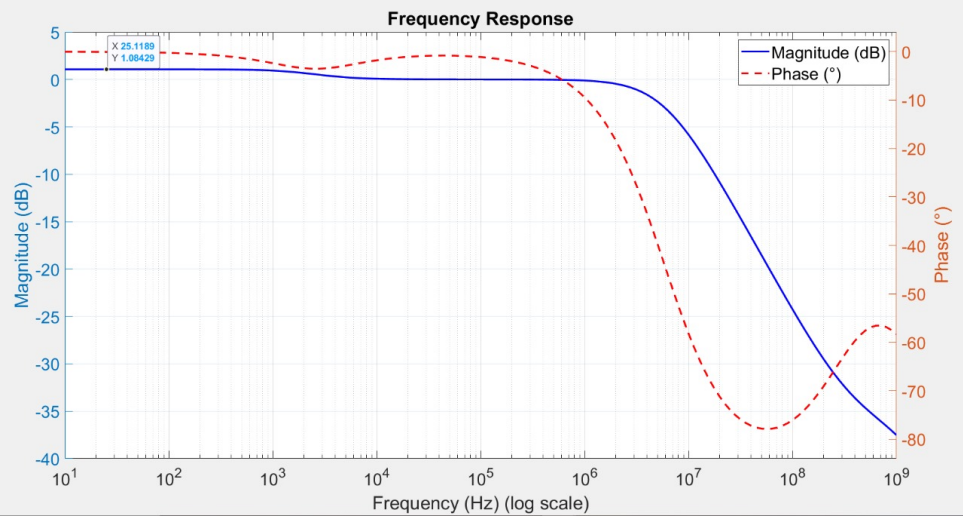

Figure 18: Open Loop OTA PSRR simulation results - Light load.

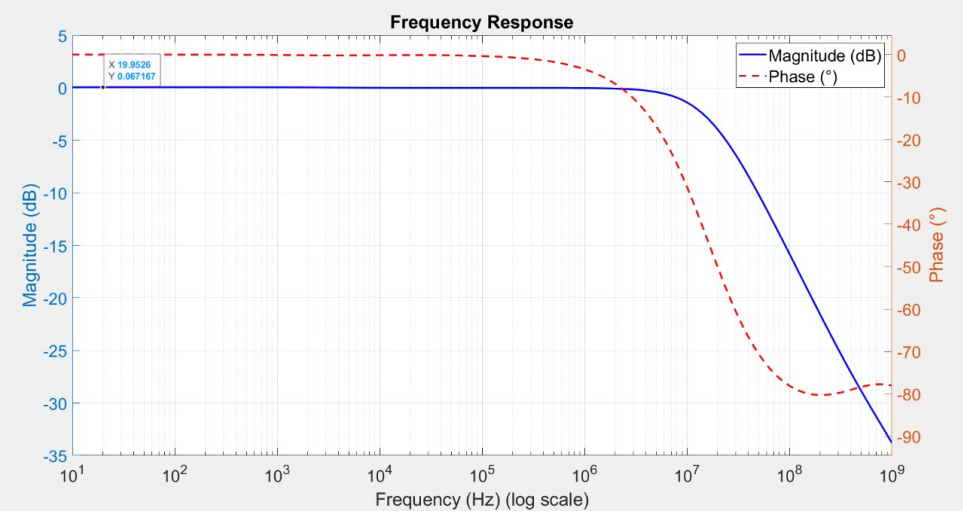

Figure 19: Open Loop OTA PSRR simulation results - Heavy load.

Simulations validated the design's noise rejection capability:

1. Heavy load: PSRR achieved -61.8dB.
2. Light load: Slightly lower PSRR, revealing opportunities for OTA gain optimization.

The findings emphasized the effectiveness of feedback in noise suppression and informed future improvements.

7. Transient Simulation Results

The transient response demonstrated quick stabilization within 1µs during load current transitions (2mA to 10mA).

1. Minimal overshoot and rapid recovery validated the loop bandwidth and compensation choices.

2. The results underscored the importance of maintaining high unity gain bandwidth for rapid load adjustment.

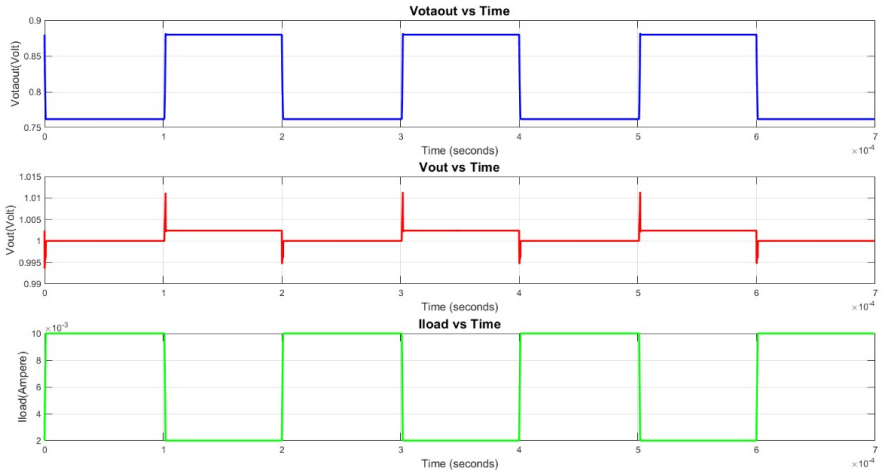

Figure 20: Transient simulation results.

8. Simulation vs. Hand Calculations

Comparison of simulated and calculated values highlighted overall alignment:

Table 5: Simulation vs. Hand Calculations with Percentage Error

Parameter	**Simulation**	**Hand-Calculation**	**% Error**
Heavy Load Loop Gain (dB)	59.12	61.42	-3.7
Light Load Loop Gain (dB)	62.4	61.42	1.5
Heavy Load PSRR (dB)	-61.83	-61.42	0.67
Light Load PSRR (dB)	-54.53	-61.42	-11.2
Heavy Load Phase Margin (degrees)	79.04	78.79	0.31
Light Load Phase Margin (degrees)	64.17	45.23	41.8
Heavy Load Unity Gain Bandwidth (MHz)	3.14	3.155	-0.48
Light Load Unity Gain Bandwidth (MHz)	2.8	3.155	-11.2

The deviations, particularly in light load PSRR, highlighted the limitations of analytical models in deep-submicron designs.

Externally Compensated LDO Design

1. Specifications

The specifications for the externally compensated LDO were carefully chosen to support stable and efficient voltage regulation under varying load conditions.

Table 6: Specifications Summary

Parameter	Value
Input Voltage (V_{in})	1.4V
Output Voltage (V_{out})	1V
Power Supply Rejection Ratio (PSRR) at heavy load	60dB
Minimum Load Current (I_{load_min})	2mA
Maximum Load Current (I_{load_max})	10mA
Load Capacitance (C_{load})	1μF
Quiescent Current ($I_{quiescent}$)	50μA
Transient Duration	1μs

These parameters aimed to optimize stability and transient response while maintaining low power consumption.

2. FET Sizes

The transistor dimensions for the externally compensated LDO were optimized to handle higher capacitances while maintaining stability and efficiency.

1. Pass transistor: 180µm/67.5nm to support high load currents with minimal dropout.
2. OTA transistors: Sized to achieve the required gain for stable operation.
3. Mirror transistors: Designed for reliable biasing under extended load conditions.

Table 7: FET Sizes and Parameters

Parameter	Pass-FET	OTA-PMOS	OTA-NMOS
Width (W)	180μm	1.2μm	0.5μm
Length (L)	67.5nm	135nm	135nm
g_m	0.1S	0.25mS	0.25mS
r_o	250Ω	320kΩ	320kΩ
g_m/I_d	10	10	10
$g_m r_o$	25	80	80

Table 8: Mirror Transistors Parameters

Width (W)	10μm
Length (L)	1μm

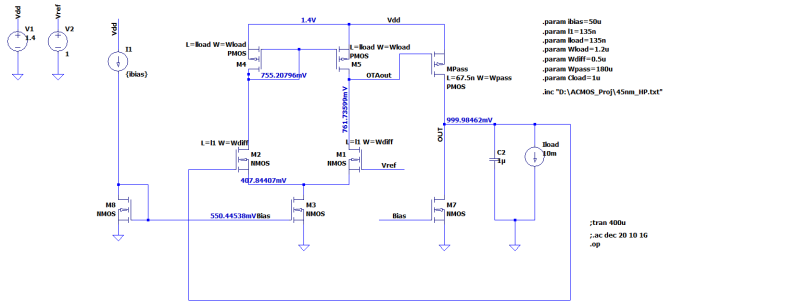

Figure 21: LDO schematic - DC-OP Heavy Load

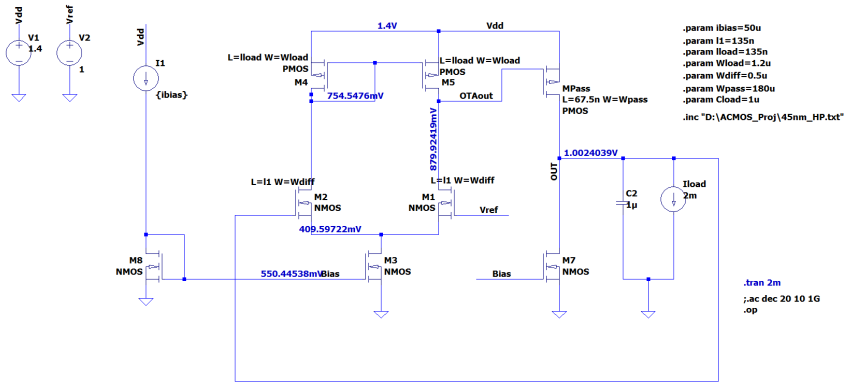

Figure 22: LDO schematic - DC-OP Light Load

3. Stability Analysis

Stability remained a key focus, with external compensation effectively managing the pole-zero locations for consistent phase margins.

1. Heavy load phase margin: 76.56°, ensuring reliable operation.
2. Light load phase margin: 84.89°, demonstrating excellent stability.
3. The first and second poles shifted predictably with external compensation, supporting robust performance across the load range.

The high phase margins highlighted the effectiveness of the external compensation strategy.

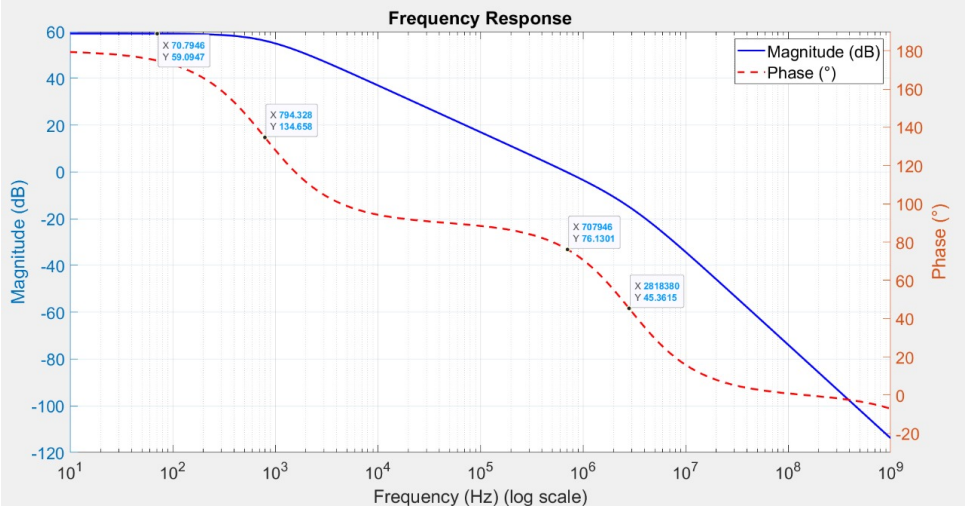

Figure 23: Stability analysis plot. - Heavy Load

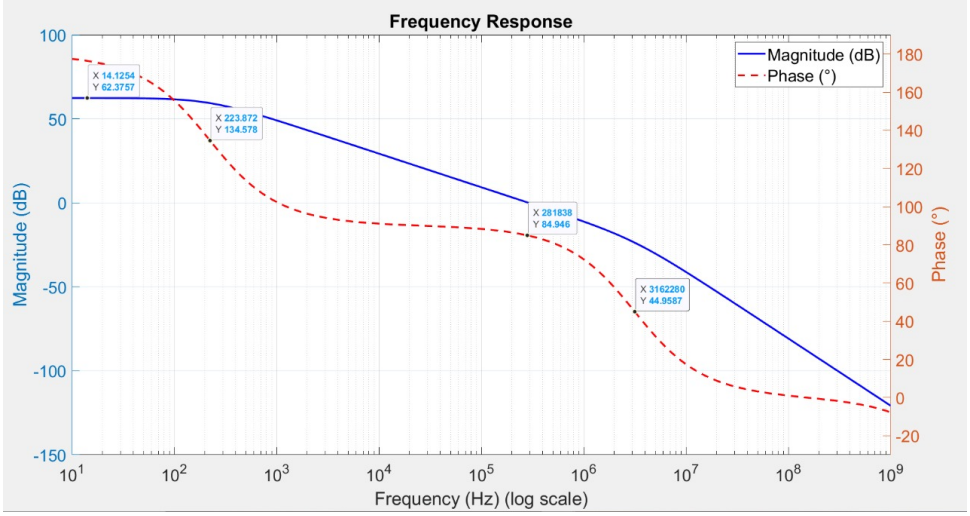

Figure 24: Stability analysis plot. - Light Load

Table 9: Key Metrics under Heavy and Light Load Conditions

Parameter	Heavy Load	Light Load
DC Loop Gain (dB)	59.12	62.38
Unity Gain Bandwidth (kHz)	684	284
Phase Margin (degrees)	76.56	84.89
Pole 1 (Hz)	768	218
Pole 2 (MHz)	2.8	3

4. PSRR Simulation Results

The externally compensated LDO exhibited improved PSRR due to enhanced feedback loop characteristics.

Simulations confirmed the externally compensated LDO's superior noise rejection capabilities:

1. Heavy load: PSRR achieved -61.8dB.
2. Light load: Slight improvements compared to internally compensated designs, further stabilizing output under variable input conditions.

These results validated the advantages of external compensation in managing PSRR.

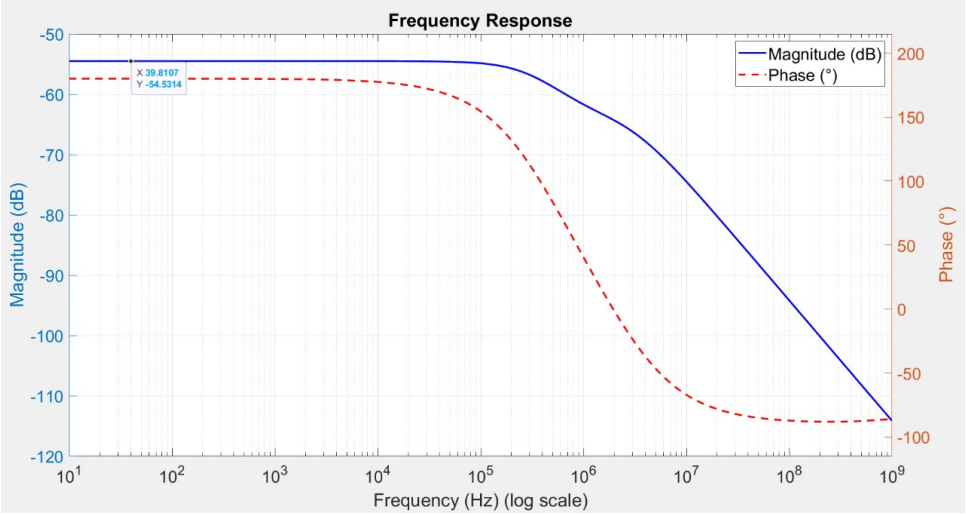

Figure 25: Closed Loop PSRR simulation results - Light load.

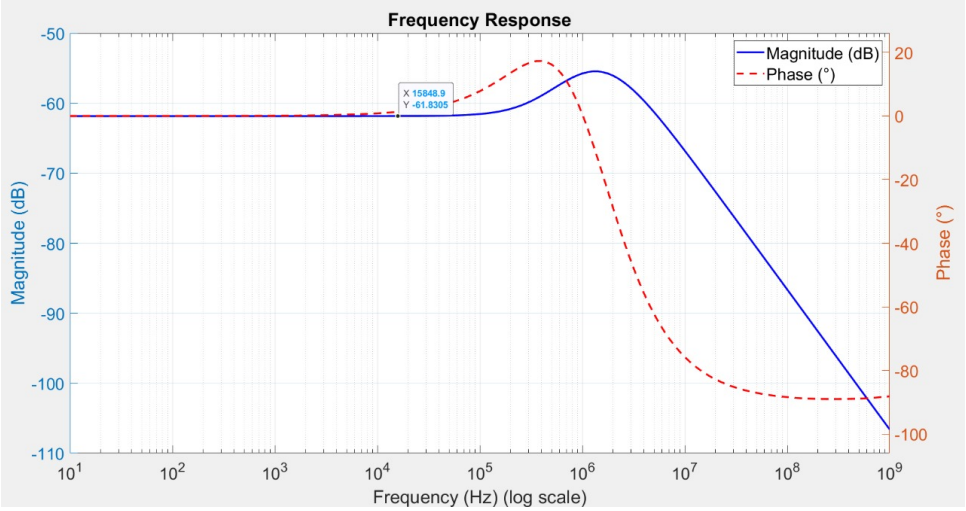

Figure 26: Closed Loop PSRR simulation results - Heavy load.

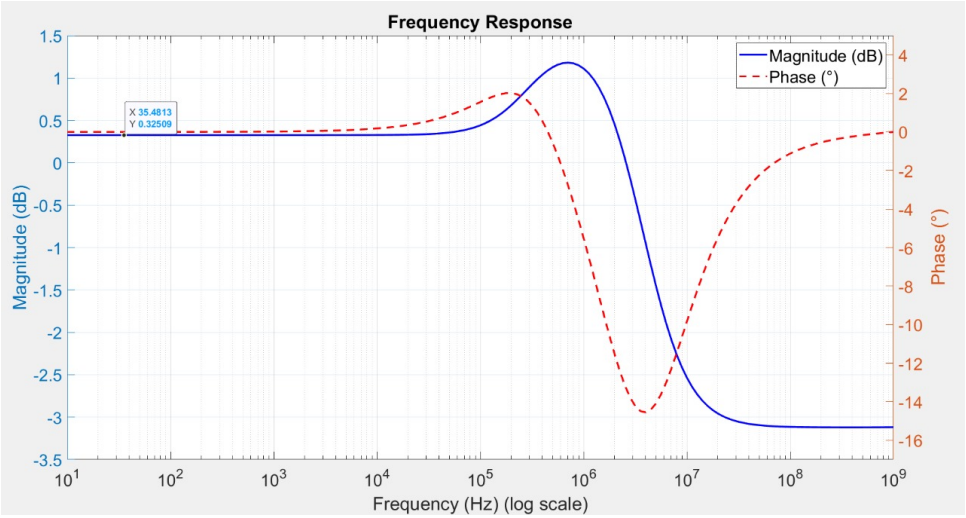

Figure 27: Closed Loop OTA PSRR simulation results - Light load.

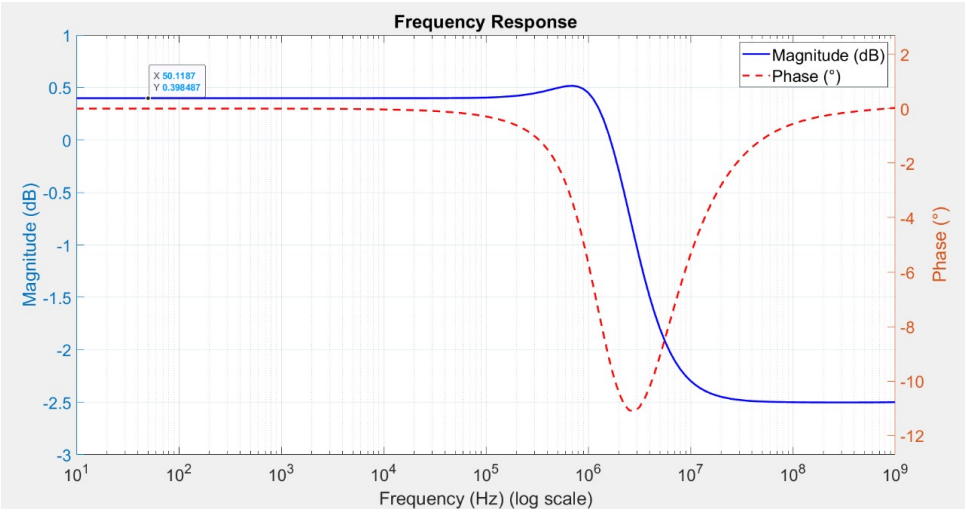

Figure 28: Closed Loop OTA PSRR simulation results - Heavy load.

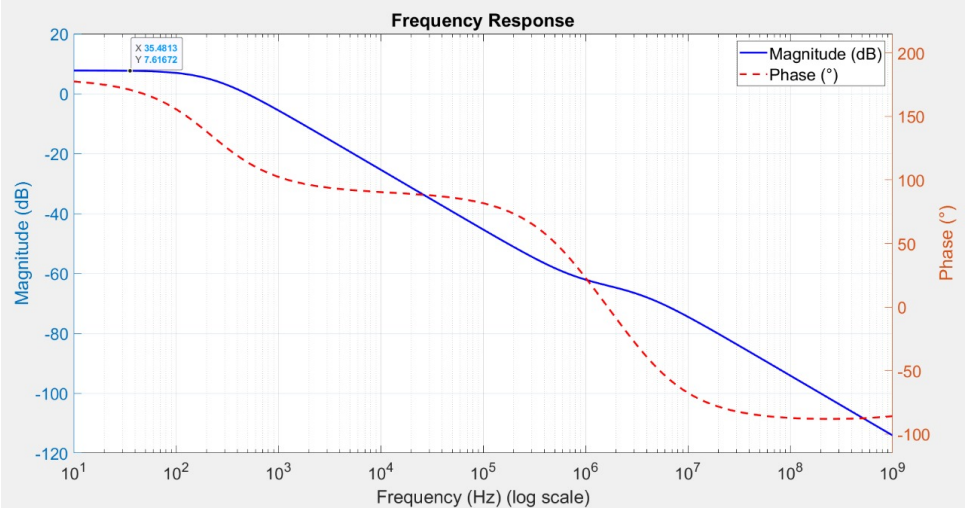

Figure 29: Open Loop PSRR simulation results - Light load.

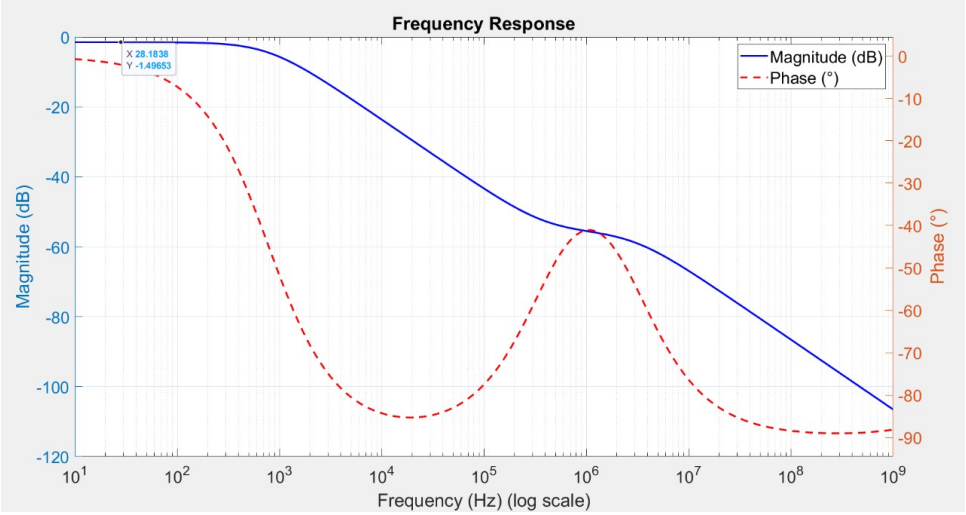

Figure 30: Open Loop PSRR simulation results - Heavy load.

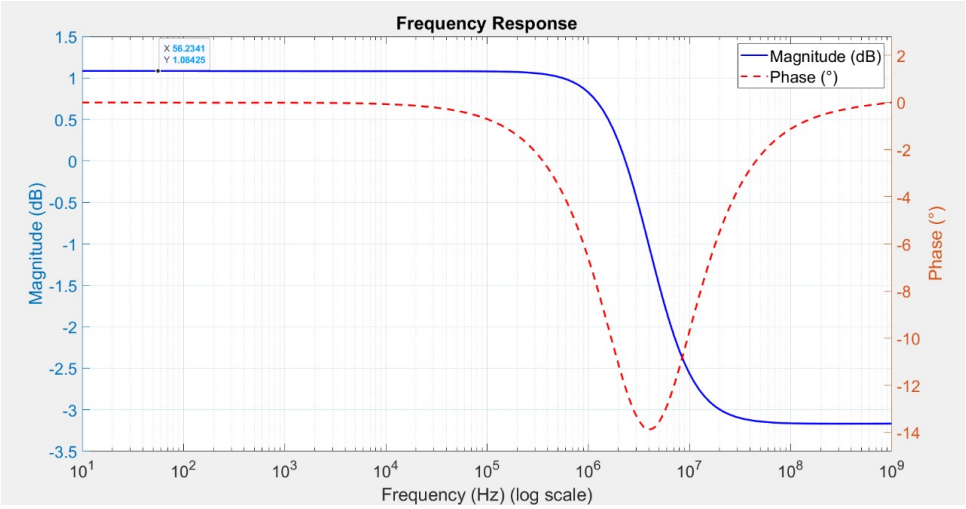

Figure 31: Open Loop OTA PSRR simulation results - Light load.

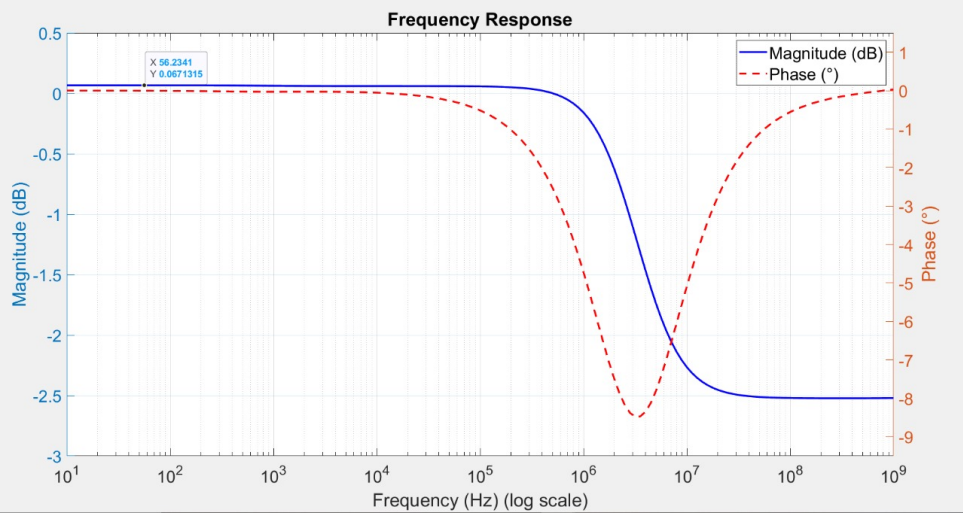

Figure 32: Open Loop OTA PSRR simulation results - Heavy load.

5. Transient Simulation Results

The transient simulations demonstrated improved output regulation under load current transitions (2mA to 10mA).

1. Stabilized within 1µs, meeting design goals.
2. External compensation reduced overshoot, ensuring smoother transitions.
3. The results reinforced the importance of compensation capacitance in minimizing transient disturbances.

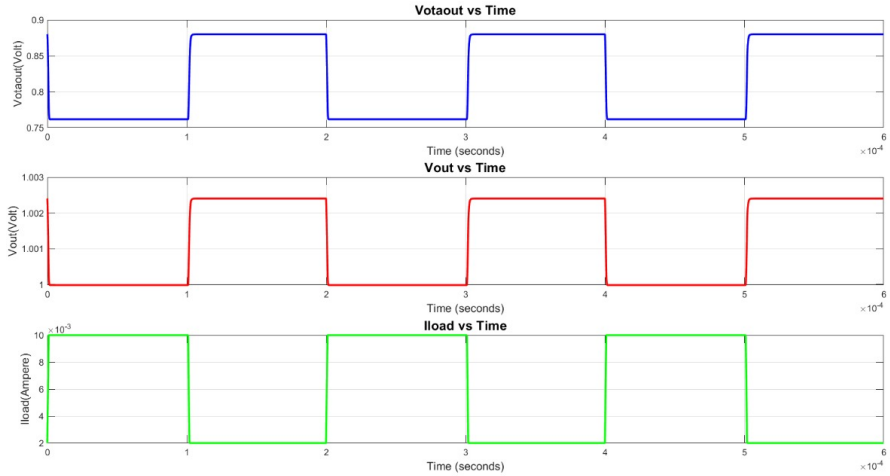

Figure 33: Transient simulation results.

6. Simulation vs. Hand Calculations

Comparing simulations with hand calculations provided valuable insights into the performance of the externally compensated LDO.

Table 10: Simulation vs. Hand Calculations with Percentage Error

Parameter	**Simulation**	**Hand-Calculation**	**% Error**
Heavy Load Loop Gain (dB)	59.12	61.42	-3.7
Light Load Loop Gain (dB)	62.4	61.42	1.5
Heavy Load PSRR (dB)	-61.8	-61.42	0.67
Light Load PSRR (dB)	-54.53	-61.42	-11.2
Heavy Load Phase Margin (degrees)	76.6	81.8	-6.2
Light Load Phase Margin (degrees)	84.9	86.5	-1.7
Heavy Load Unity Gain Bandwidth (kHz)	684	636	7.5
Light Load Unity Gain Bandwidth (kHz)	284	187	56.2

These comparisons underscored the effectiveness of external compensation, while minor discrepancies pointed to the need for fine-tuning analytical models.