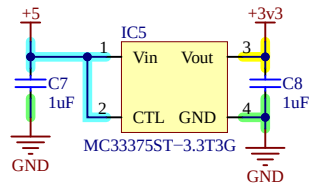
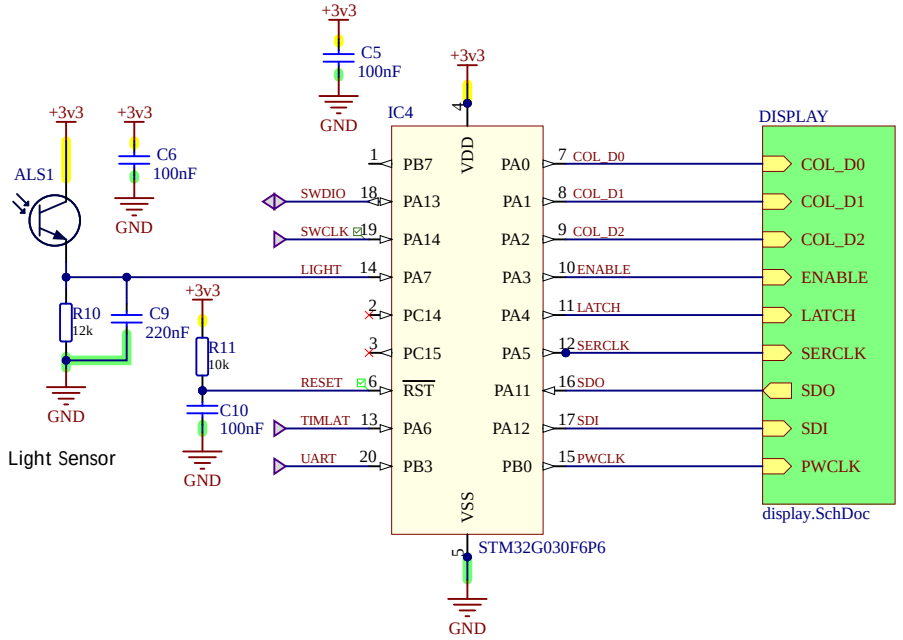
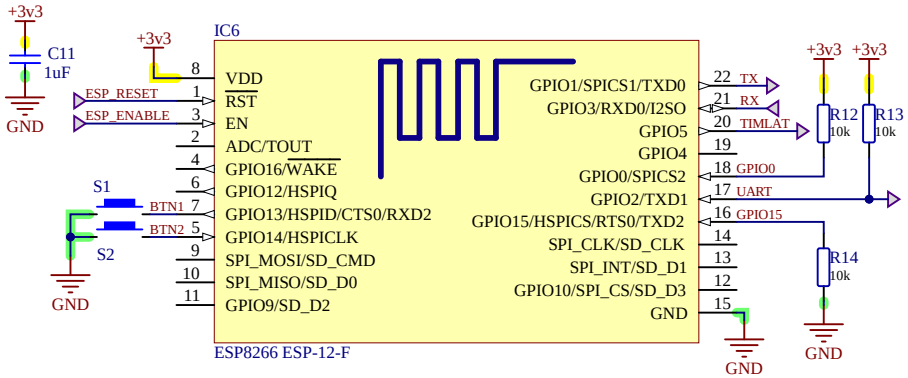


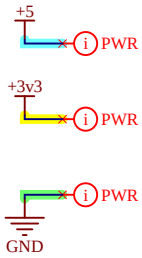
3v3 LDO



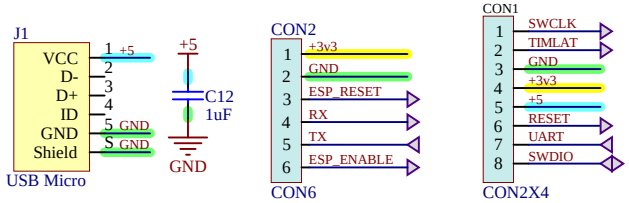
Display Controller



ESP8266 E12F



Net Classes



Connectors

Title		
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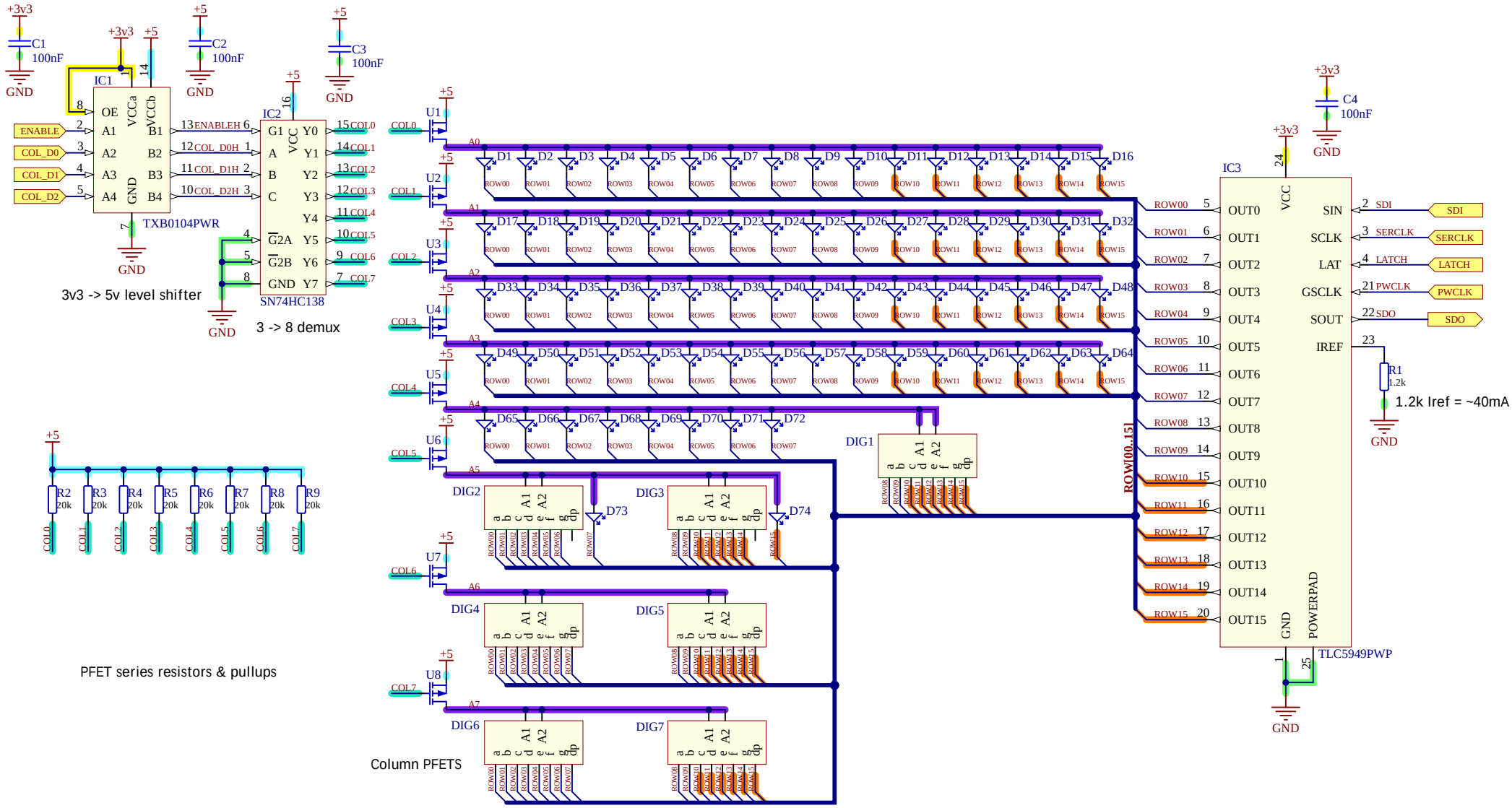
File: C:\Dev\clock\clock.SchDoc		Drawn By:



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Date: 10/18/2020		Sheet of
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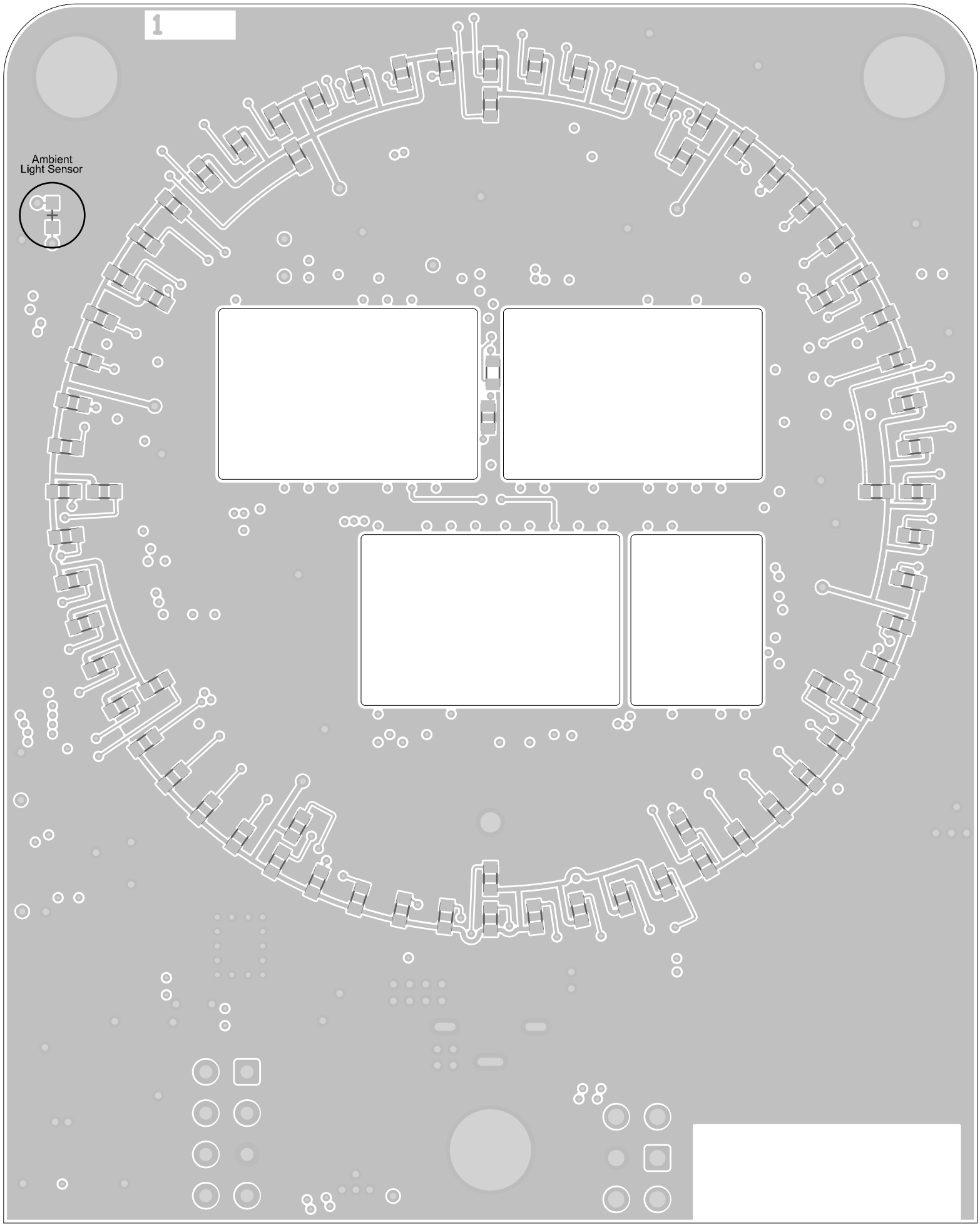
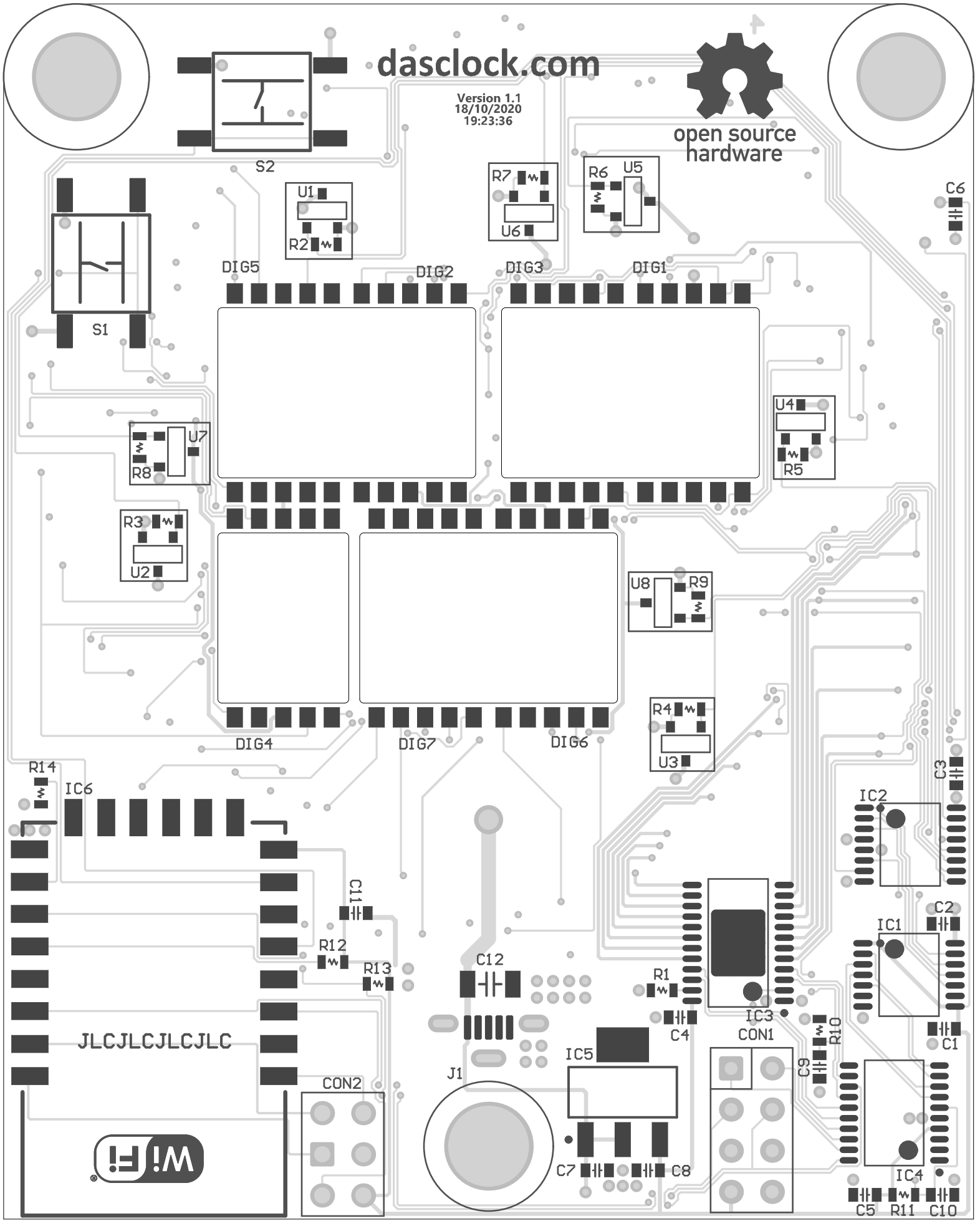

1
Ambient
Light Sensor


dasclock.com
Version 1.1
18/10/2020
19:23:36
open source
hardware
S2
S1
U1
R2
R7
U6
R6
U5
C6
DIG5
DIG2
DIG3
DIG1
U4
R5
U7
R8
R3
U2
U8
R9
R4
U3
DIG4
DIG7
DIG6
R14
IC6
C3
IC2
C11
R12
R13
C12
R1
C4
IC3
CON1
C2
IC1
C1
R10
C9
JLCJLCJLCJLC
J1
IC5
CON2
C7
C8
IC4
C5
R11
C10

Designator	Value	Quantity	Name	Footprint	Description
ALS1		1	PHOTOTRANSISTOR	ALS-PT19-315C	Photo transistor
C1-C6, C10	100nF	7	Cap	CAPC_0603_1608X08L	Capacitor
C7, C8, C11	1uF	3	Cap	CAPC_0603_1608X08L	Capacitor
C9	220nF	1	Cap	CAPC_0603_1608X08L	Capacitor
C12	1uF	1	Cap	CAPC_1206_3216X16L	Capacitor
D1-D74		74	LED	0603 Chip SMD LED	Red 0603 SMD LED
DIG1-DIG7		7	KCSA03-105	KCSA03105	Low profile 7 segment digit
IC1		1	TXB0104PWR	TSOP65P640X120-14L	4 channel level shifter
IC2		1	SN74HC138	TSOP65P640X110-16L	3 -> 8 demux
IC3		1	TLC5949PWP	TSOP65P640X120-24L - POWERPAD	16 channel cc sink led driver
IC4		1	STM32G030F6P6	TSOP65P630X120-20L	MCU 64MHz tssop20
IC5		1	MC33375ST−3.3T3G	SOT230P700X180-4N	3.3v LDO
IC6		1	ESP8266 ESP-12-F	ESP8266 ESP-12-E	ESP8266 ESP-12-F
J1		1	USB Micro	USB 1051330011	USB 2.0 Type B Micro vertical SMT
R1	1.2k	1	RES0603	RESC1608X03L	Chip Resistor
R2-R9	20k	8	RES0603	RESC1608X03L	Chip Resistor
R10	12k	1	RES0603	RESC1608X03L	Chip Resistor
R11-R14	10k	4	RES0603	RESC1608X03L	Chip Resistor
S1, S2		2	4-1437565-1	FSM-SWITCH	6x6mm SMD tactile switch,SPST-NO
U1-U8		8	MOSFET-P	SOT95P230X110-3L	P channel mosfet 1.2A

Design Rules Verification Report

Filename : C:\Dev\clock\clock.PcbDoc

Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=7.874mil) (InComponentClass('LED_DIGIT') AND False),(OnLayer('Multi-Layer'))	0
Clearance Constraint (Gap=4mil) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=5mil) (Max=71497.938mil) (Preferred=8mil) (All)	0
Routing Layers(All)	0
Routing Layers(TouchesRoom('BOTTOM_GND'))	0
Power Plane Connect Rule(Relief Connect)(Expansion=11.811mil) (Conductor Width=4mil) (Air Gap=4mil) (Entries=4)	0
Power Plane Connect Rule(Direct Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4)	0
Minimum Annular Ring (Minimum=5.118mil) (All)	0
Hole Size Constraint (Min=7.874mil) (Max=248.031mil) (All)	0
Hole To Hole Clearance (Gap=9.842mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0mil) (All),(All)	0
Silk To Solder Mask (Clearance=4mil) (False),(All)	0
Net Antennae (Tolerance=0mil) (False)	0
Board Clearance Constraint (Gap=0mil) (OnLayer('Top Copper') Or OnLayer('Bottom Copper') Or OnLayer('Signal Laye	0
Component Clearance Constraint (Horizontal Gap = 3.937mil, Vertical Gap = 0mil) (All),(All)	0
Height Constraint (Min=0mil) (Max=71497.938mil) (Prefered=500mil) (All)	0
Total	0