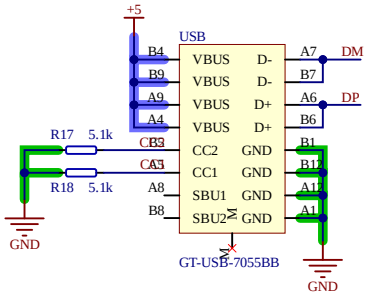
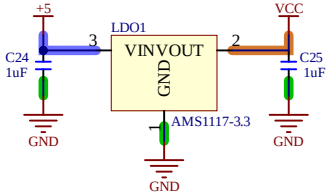
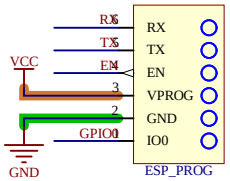
USB Connector



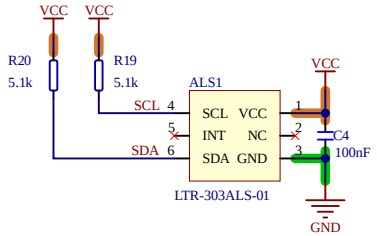
3.3V LDO



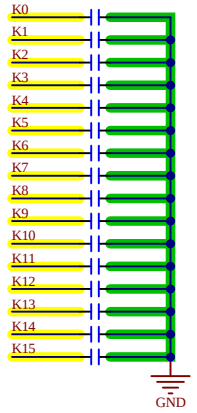
ESP Prog header



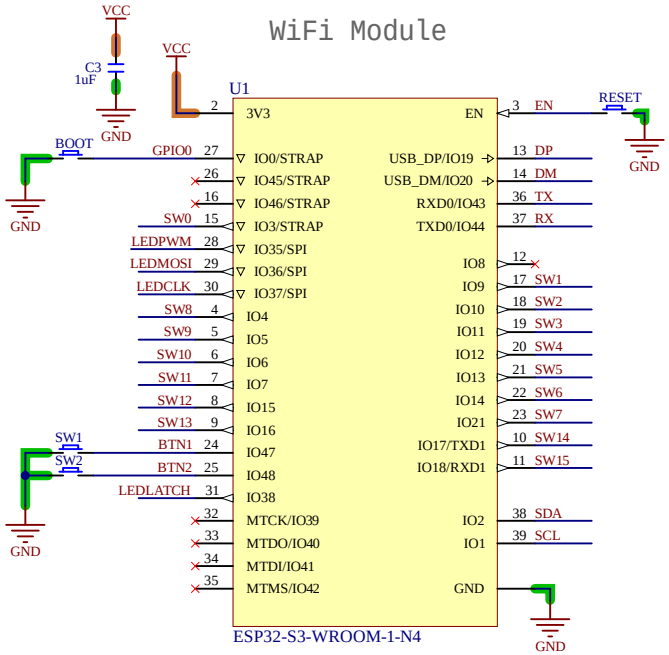
Ambient Light Sensor



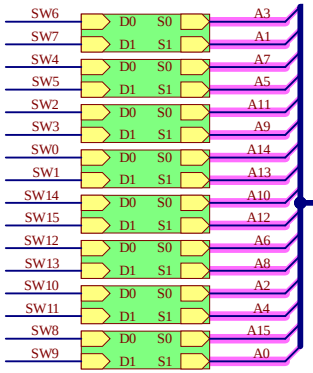
Cathode debounce



WiFi Module

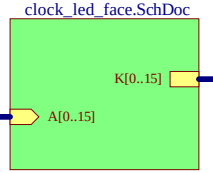


Anode switches

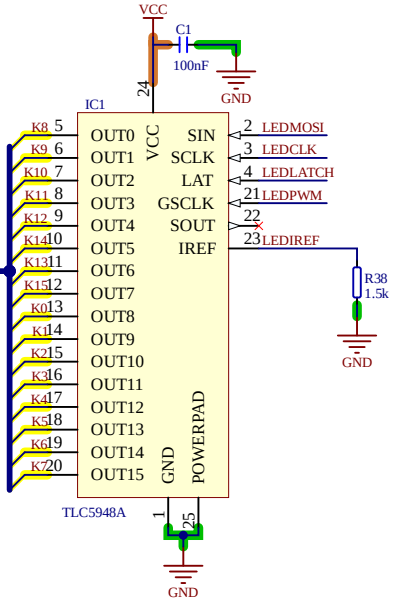


LEDs

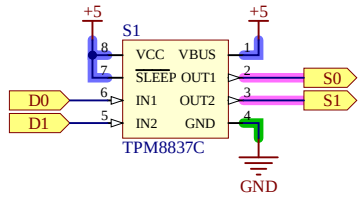
CLOCK FACE
clock_led_face.SchDoc



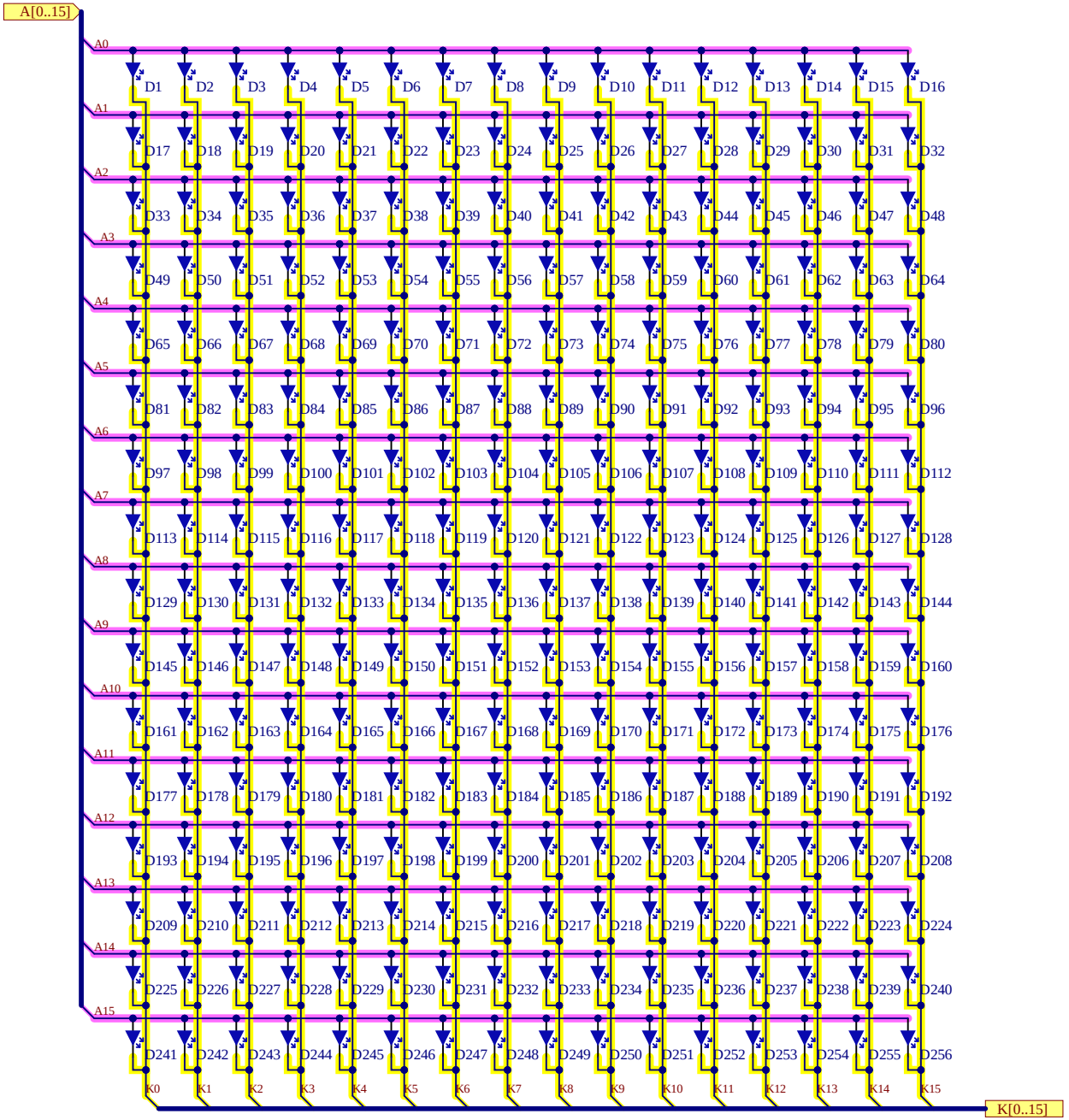
LED Driver



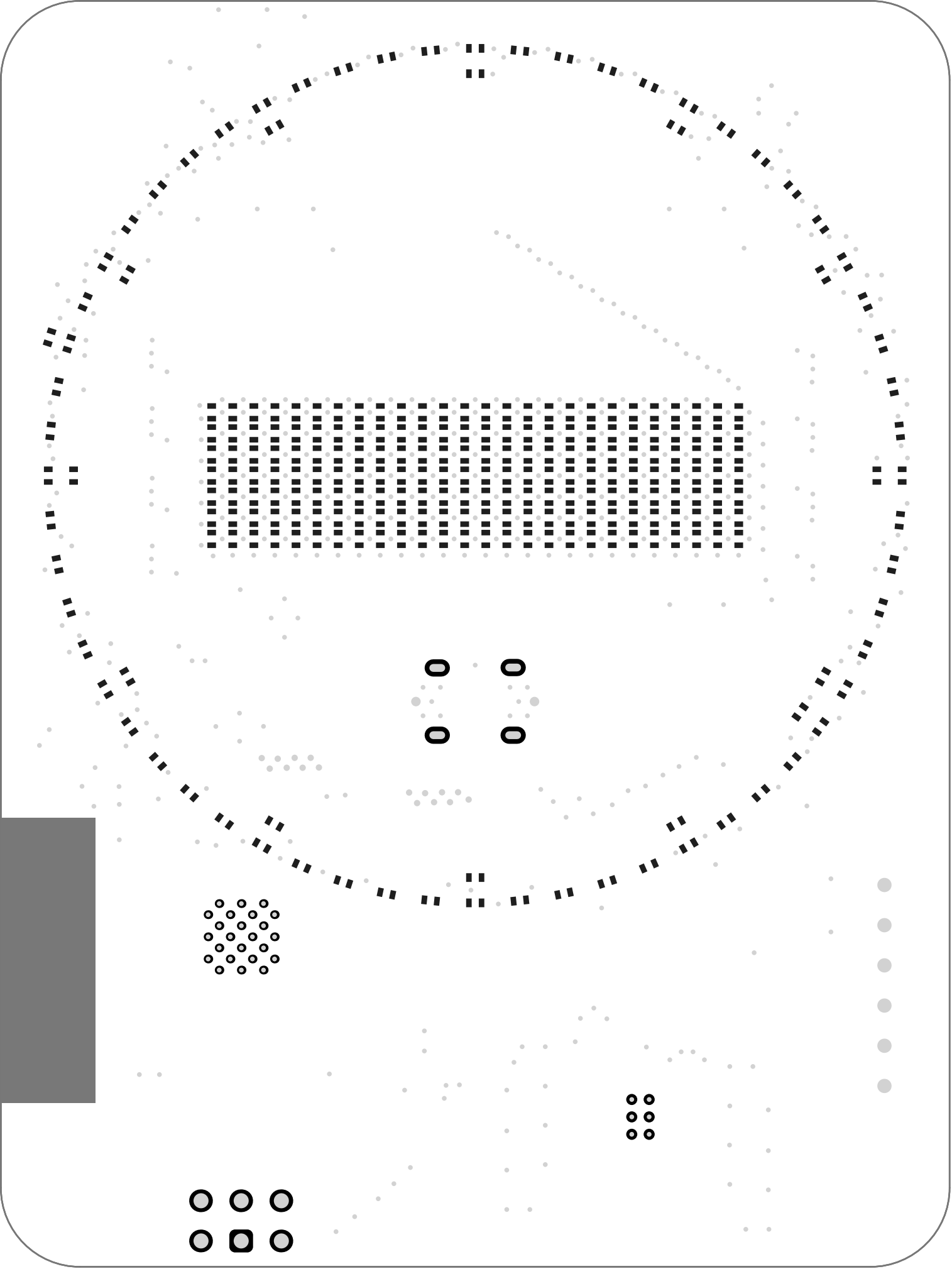
Clock Monsieur	Revision *
	Saved on 31 Oct 2025
chs	Sheet 1 of 2

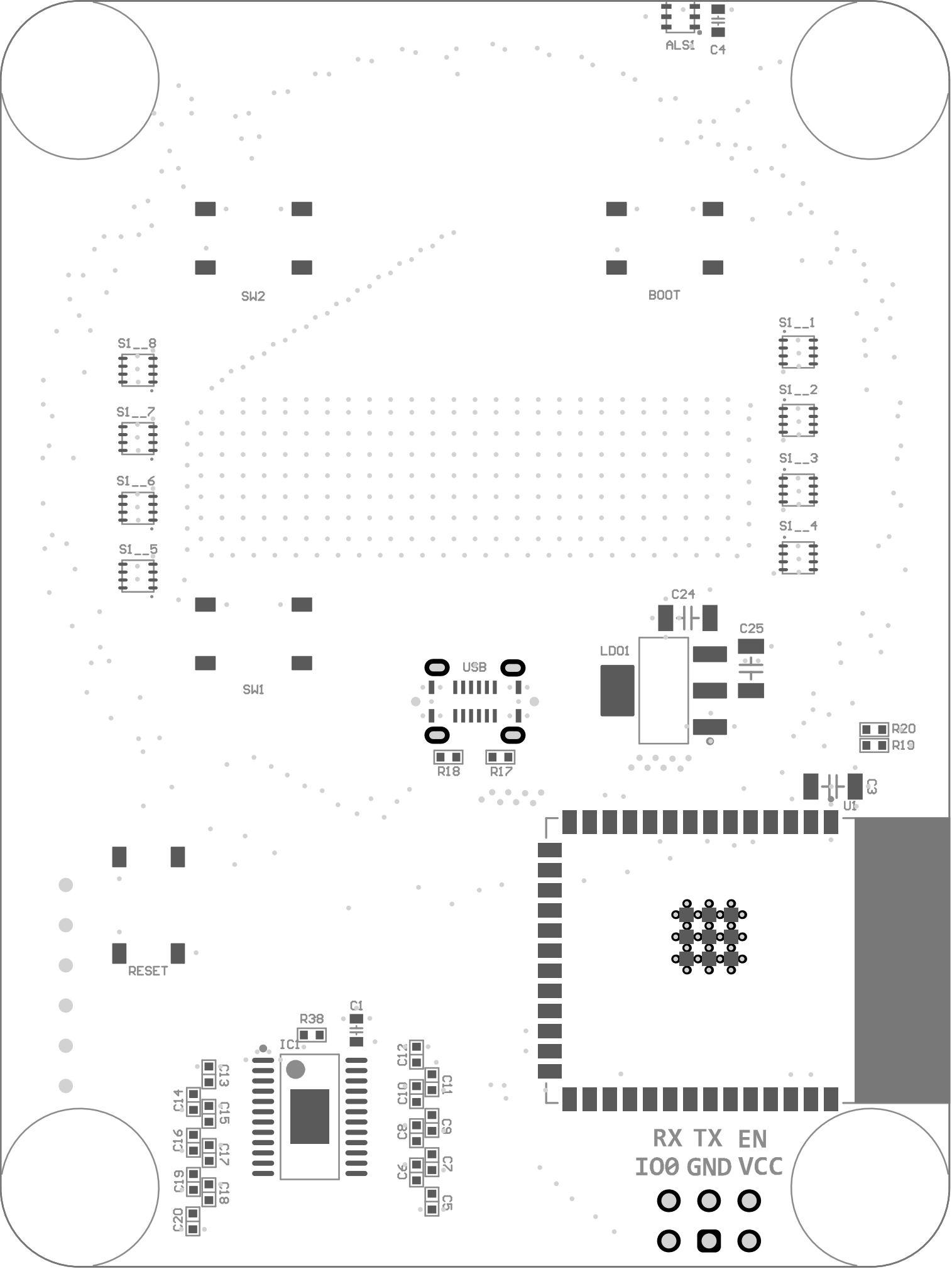


Dual anode switch	Revision * Saved on 31 Oct 2025
chs	Sheet 2 of 2



Clock Face	Revision *
	Saved on 31 Oct 2025
chs	Sheet * of *




ALS1
C4
SW2
BOOT
S1__8
S1__7
S1__6
S1__5
S1__1
S1__2
S1__3
S1__4
C24
C25
LDO1
SW1
USB
R18
R17
R20
R19
C3
U1
RESET
R38
C1
IC1
C12
C10
C11
C8
C9
C6
C2
C5
C13
C14
C15
C16
C17
C19
C18
C20
RX TX EN
IO0 GND VCC

Electrical Rules Check Report

Class	Document	Message
		Successful Compile for clock_led.PrjPcb

Design Rules Verification Report

Filename : E:\dev\clock_monsieur\pcb\clock_led.PcbDoc

Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.102mm) (All),(All)	0
Clearance Constraint (Gap=0.102mm) (InNetClass('K[0..15]')),(InNetClass('K[0..15]')	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.076mm) (Max=1mm) (Preferred=0.102mm) (All	0
Routing Layers(All)	0
Routing Via (Templates Used To Check Via: GND_VIA, LED_ROUTING, SW_ROUTING, TH_TEST_VIA, v70h30m0	0
Differential Pairs Uncoupled Length using the Gap Constraints (Min=0.254mm) (Max=0.254mm) (Prefered=0.254mm)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm	0
Hole Size Constraint (Min=0.025mm) (Max=6mm) (All)	0
Pads and Vias to follow the Drill pairs settings	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.1mm) (All),(All)	0
Silk To Solder Mask (Clearance=0mm) (False),(All)	0
Silk to Silk (Clearance=0mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Component Clearance Constraint (Horizontal Gap = 0.125mm, Vertical Gap = 0.254mm) (All),(All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All	0
Total	0