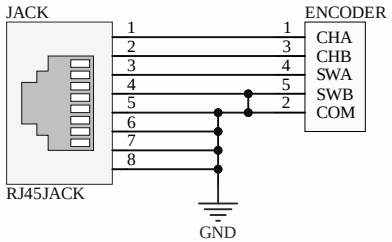
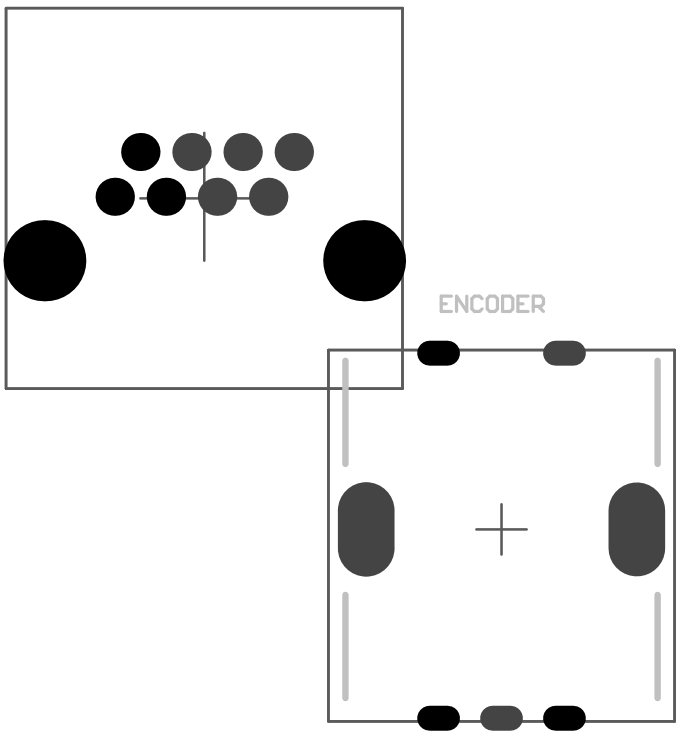


*	Revision * Saved on 18/09/2023
*	Sheet * of *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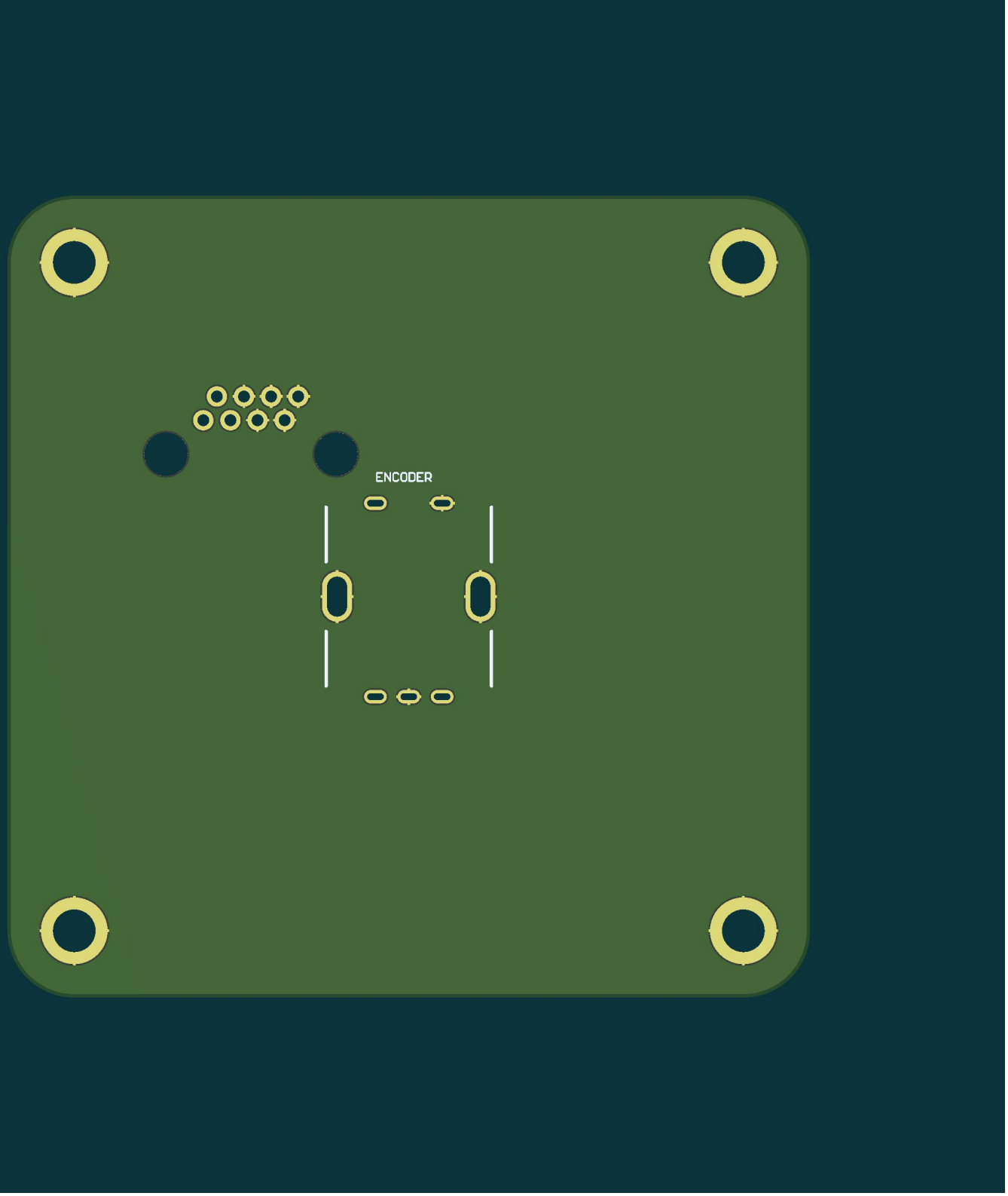
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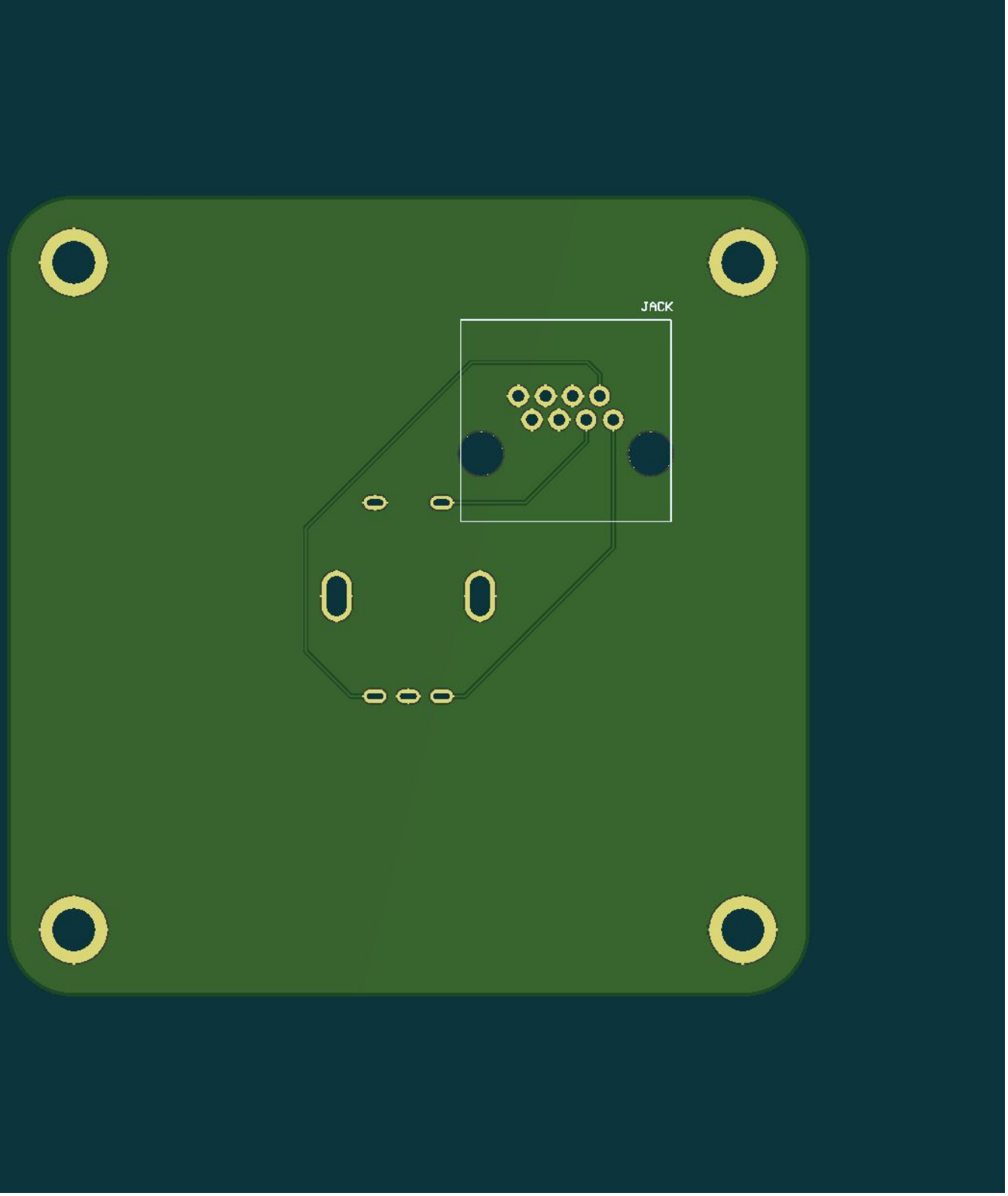
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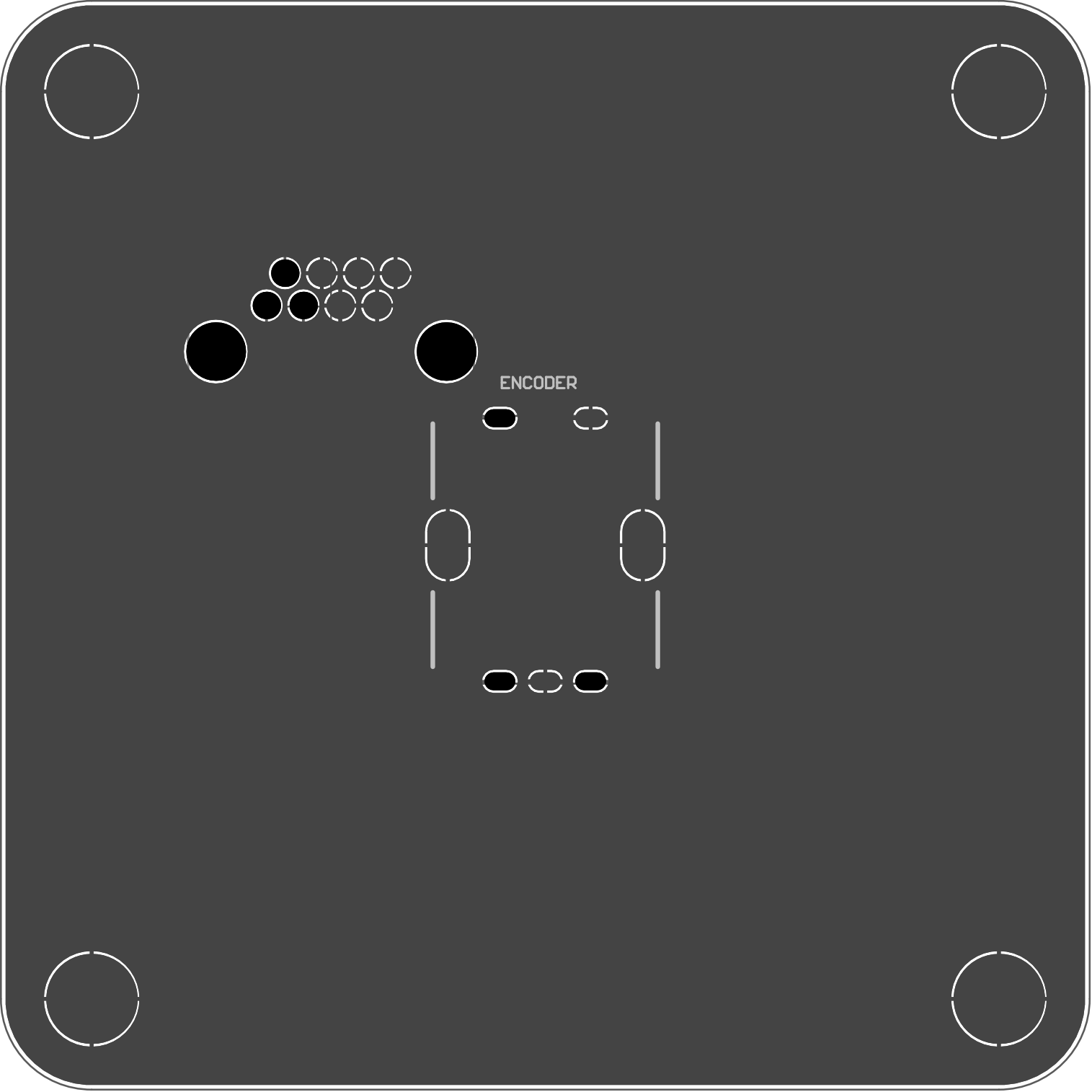
ENCODER

Design Rules Verification Repor

Filename : U:\dev\light_driver\pcb\controller\controller.PcbDoc

Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=5mil) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=6mil) (Max=10mil) (Preferred=10mil) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4	0
Hole Size Constraint (Min=0.984mil) (Max=157.48mil) (All)	0
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=10mil) (All),(All)	0
Silk To Solder Mask (Clearance=10mil) (IsPad),(All)	0
Silk to Silk (Clearance=10mil) (All),(All)	0
Net Antennae (Tolerance=0mil) (All)	0
Board Clearance Constraint (Gap=0mil) (All)	0
Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	0
Total	0