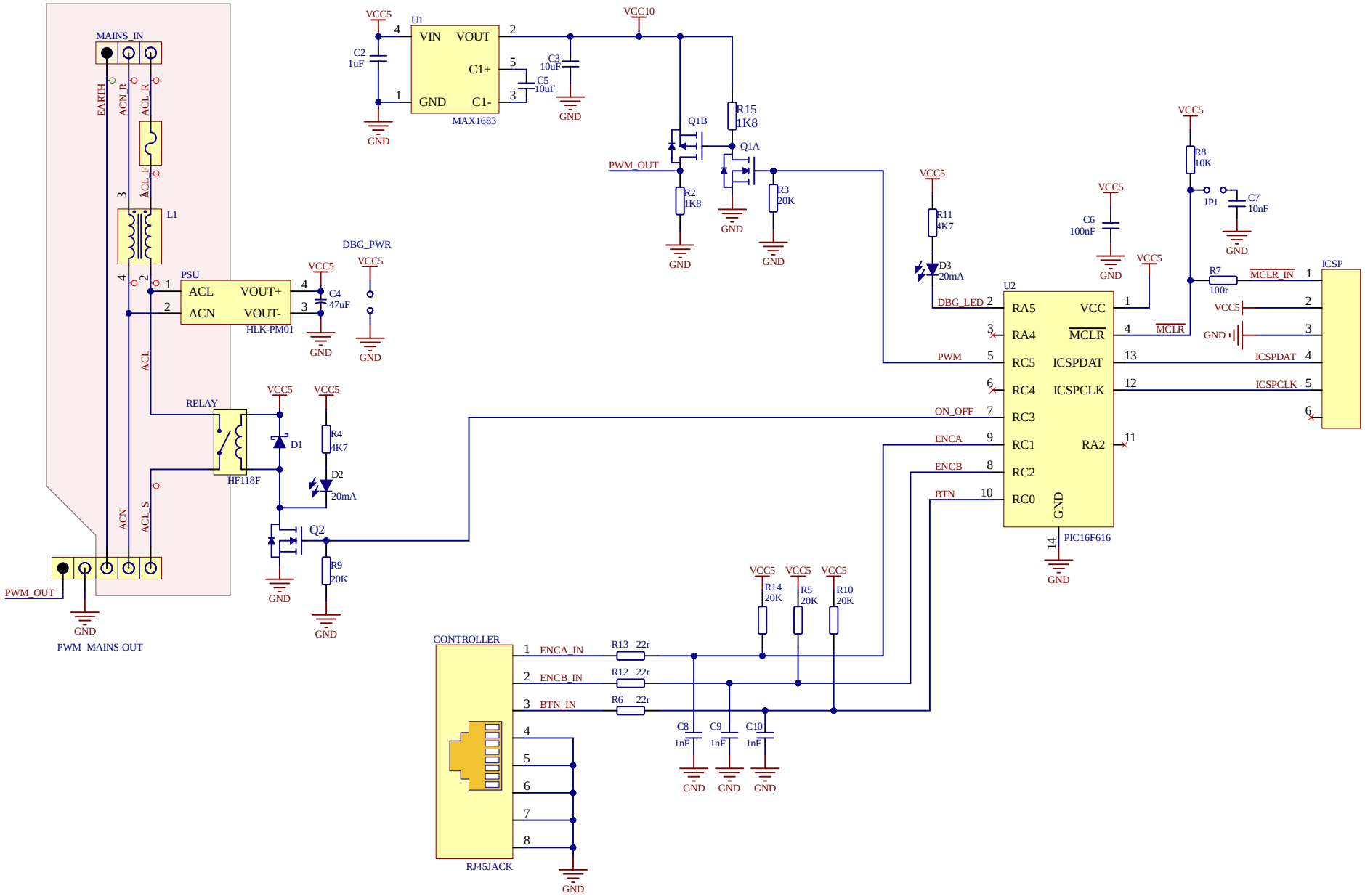
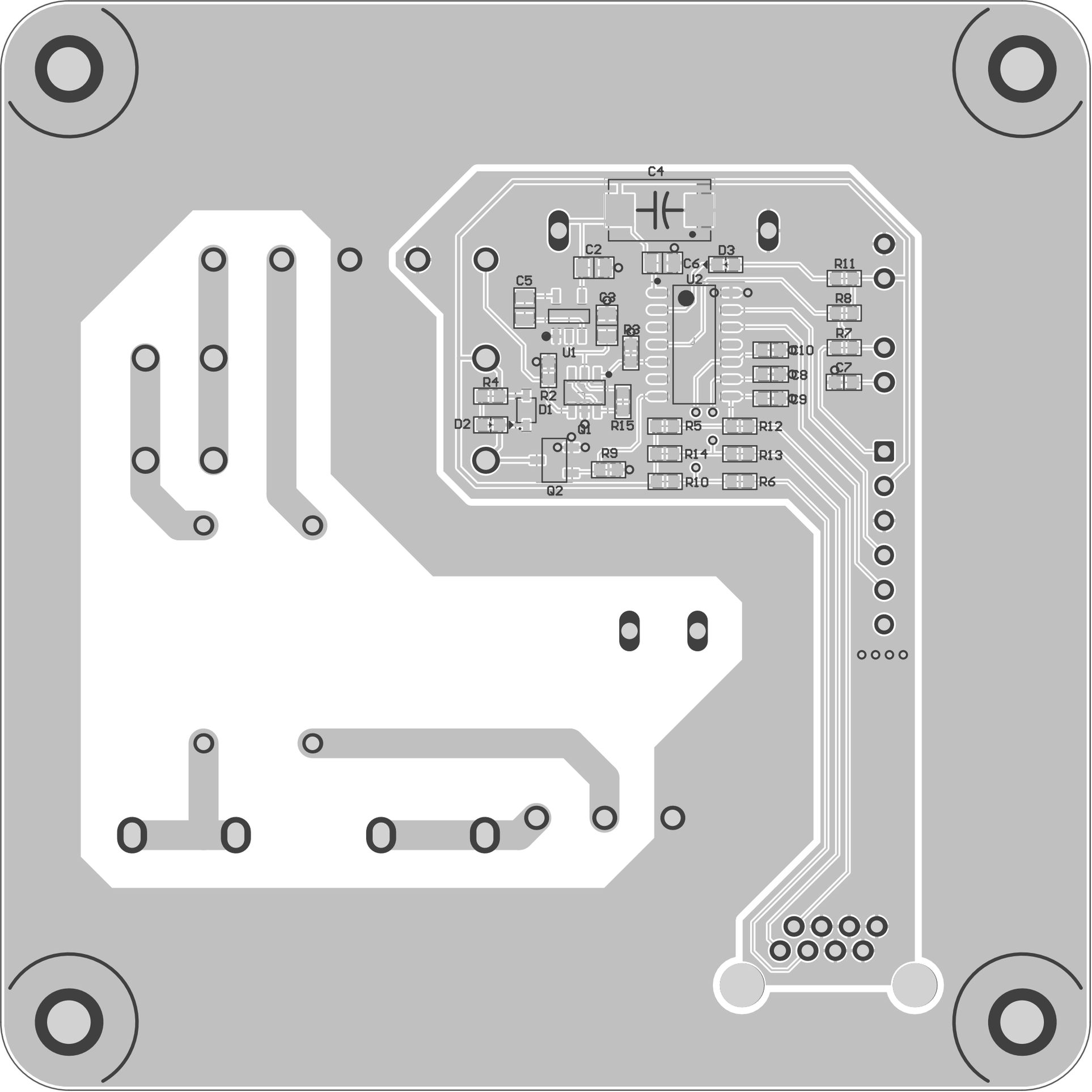
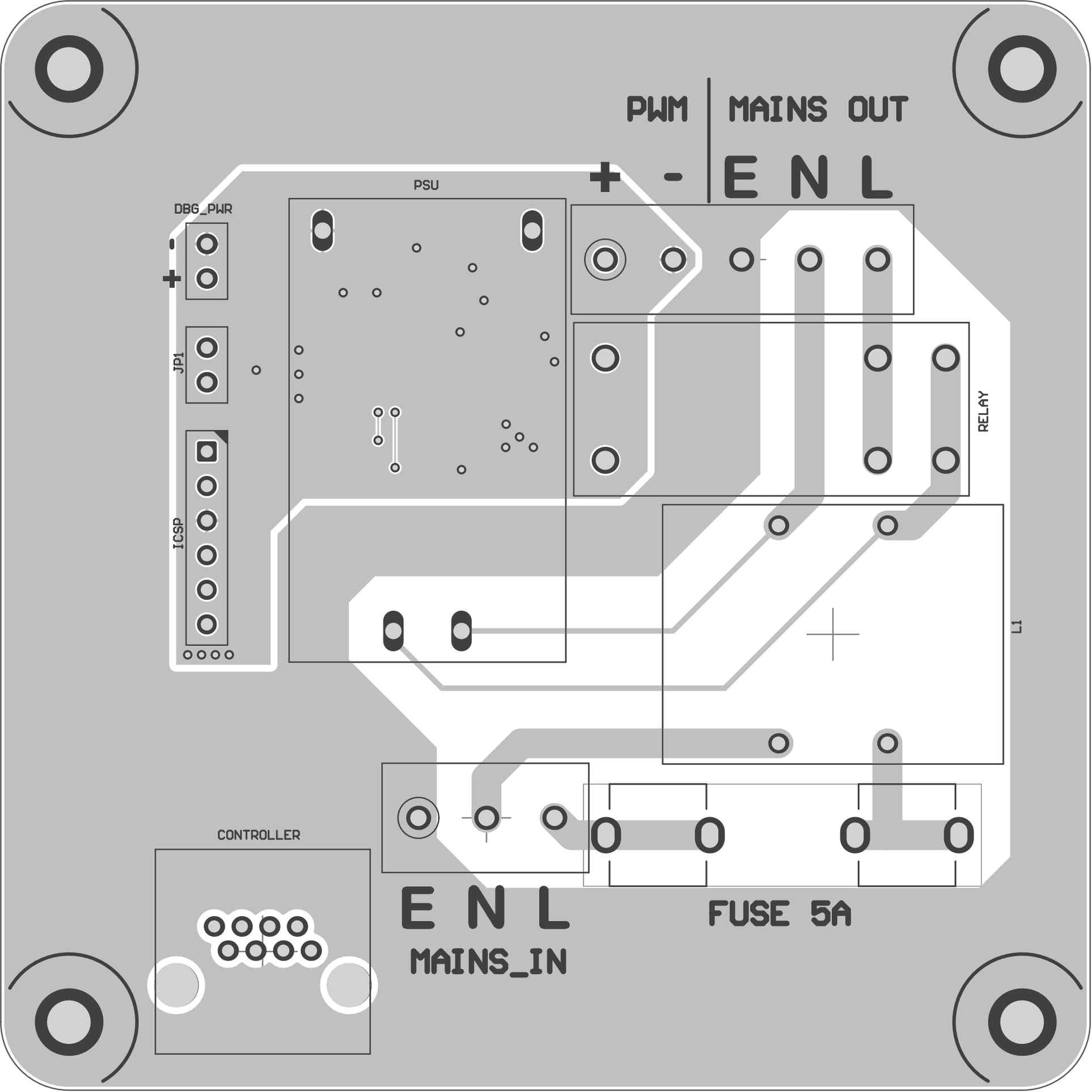
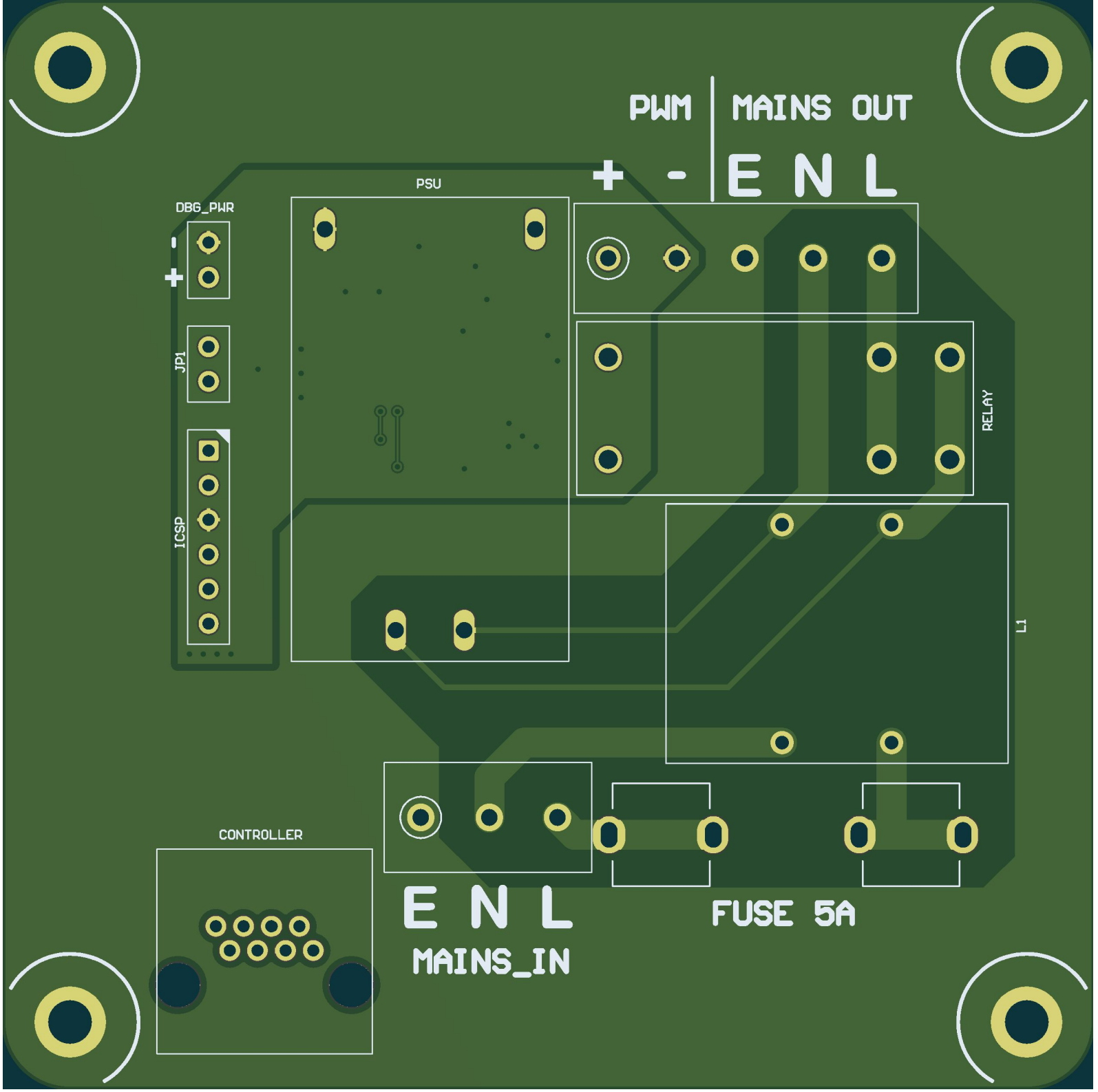


*	Revision *
	Saved on 24/09/2023
*	Sheet * of *


C4
C2
C6
D3
R11
C5
U2
C3
R8
R3
R7
U1
C10
C8
C9
C7
R4
R2
D1
D2
Q1
R15
R5
R12
R14
R13
R9
R10
R6
Q2


PWM
MAINS OUT
+
-
E N L
PSU
DBG_PWR
JP1
ICSP
RELAY
L1
CONTROLLER
E N L
MAINS_IN
FUSE 5A


PWM
MAINS OUT
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E N L
PSU
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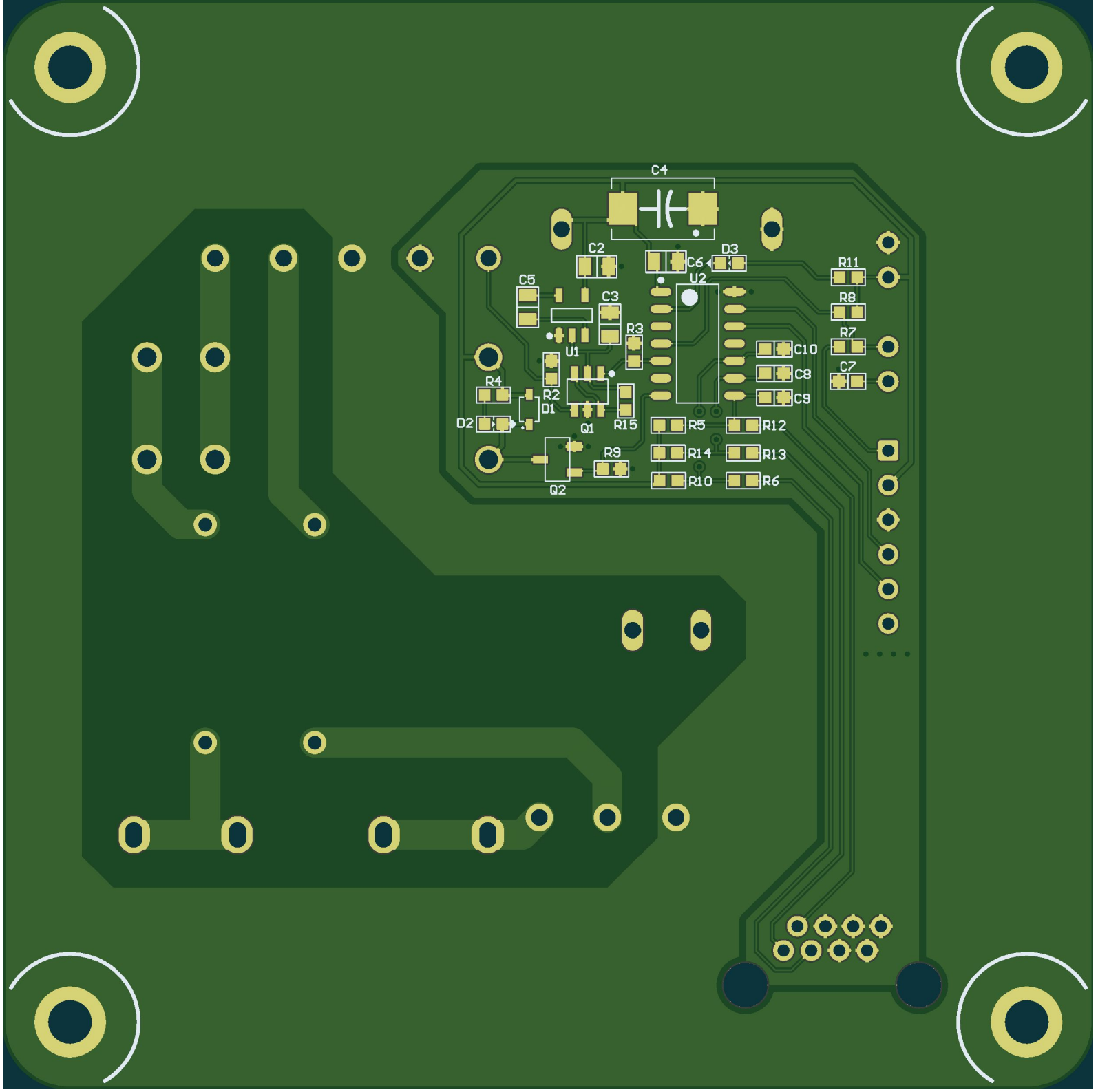
C4
C2
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R11
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U2
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R8
R3
R7
U1
C10
C7
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R2
C8
D1
C9
D2
Q1
R15
R5
R12
R14
R13
R9
R10
R6
Q2

Electrical Rules Check Report

Class	Document	Message
		Successful Compile for

Design Rules Verification Report

Filename : U:\dev\light_driver\pcb\driver\driver.PcbDoc

Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=5mil) (All),(All)	0
Clearance Constraint (Gap=19.685mil) (InNet('EARTH')),(IsKeepOut OR (NOT InNetClass('MAINS'))	0
Clearance Constraint (Gap=98.425mil) (InNetClass('MAINS')),(All)	0
Clearance Constraint (Gap=9.842mil) (InNet('EARTH')),(IsPad AND (NOT PadIsPlated)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=10mil) (Max=157.48mil) (Preferred=10mil) (InNetClass('MAINS')	0
Width Constraint (Min=5mil) (Max=20mil) (Preferred=5mil) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4	0
Minimum Annular Ring (Minimum=5.906mil) (All)	0
Hole Size Constraint (Min=15.748mil) (Max=196.85mil) (All)	0
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=3.937mil) (All),(All)	0
Silk To Solder Mask (Clearance=0mil) (All),(All)	0
Silk to Silk (Clearance=0mil) (All),(All)	0
Net Antennae (Tolerance=0mil) (All)	0
Board Clearance Constraint (Gap=0mil) (NOT (OnLayer('Top Overlay') OR OnLayer('Bottom Overlay'))	0
Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	0
Total	0