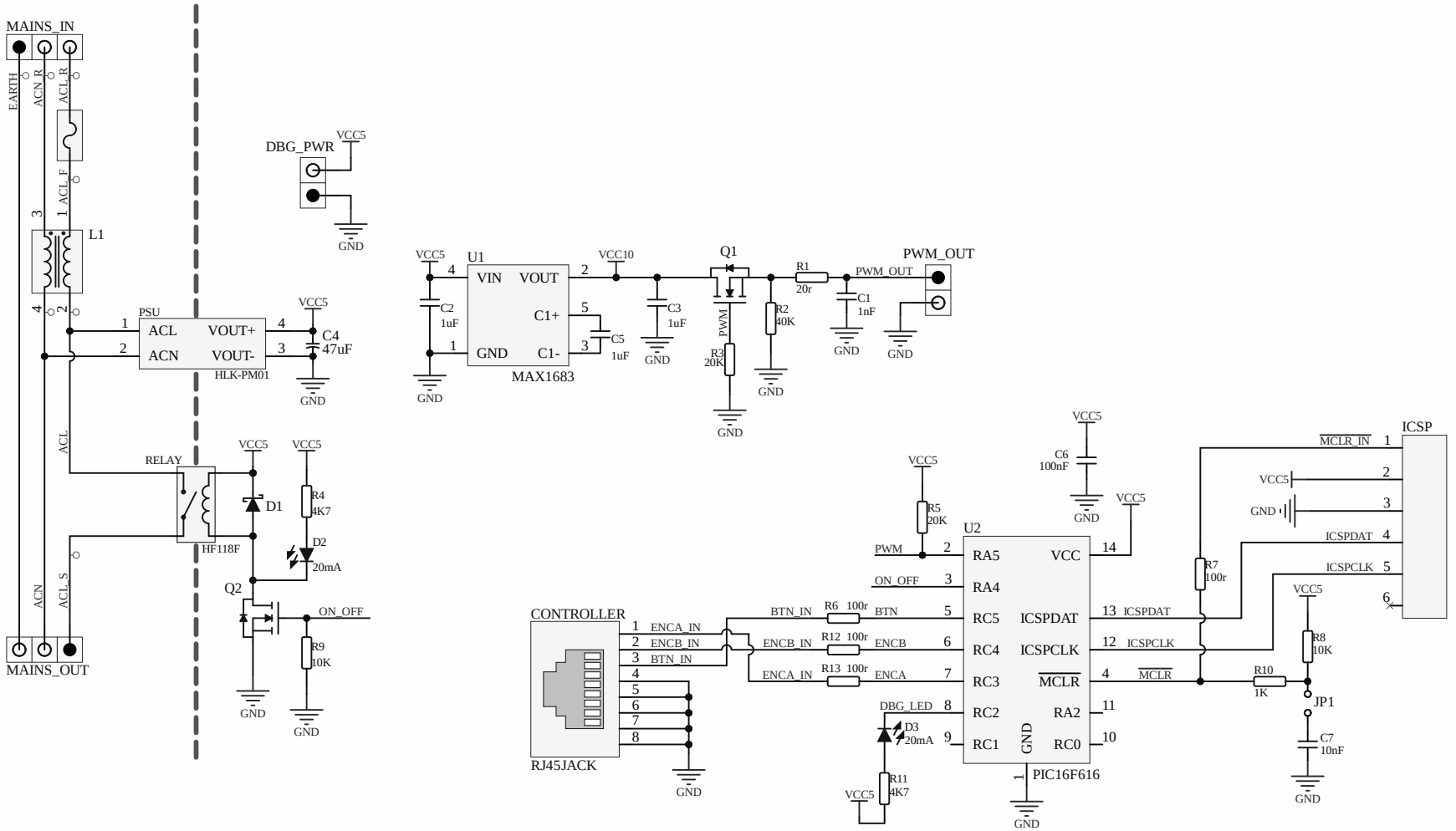
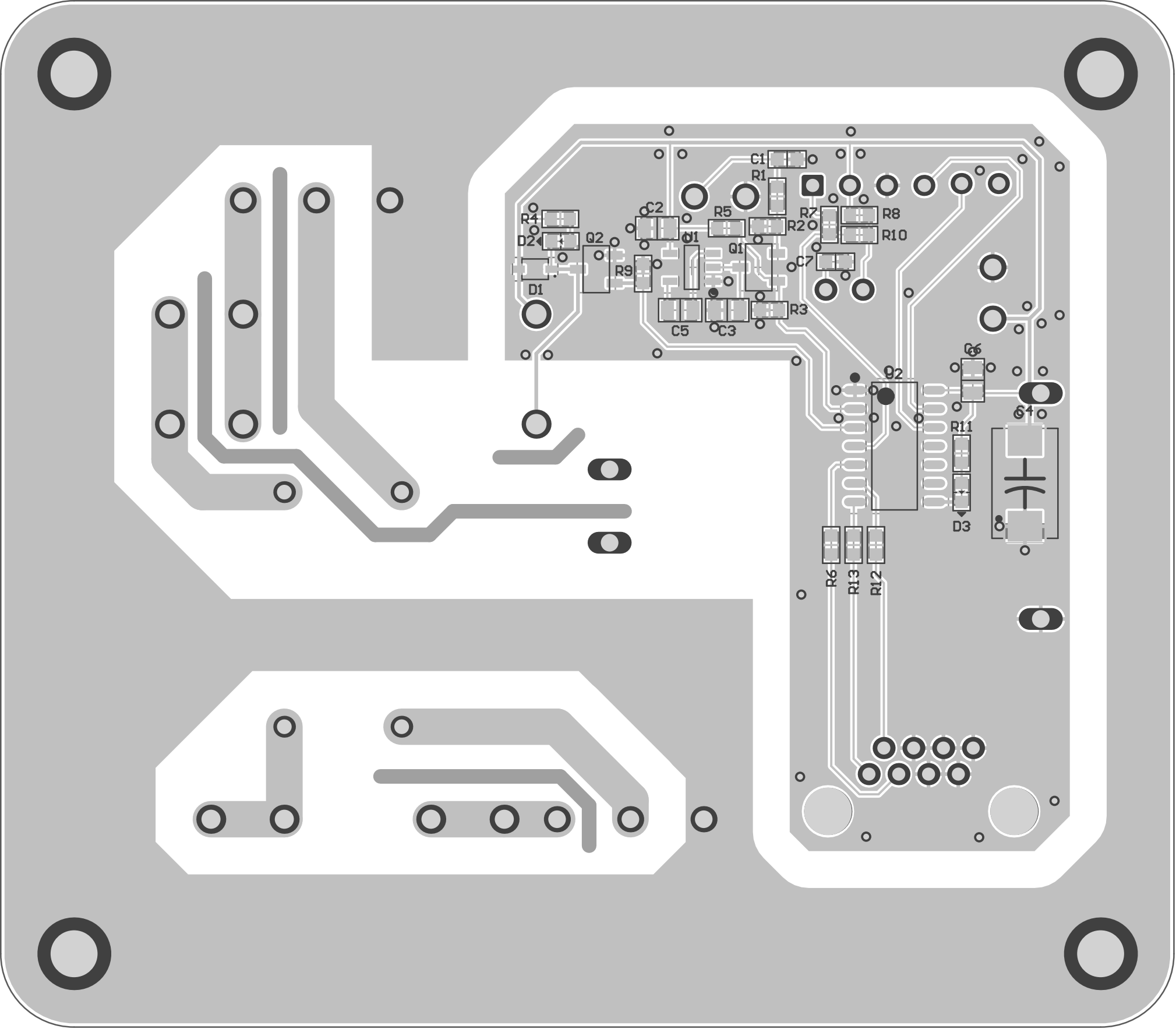
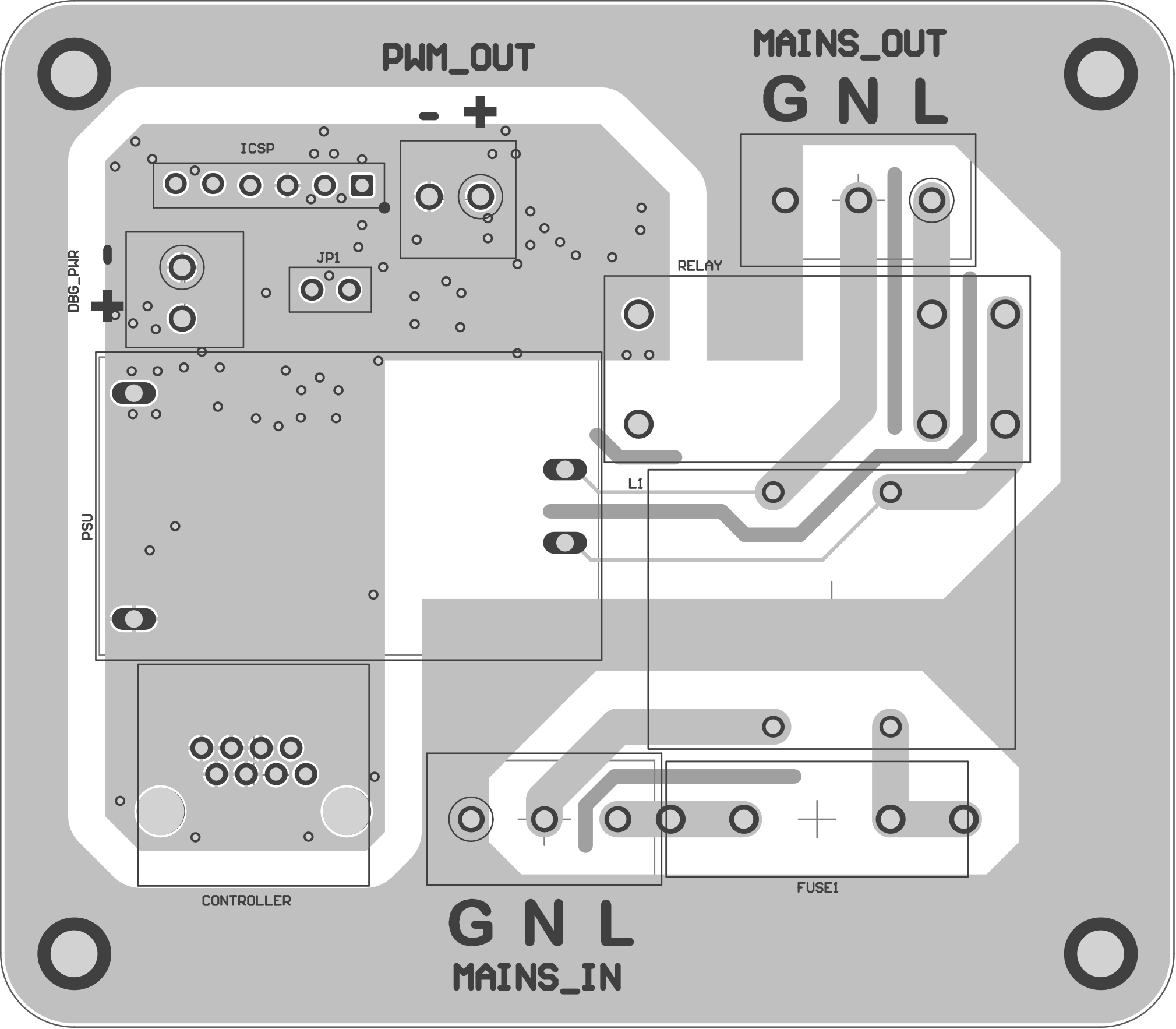
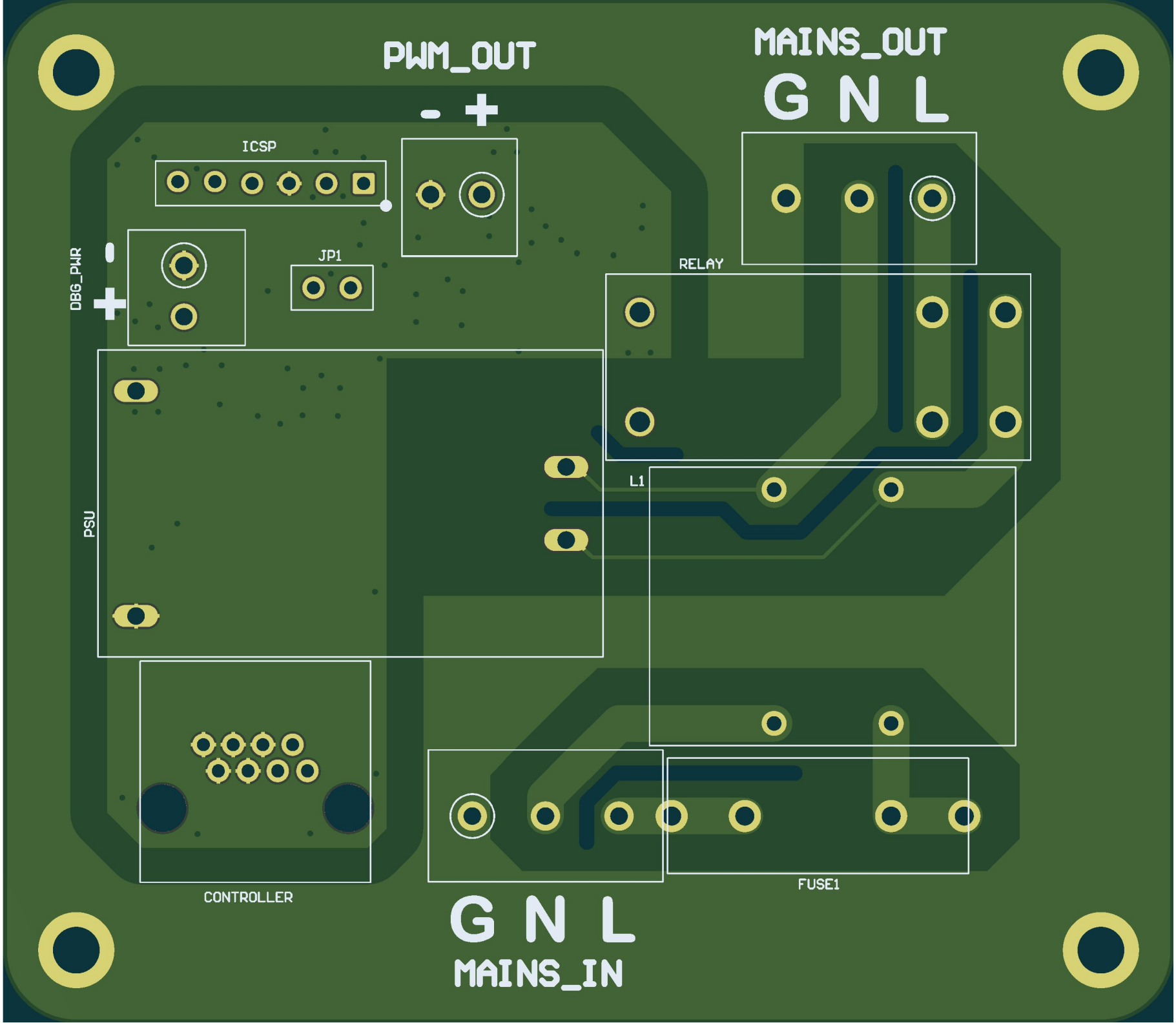
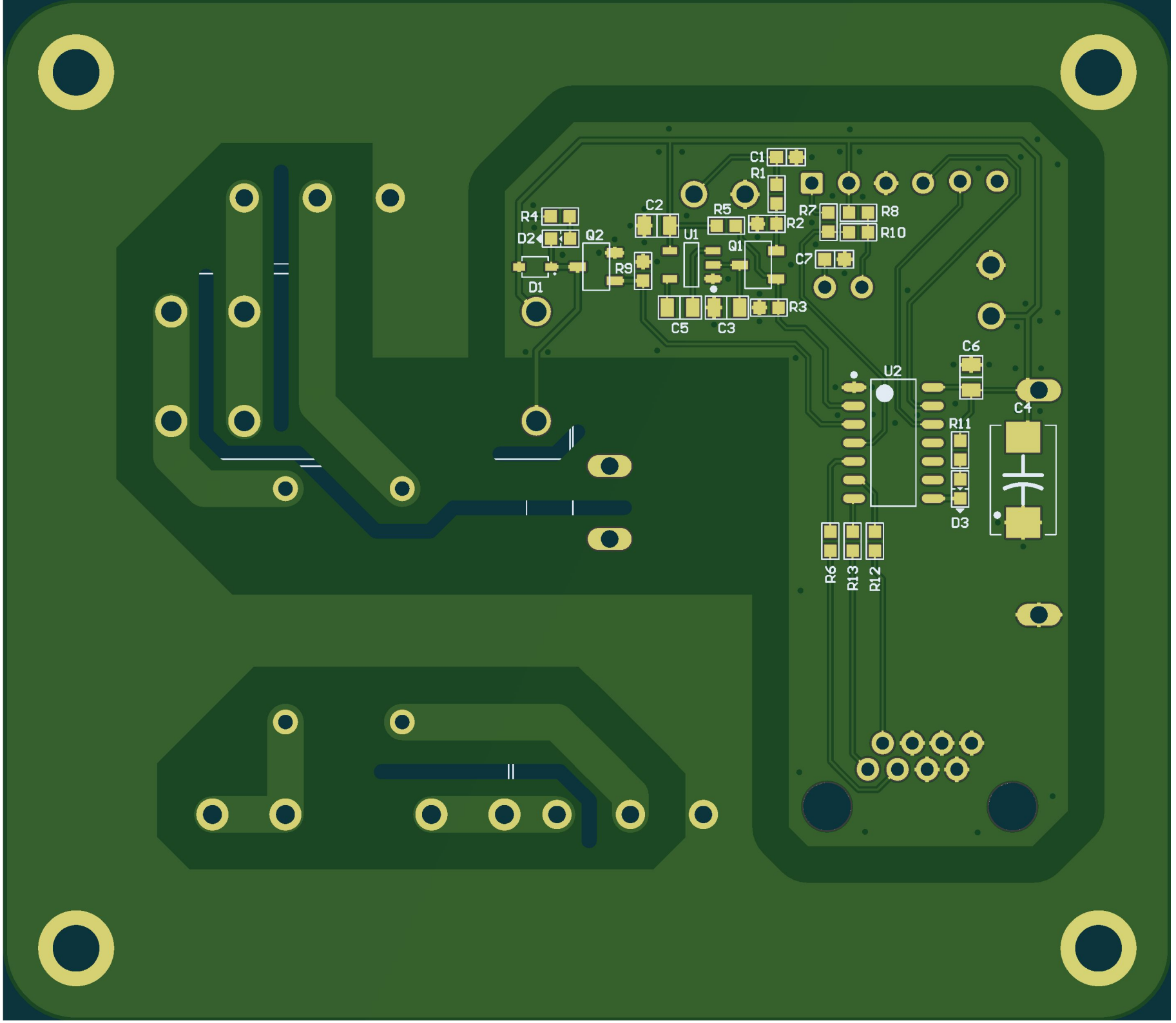


*	Revision *
	Saved on 19/09/2023
*	Sheet * of *


C1
R1
R4
D2
Q2
C2
R5
R7
R8
R2
R10
D1
R9
Q1
C7
R3
C5
C3
Q2
Q4
Q6
R11
D3
R6
R13
R12


PWM_OUT
- +
MAINS_OUT
G N L
ICSP
JP1
DBG_PWR
RELAY
L1
PSU
CONTROLLER
FUSE1
G N L
MAINS_IN


PWM_OUT
- +
MAINS_OUT
G N L
ICSP
JP1
DBG_PWR
RELAY
L1
PSU
CONTROLLER
FUSE1
G N L
MAINS_IN


C1
R1
R4
D2
Q2
C2
U1
R5
R2
R7
R8
R10
Q1
C7
D1
R9
C5
C3
R3
C6
U2
C4
R11
D3
R6
R13
R12

Electrical Rules Check Report

Class	Document	Message
		Successful Compile for

Design Rules Verification Report

Filename : U:\dev\light_driver\pcb\driver\driver.PcbDoc

Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.254mm) (InNet('EARTH')),(IsKeepOut	0
Clearance Constraint (Gap=0.152mm) (All),(All)	0
Clearance Constraint (Gap=2.5mm) (InNet('EARTH')),(All	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.254mm) (Max=4mm) (Preferred=0.254mm) (InNetClass('MAINS')	0
Width Constraint (Min=0.127mm) (Max=0.508mm) (Preferred=0.127mm) (All	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm	0
Minimum Annular Ring (Minimum=0.15mm) (All)	0
Hole Size Constraint (Min=0.4mm) (Max=5mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.1mm) (All),(All)	0
Silk To Solder Mask (Clearance=0mm) (All),(All)	0
Silk to Silk (Clearance=0mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) (All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All	0
Total	0