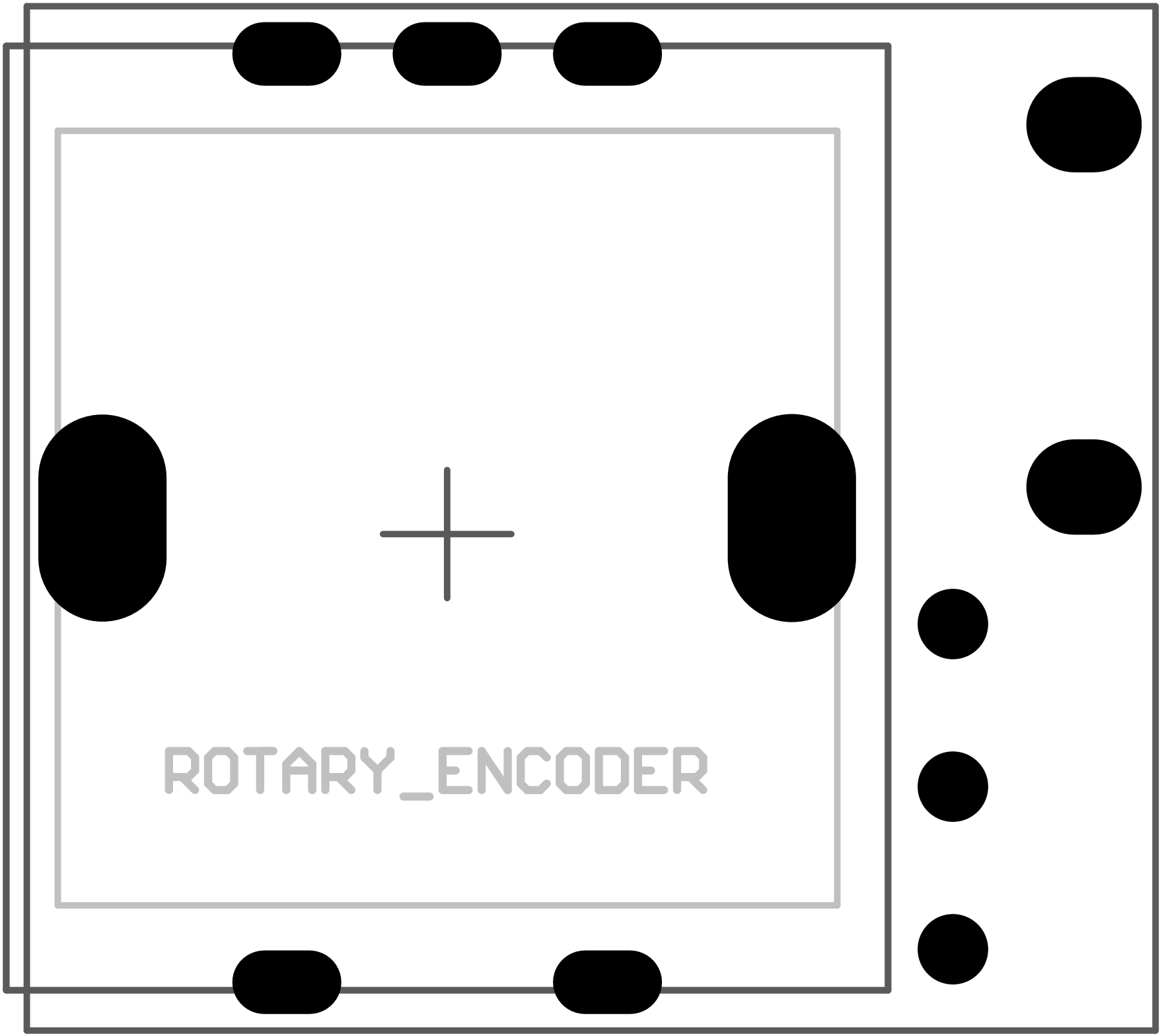
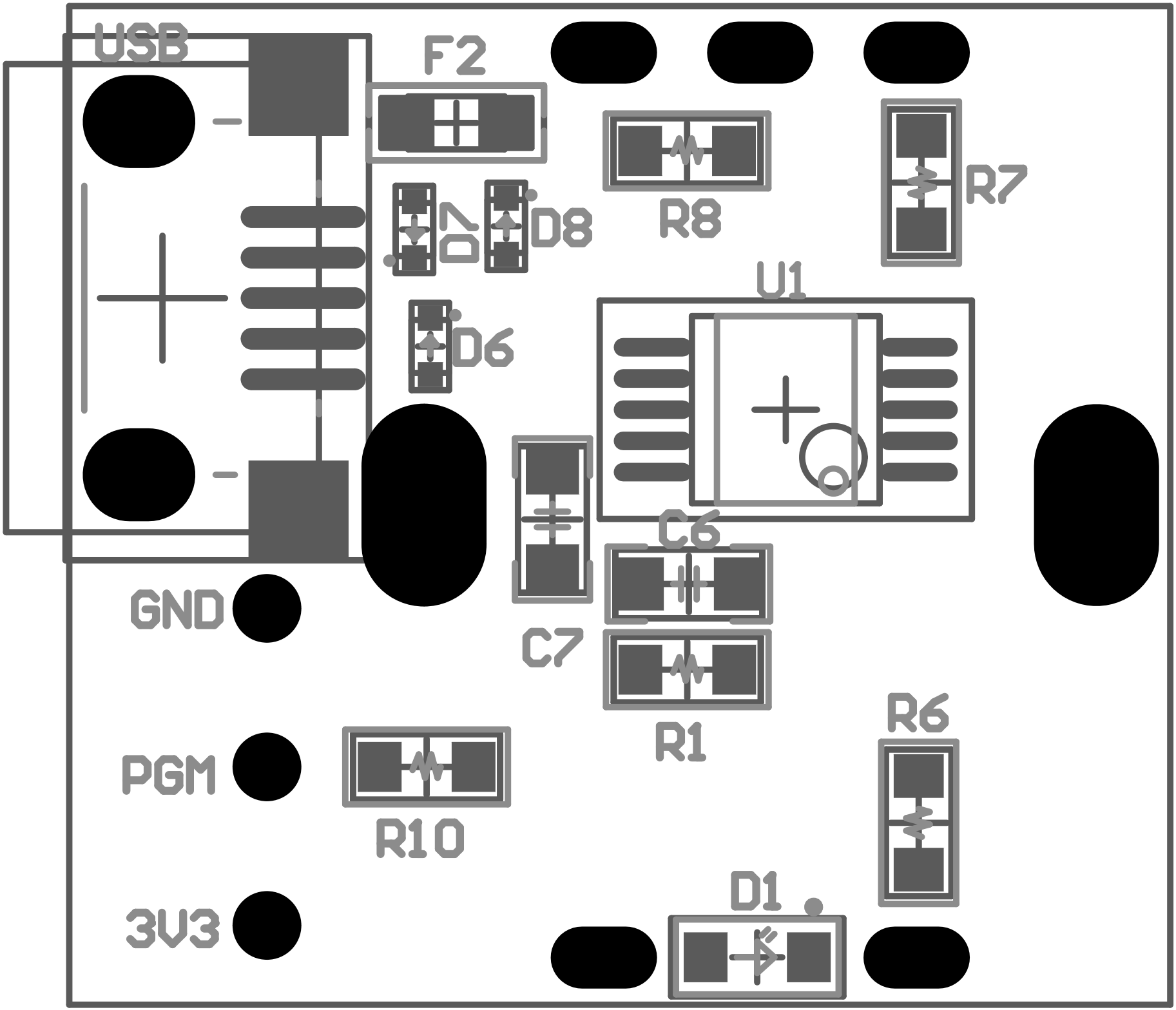

ROTARY_ENCODER


USB
F2
D8
R8
R7
U1
D6
C6
C7
GND
R1
R6
PGM
R10
D1
3V3

Comment	Designator	Footprint	JLCPCB Part #
1uF	C6	MLCC_0603	C29936
1uF	C7	MLCC_0603	C29936
20mA	D1	SMT_LED_0603	C205445
TVS_DIODE	D6	TVS_DIODE	C151980
TVS_DIODE	D7	TVS_DIODE	C151980
TVS_DIODE	D8	TVS_DIODE	C151980
1A	F2	FUSE 0603	C210357
680r	R1	SMT_RES_0603	C23228
220r	R6	SMT_RES_0603	C27592
220r	R7	SMT_RES_0603	C27592
220r	R8	SMT_RES_0603	C27592
10k	R10	SMT_RES_0603	C25804
CH554E	U1	MSOP10	C111293
USB Micro	USB	USB MICRO B	C397452

Design Rules Verification Report

Filename : E:\dev\hid_kbd\pcb\wch554g\wch554g.PcbDoc

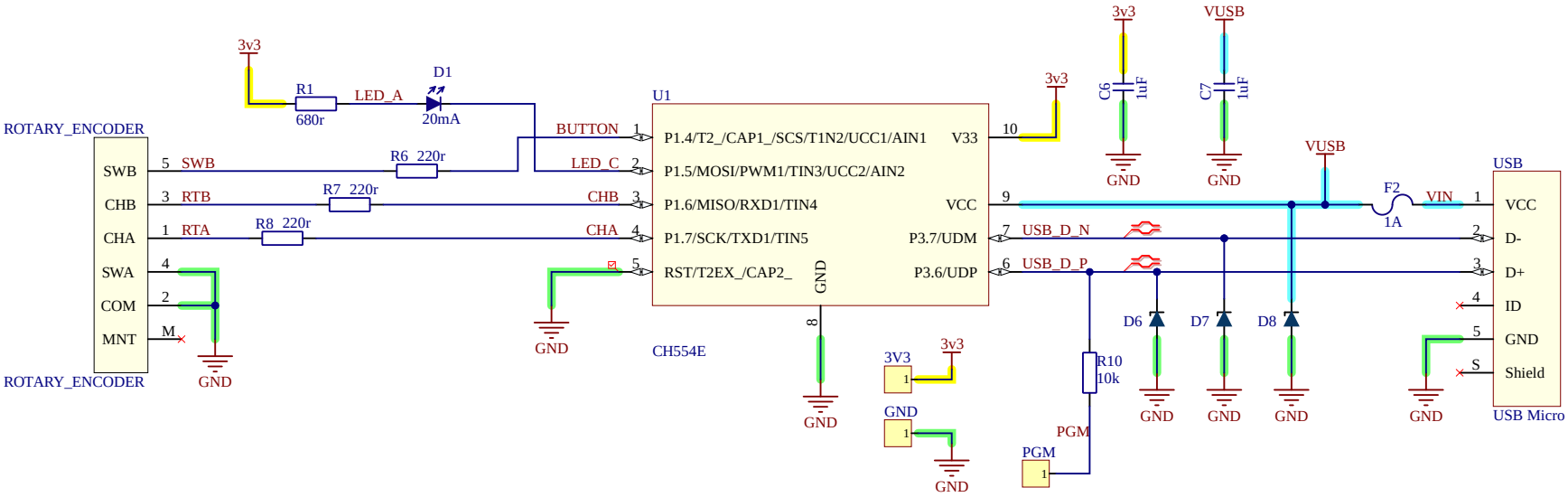
Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=6mil) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=4mil) (Max=30mil) (Preferred=5mil) (All)	0
Routing Layers(All)	0
Routing Via (Templates Used To Check Via: GND_VIA) (All)	0
Differential Pairs Uncoupled Length using the Gap Constraints (Min=4mil) (Max=10mil) (Prefered=10mil) and Widt	0
Power Plane Connect Rule(Relief Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4	0
Hole Size Constraint (Min=11.811mil) (Max=393.701mil) (All)	0
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=3.9mil) (All),(All)	0
Silk To Solder Mask (Clearance=10mil) (False),(False)	0
Silk to Silk (Clearance=0mil) (All),(All)	0
Net Antennae (Tolerance=0mil) (All)	0
Board Clearance Constraint (Gap=0mil) ((OnLayer('Top Layer') AND OnLayer('Bottom Layer'))	0
Component Clearance Constraint (Horizontal Gap = 0mil, Vertical Gap = 10mil) (All),(All)	0
Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	0
Total	0

Electrical Rules Check Report

Class	Document	Message
		Successful Compile for



Knob CH554G V2	Revision 1 Saved on 19/10/2024
skilbeck.com	Sheet 1 of 1