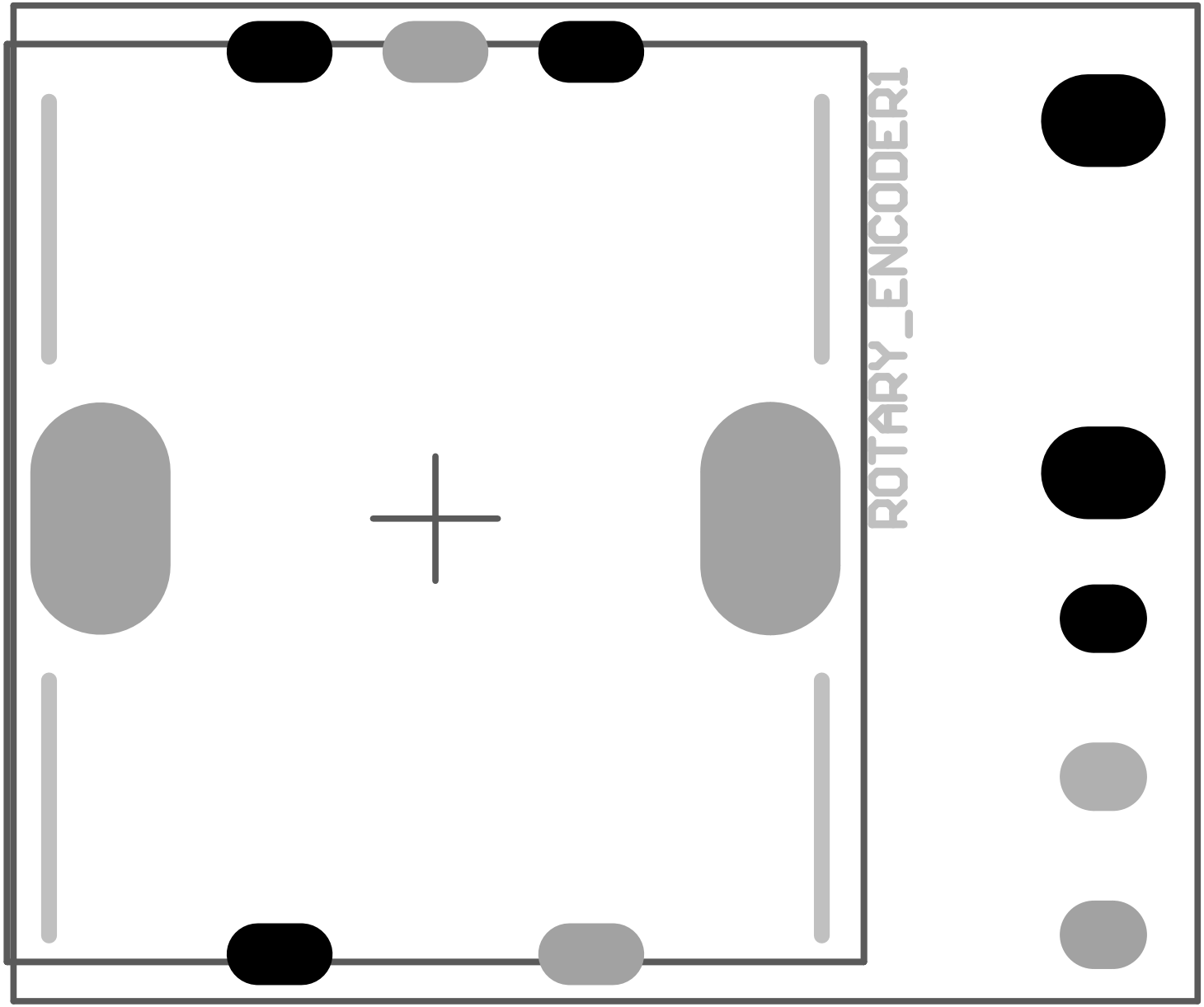
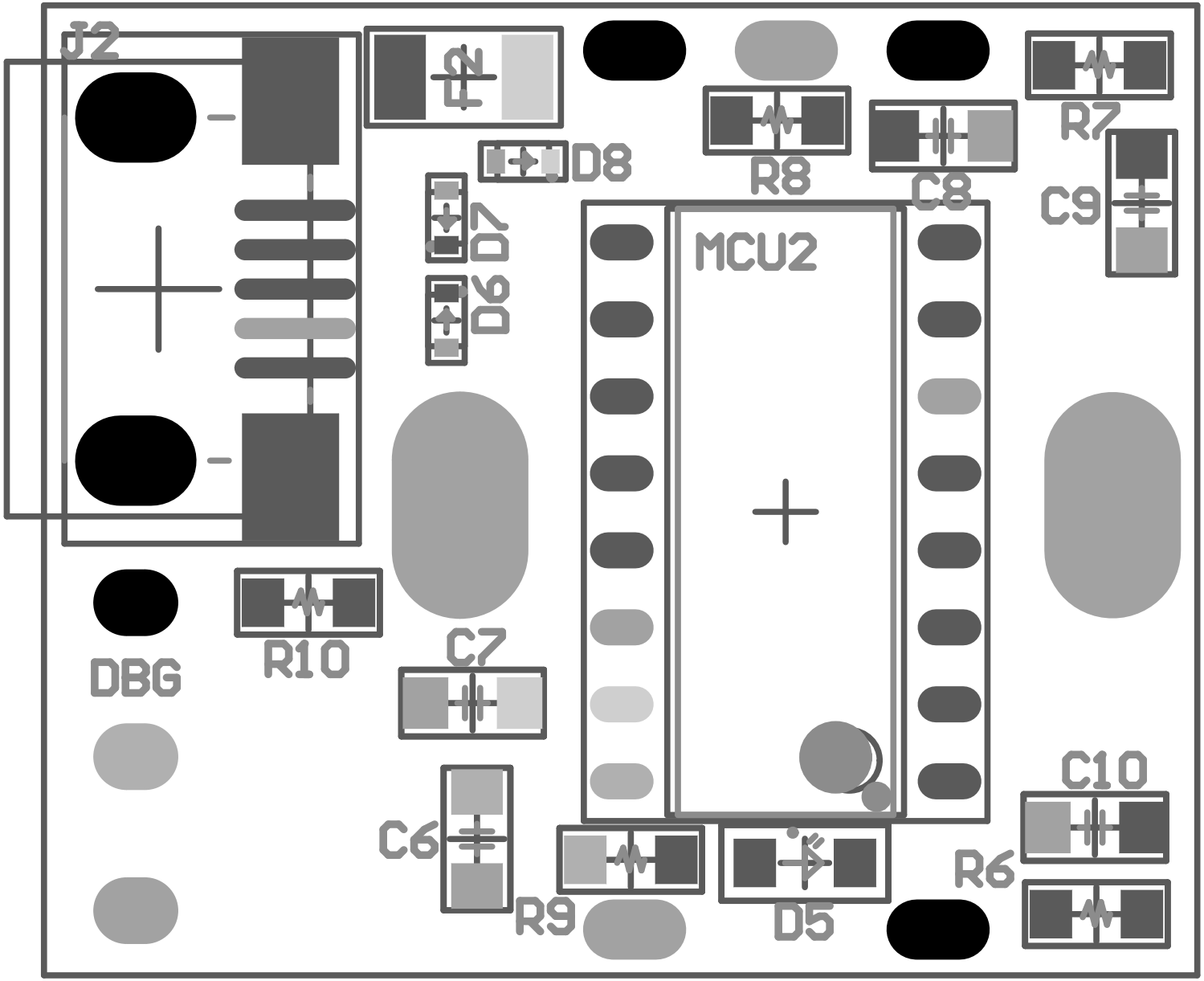

ROTARY_ENCODER1


J2
C11
D8
R8
C8
R7
C9
D7
D6
MCU2
DBG
R10
C7
C6
R9
D5
C10
R6

Footprint	Quantity	Designator	Description	Value	JLCPCB Part #
MLCC 0603	2	C6, C7	MLCC	1uF	C105524
MLCC 0603	3	C8, C9, C10	MLCC	10nF	C519509
SMT LED 0603	1	D5	LED	20mA	C434424
SODFL 98x40 2 pin	3	D6, D7, D8	TVS Diode	TVS_DIODE	C384848
FUSE_0805	1	F2	FUSE	1A	C70061
USB Micro B Receptacle	1	J2	USB Micro B Receptacle	USB	C397452
SOP16 x1.27	1	MCU2	CH554G SOP16 MCU	CH554G	C114295
0603 SMT Resistor	3	R6, R7, R8	Resistor	120r	C22787
0603 SMT Resistor	1	R9	Resistor	680r	C23228
0603 SMT Resistor	1	R10	Resistor	10k	C25804

Design Rules Verification Report

Filename : U:\dev\hid_kbd\pcb\wch554g\wch554g.PcbDoc

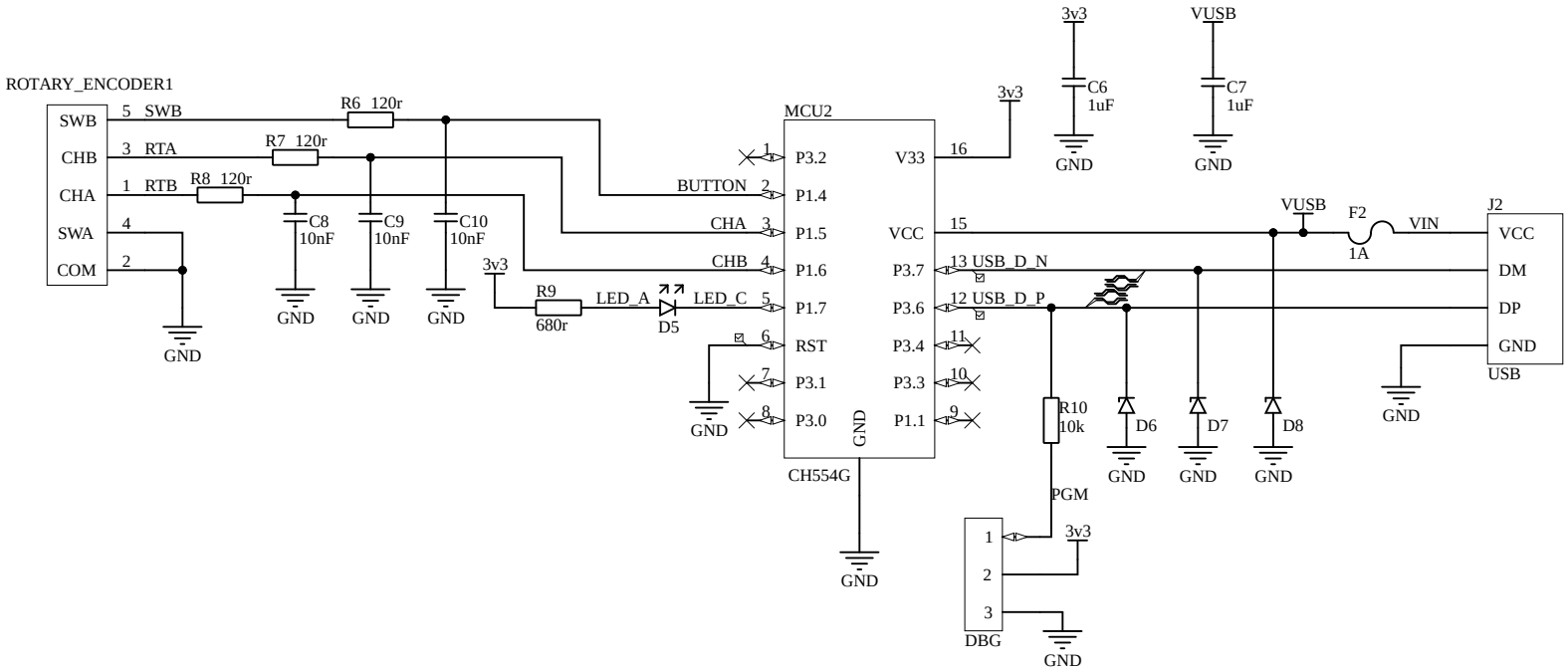
Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=6mil) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=4mil) (Max=30mil) (Preferred=5mil) (All)	0
Routing Layers(All)	0
Routing Via (Templates Used To Check Via: GND_VIA) (All)	0
Differential Pairs Uncoupled Length using the Gap Constraints (Min=4mil) (Max=10mil) (Prefered=10mil) and Widt	0
Power Plane Connect Rule(Relief Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4	0
Hole Size Constraint (Min=11.811mil) (Max=393.701mil) (All)	0
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=4mil) (All),(All)	0
Silk To Solder Mask (Clearance=10mil) (False),(False)	0
Silk to Silk (Clearance=0mil) (All),(All)	0
Net Antennae (Tolerance=0mil) (All)	0
Board Clearance Constraint (Gap=0mil) (All)	0
Component Clearance Constraint (Horizontal Gap = 0mil, Vertical Gap = 10mil) (All),(All)	0
Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	0
Total	0

Electrical Rules Check Report

Class	Document	Message
		Successful Compile for



*	Revision * Saved on 05/06/2022
*	Sheet * of *