





| Designator | Quantity | Comment | Description    | Footprint              | JLCPCB Part # |
|------------|----------|---------|----------------|------------------------|---------------|
| U1         |          | 1       | CH554E         | MSOP10 3x3 x 0.5       | C111293       |
| F1         |          | 1 1A    | FUSE           | FUSE_0805              | C70061        |
| D4         |          | 1       | LED            | SMT LED 0603           | C434424       |
| C1, C2     |          | 2 1uF   | MLCC           | MLCC 0603              | C105524       |
| C3, C4, C5 | 3        | 3 10nF  | MLCC           | MLCC 0603              | C519509       |
| R1, R2, R3 | 3        | 3 120r  | Resistor       | 0603 SMT Resistor      | C22787        |
| R4         |          | 1 10k   | Resistor       | 0603 SMT Resistor      | C25804        |
| R5         |          | 1 680r  | Resistor       | 0603 SMT Resistor      | C23228        |
| D1, D2, D3 |          | 3       | TVS Diode      | SODFL 98x40 2 pin      | C384848       |
| J1         |          | 1       | USB Receptacle | USB Micro B Receptacle | C397452       |

**Design Rules Verification Report**Filename: U:\dev\hid\_kbd\pcb\wch554e\wch554e\wch554e.PcbDoc

Warnings 0 Rule Violations 0

## Warnings Total

| Rule Violations   |   |
|---|---|
| Clearance Constraint (Gap=0.152mm) (All), (All)   | 0 |
| Short-Circuit Constraint (Allowed=No) (All),(All)   | 0 |
| Un-Routed Net Constraint ( (All) )  | 0 |
| Modified Polygon (Allow modified: No), (Allow shelved: No)  | 0 |
| Width Constraint (Min=0.127mm) (Max=2.54mm) (Preferred=0.254mm) (All                                    | 0 |
| Routing Via (Templates Used To Check Via: GND_VIA, routing_via) (All                                    | 0 |
| Power Plane Connect Rule(Relief Connect )(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm | 0 |
| Hole Size Constraint (Min=0.4mm) (Max=3.5mm) (All   | 0 |
| Hole To Hole Clearance (Gap=0.254mm) (All), (All)   | 0 |
| Minimum Solder Mask Sliver (Gap=0.1mm) (All),(All)  | 0 |
| Net Antennae (Tolerance=0mm) (All)  | 0 |
| Board Clearance Constraint (Gap=0mm) (All)  | 0 |
| Component Clearance Constraint ( Horizontal Gap = 0.152mm, Vertical Gap = 0.254mm ) (All),(All)         | 0 |
| Total   | 0 |

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## **Electrical Rules Check Report**

| Class   | Document       | Message   |
|---------|----------------|---|
| Warning | wch554e.SchDoc | GND contains IO Pin and Power Pin objects (Pin U1-5, Pin DBG-3, Pin U1-8) |
|         |                |   |

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## **Board Stack Report**

Stack Up

Layer Stack

| Layer | Board Layer Stack | Name                  | Material | Thickness | Constant |
|-------|-------------------|-----------------------|----------|-----------|----------|
| 1     |                   | Top Paste             |          |           |          |
| 2     |                   | Top Overlay           |          |           |          |
| 3     |                   | Top Solder            | SM-001   | 0.025mm   | 4        |
| 4     |                   | Top Layer             | Copper   | 0.035mm   |          |
| 5     |                   | Dielectric 1          | Core-043 | 0.680mm   | 4.3      |
| 6     |                   | Bottom Layer          | Copper   | 0.035mm   |          |
| 7     |                   | Bottom Solder         | SM-001   | 0.025mm   | 4        |
| 8     |                   | <b>Bottom Overlay</b> |          |           |          |
| 9     |                   | <b>Bottom Paste</b>   |          |           |          |
|       | Height: 0.801mm   |                       |          |           |          |