





Designator	Quantity	Value	Footprint	Detail	Notes	Supplier Part Number 1
C1, C11	2	2.2uF	MLCC_0805	MLCC 0805	Any suitable	
C3	1	1uF	CAPC1608X07L	MLCC 0603	Any suitable	
C8, C10	2	3.3nF	CAPC1608X07L	MLCC 0603	Any suitable	
С9	1	100nF	CAPC1608X07L	MLCC 0603	Any suitable	
D1, D2, D3	3		SODFL98X40-2L	SODFL, 0.6x1.0mm	Any suitable USB TVS diodes	C312244
LDO	1	200mA	SOT95P237X110-3L	SOT23x3 2.90x2.37mm Pitch 0.95mm	Or similar	C479053
LED	1	20mA	SMT_LED_0603	SMT LED 0603	Any suitable	
MCU	1		TSOP65P630X120-20L	TSOPx20 6.45x4.35mm Pitch 0.65mm		
R1	1	10k	RESC1608X05L	0603 SMT Resistor	Any suitable 1%	
R2	1	520r	RESC1608X05L	0603 SMT Resistor	Any suitable 1%	
R3	1	1.5k	RESC1608X05L	0603 SMT Resistor	Any suitable 1%	
R5, R6	2	120	RESC1608X05L	0603 SMT Resistor	Any suitable 1%	
R7	1	2K	RESC1608X05L	0603 SMT Resistor	Any suitable 1%	
ROTARY ENCODER	1		PEC12R-4XXXF-SXXXX_1	Rotary encoder	Any suitable	
USB	1		USB MICRO B JLCPCB	USB Micro B Receptacle		C397452

Design Rules Verification ReporFilename : U:\dev\hid_kbd\pcb\volume_knob\volume_knob.PcbDoc

Warnings 0 Rule Violations 0

Warnings Total

Rule Violations	
Clearance Constraint (Gap=0.127mm) (All),(All)	0
Clearance Constraint (Gap=0.127mm) (InNet('DP')),(InNet('DM')	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.127mm) (Max=1.016mm) (Preferred=0.127mm) (All	0
Routing Layers(All)	0
Routing Via (Templates Used To Check Via: via_gnd_stitch, via_power, via_signal_routing) (All	0
Differential Pairs Uncoupled Length using the Gap Constraints (Min=0.254mm) (Max=0.254mm) (Prefered=0.254mm)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm	0
Minimum Annular Ring (Minimum=0.13mm) (All,	0
Hole Size Constraint (Min=0.025mm) (Max=3.5mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All), (All)	0
Minimum Solder Mask Sliver (Gap=0.115mm) (All), (All)	0
Silk To Solder Mask (Clearance=0.254mm) (Disabled)(IsPad),(All	0
Silk to Silk (Clearance=0.254mm) (Disabled)(All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Component Clearance Constraint (Horizontal Gap = 0.254mm, Vertical Gap = 0.254mm) (All),(All)	0
Height Constraint (Min=0mm) (Max=1000mm) (Prefered=12.7mm) (All	0
Total	0

Electrical Rules Check Report

Class	Document	Message
		Successful Compile for