







| Designator     | Quantity | Value | Description    | Model:Footprint        | Line # |
|----------------|----------|-------|----------------|------------------------|--------|
| U1             | 1        |       | CH554E         | MSOP10 3x3 x 0.5       |        |
| DBG            | 1        |       | Debug header   | 4 way debug header     |        |
| F1             | 1        | 500mA | FUSE           | FUSE 0603              |        |
| D4             | 1        | 20mA  | LED            | SMT LED 0603           |        |
| C1             | 1        | 1uF   | MLCC           | MLCC 0603              |        |
| C2             | 1        | 2.2uF | MLCC           | MLCC 0603              |        |
| R4             | 1        | 10k   | Resistor       | 0603 SMT Resistor      |        |
| R5             | 1        | 1k    | Resistor       | 0603 SMT Resistor      |        |
| ROTARY_ENCODER | 1        |       | Rotary Encoder | Rotary encoder         |        |
| D1, D2, D3     | 3        |       | TVS Diode      | SODFL 98x40 2 pin      |        |
| J1             | 1        |       | USB Receptacle | USB Micro B Receptacle |        |

## Design Rules Verification Report

Filename : U:\dev\hid\_kbd\pcb\wch554e\wch554e\wch554e.PcbDoc

Warnings 0  
Rule Violations 0

| Warnings |   |
|----------|---|
| Total    | 0 |

| Rule Violations   |   |
|---|---|
| Clearance Constraint (Gap=6mil) (All),(All)   | 0 |
| Short-Circuit Constraint (Allowed=No) (All),(All)   | 0 |
| Un-Routed Net Constraint ( All )  | 0 |
| Modified Polygon (Allow modified: No), (Allow shelved: No)  | 0 |
| Width Constraint (Min=5mil) (Max=100mil) (Preferred=10mil) (All)  | 0 |
| Routing Via (Templates Used To Check Via: GND_VIA, routing_via) (All)   | 0 |
| Power Plane Connect Rule(Relief Connect )(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4 | 0 |
| Hole Size Constraint (Min=15.748mil) (Max=137.795mil) (All)   | 0 |
| Hole To Hole Clearance (Gap=10mil) (All),(All)  | 0 |
| Minimum Solder Mask Sliver (Gap=3.937mil) (All),(All)   | 0 |
| Net Antennae (Tolerance=0mil) (All)   | 0 |
| Board Clearance Constraint (Gap=0mil) (All)   | 0 |
| Component Clearance Constraint ( Horizontal Gap = 6mil, Vertical Gap = 10mil ) (All),(All)                    | 0 |
| Total   | 0 |