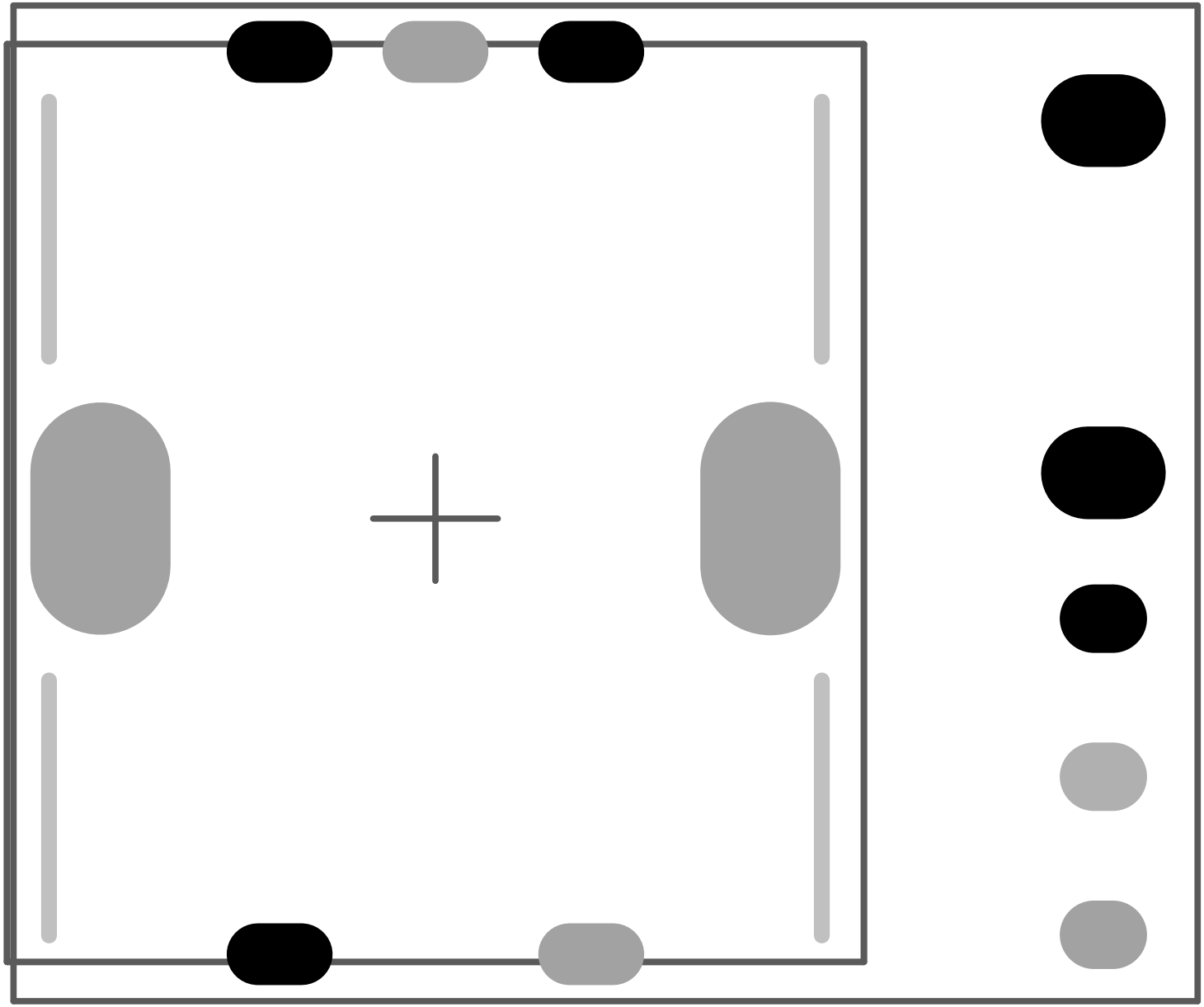
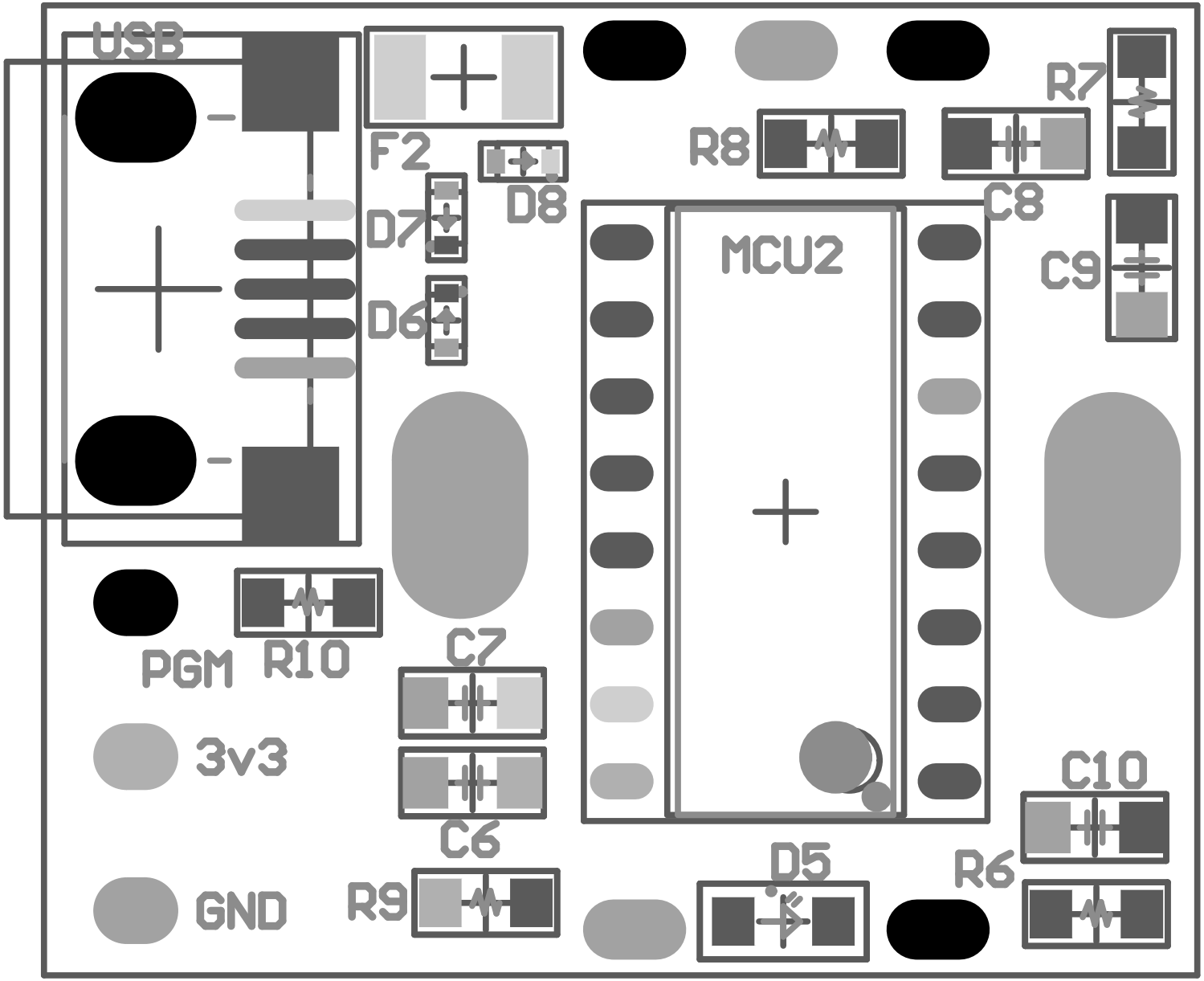



USB
F2
D8
D7
D6
R8
R7
C8
C9
MCU2
PGM
R10
C7
3v3
C6
R9
GND
D5
C10
R6

Footprint	Quantity	Designator	Description	Value	JLCPCB Part #
MLCC 0603	2	C6, C7	MLCC	1uF	C105524
MLCC 0603	3	C8, C9, C10	MLCC	6.8nF	C1631
SMT LED 0603	1	D5	LED	20mA	C138545
SODFL 98x40 2 pin	3	D6, D7, D8	TVS Diode	TVS_DIODE	C384848
FUSE_0805	1	F2	FUSE	1A	C70061
SOP16 x1.27	1	MCU2	CH554G SOP16 MCU	CH554G	C114295
0603 SMT Resistor	3	R6, R7, R8	Resistor	68r	C27592
0603 SMT Resistor	1	R9	Resistor	680r	C23228
0603 SMT Resistor	1	R10	Resistor	10k	C22765
USB Micro B Receptacle	1	USB	USB Receptacle	USB Micro	C397452

Design Rules Verification Report

Filename : U:\dev\hid_kbd\pcb\wch554g\wch554g.PcbDoc

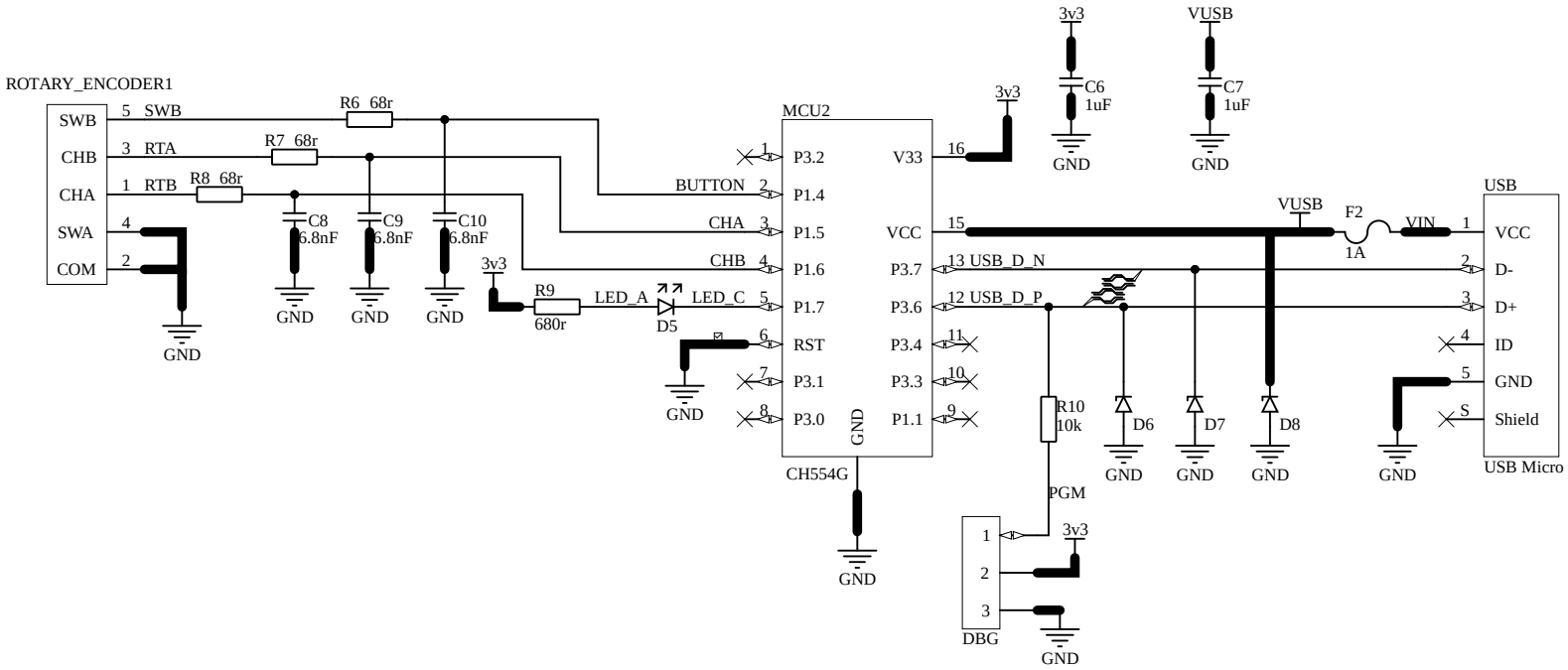
Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.152mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.102mm) (Max=0.762mm) (Preferred=0.127mm) (All	0
Routing Layers(All)	0
Routing Via (Templates Used To Check Via: GND_VIA) (All)	0
Differential Pairs Uncoupled Length using the Gap Constraints (Min=0.102mm) (Max=0.254mm) (Prefered=0.254mm)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm	0
Hole Size Constraint (Min=0.3mm) (Max=10mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.102mm) (All),(All)	0
Silk To Solder Mask (Clearance=0.254mm) (False),(False)	0
Silk to Silk (Clearance=0mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) (All)	0
Component Clearance Constraint (Horizontal Gap = 0mm, Vertical Gap = 0.254mm) (All),(All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All	0
Total	0

Electrical Rules Check Report

Class	Document	Message
		Successful Compile for



USB Knob CH552G	Revision 1 Saved on 14/06/2022
skilbeck.com	Sheet 1 of 1