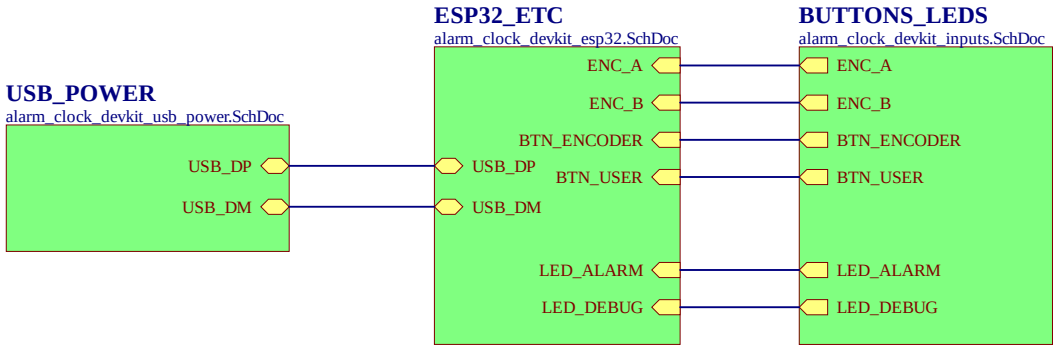
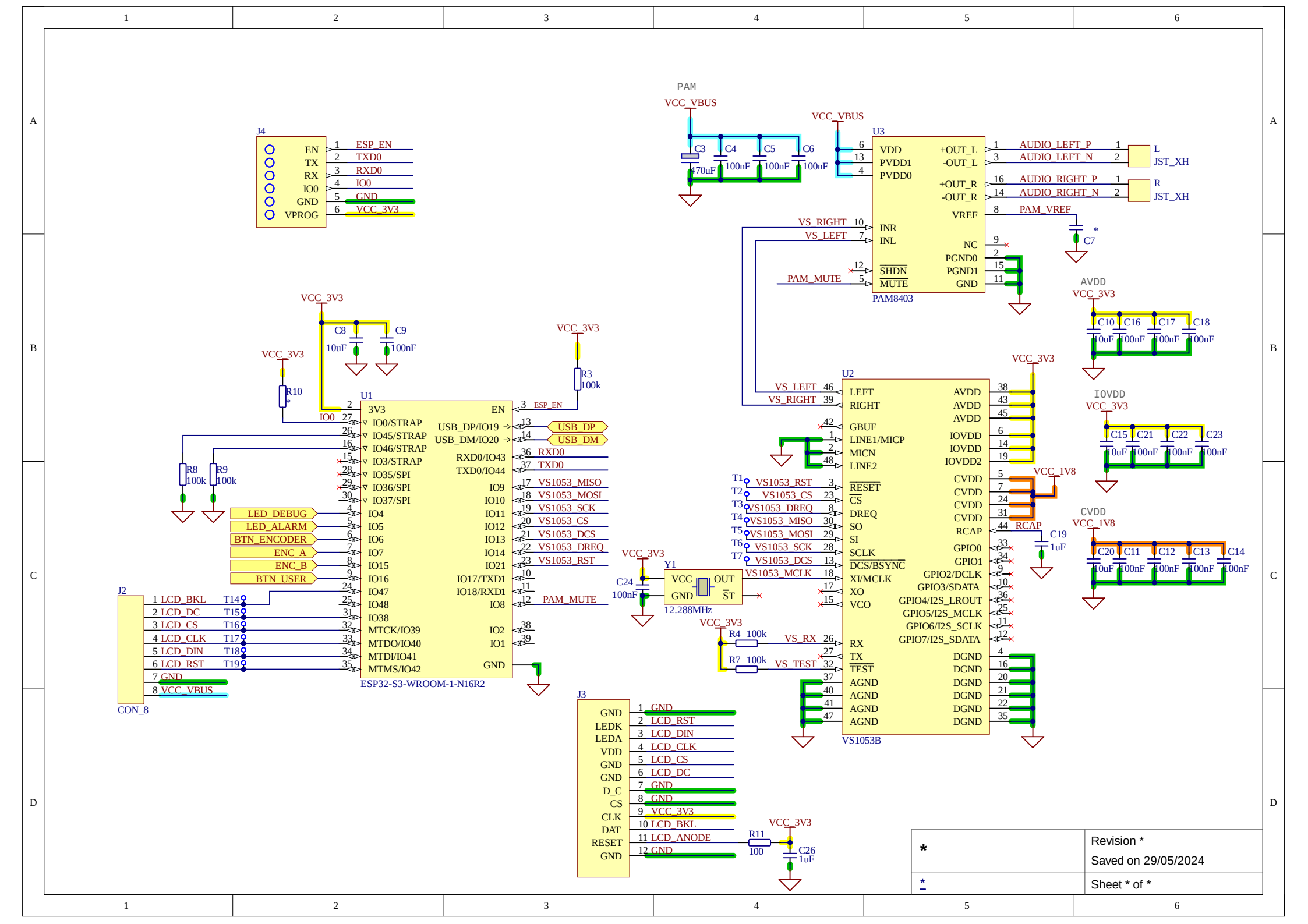


Wifi Alarm Clock	Revision 1 Saved on 27/05/2024
skilbeck.com	Sheet 1 of 1


PAM
J4
EN
TX
RX
IO0
GND
VPROG
ESP_EN
TXD0
RXD0
IO0
GND
VCC_3V3
VCC_VBUS
C3
C4
C5
C6
470uF
100nF
100nF
100nF
U3
VDD
PVDD1
PVDD0
+OUT_L
-OUT_L
+OUT_R
-OUT_R
VREF
NC
PGND0
PGND1
GND
INR
INL
SHDN
MUTE
PAM8403
AUDIO_LEFT_P
AUDIO_LEFT_N
AUDIO_RIGHT_P
AUDIO_RIGHT_N
L
R
JST_XH
PAM_VREF
C7
VS_RIGHT
VS_LEFT
PAM_MUTE
AVDD
C10
C16
C17
C18
10uF
100nF
U1
3V3
IO0/STRAP
IO45/STRAP
IO46/STRAP
IO3/STRAP
IO35/SPI
IO36/SPI
IO37/SPI
IO4
IO5
IO6
IO7
IO15
IO16
IO47
IO48
IO38
MTCK/IO39
MTDO/IO40
MTDI/IO41
MTMS/IO42
EN
USB_DP/IO19
USB_DM/IO20
RXD0/IO43
TXD0/IO44
IO9
IO10
IO11
IO12
IO13
IO14
IO21
IO17/TXD1
IO18/RXD1
IO8
IO2
IO1
GND
ESP32-S3-WROOM-1-N16R2
R3
100k
R10
R8
R9
LED_DEBUG
LED_ALARM
BTN_ENCODER
ENC_A
ENC_B
BTN_USER
USB_DP
USB_DM
VS1053_MISO
VS1053_MOSI
VS1053_SCK
VS1053_CS
VS1053_DCS
VS1053_DREQ
VS1053_RST
U2
LEFT
RIGHT
GBUF
LINE1/MICP
MICN
LINE2
RESET
CS
DREQ
SO
SI
SCLK
DCS/BSYNC
XI/MCLK
XO
VCO
RX
TX
TEST
AGND
IOVDD
IOVDD2
CVDD
RCAP
GPIO0
GPIO1
GPIO2/DCLK
GPIO3/SDATA
GPIO4/I2S_LROUT
GPIO5/I2S_MCLK
GPIO6/I2S_SCLK
GPIO7/I2S_SDATA
DGND
VS1053B
IOVDD
C15
C21
C22
C23
CVDD
VCC_1V8
C19
1uF
C20
C11
C12
C13
C14
J2
LCD_BKL
LCD_DC
LCD_CS
LCD_CLK
LCD_DIN
LCD_RST
CON_8
Y1
12.288MHz
C24
100nF
R4
R7
VS_RX
VS_TEST
J3
LEDK
LEDA
VDD
D_C
CS
CLK
DAT
RESET
LCD_ANODE
R11
100
C26
1uF
*
Revision *
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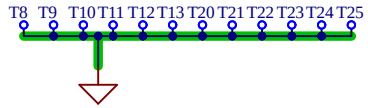
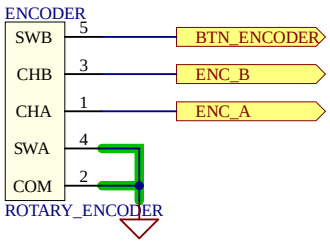
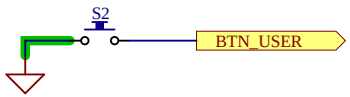
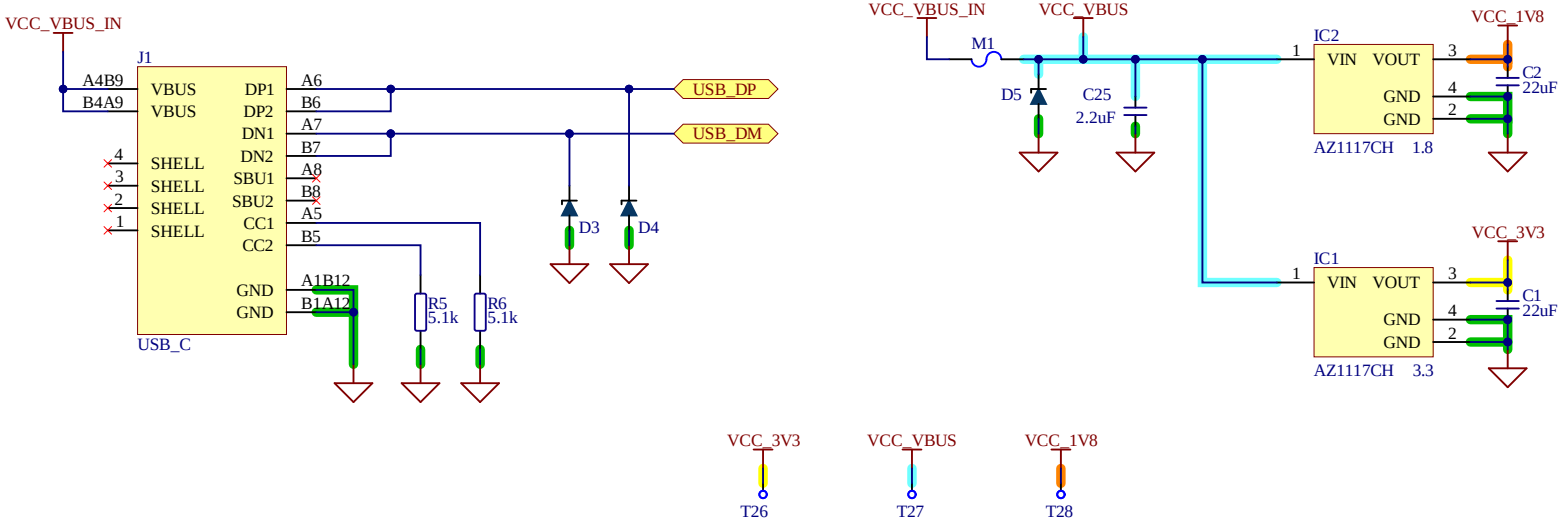
Sheet * of *







*	Revision * Saved on 29/05/2024
*	Sheet * of *



*	Revision *
	Saved on 29/05/2024
*	Sheet * of *

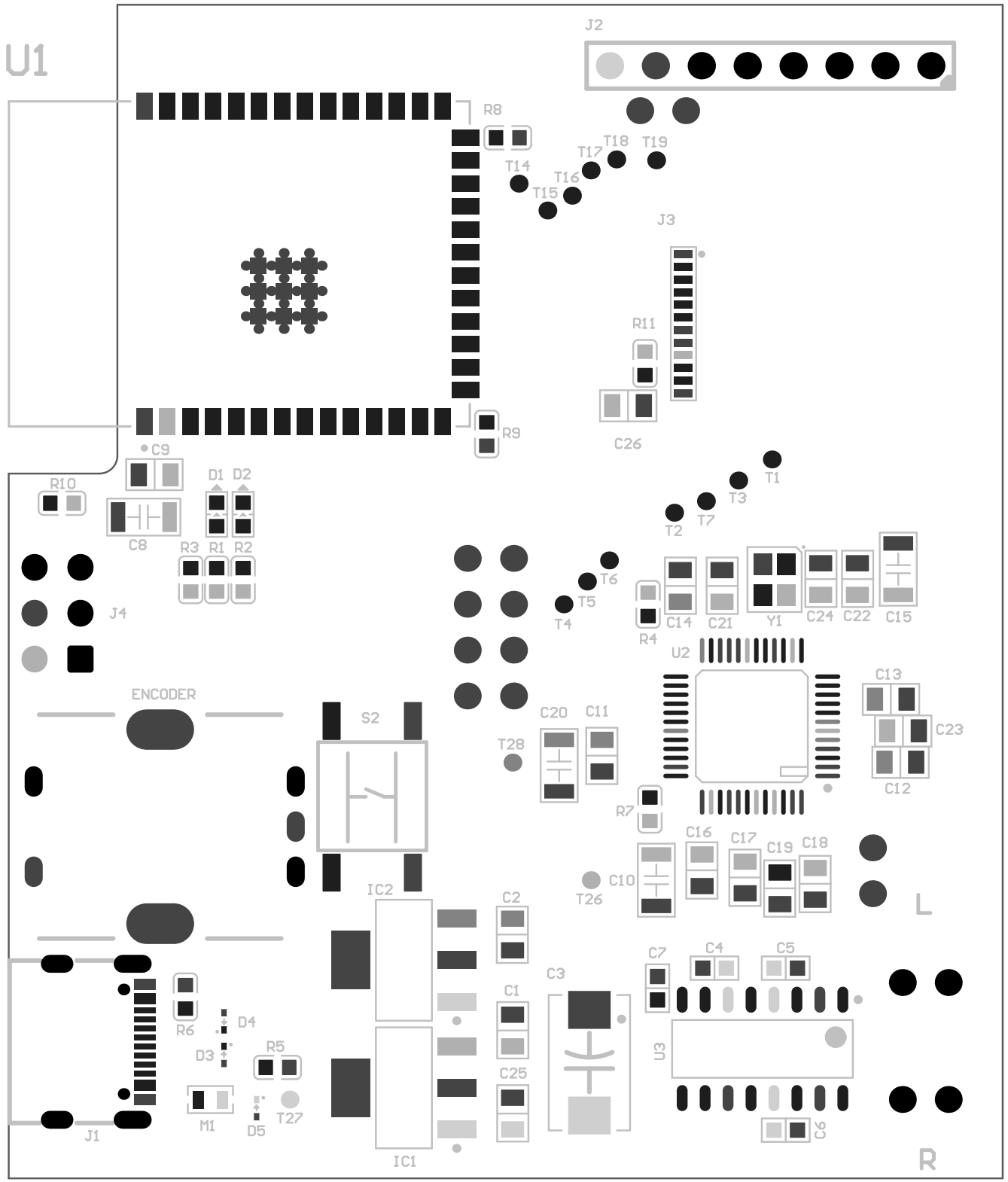
Design Rules Verification Report

Filename : E:\dev\wifi_alarm_clock\pcbs\devkit\alarm_clock_devkit\alarm_clock_devkit.PC

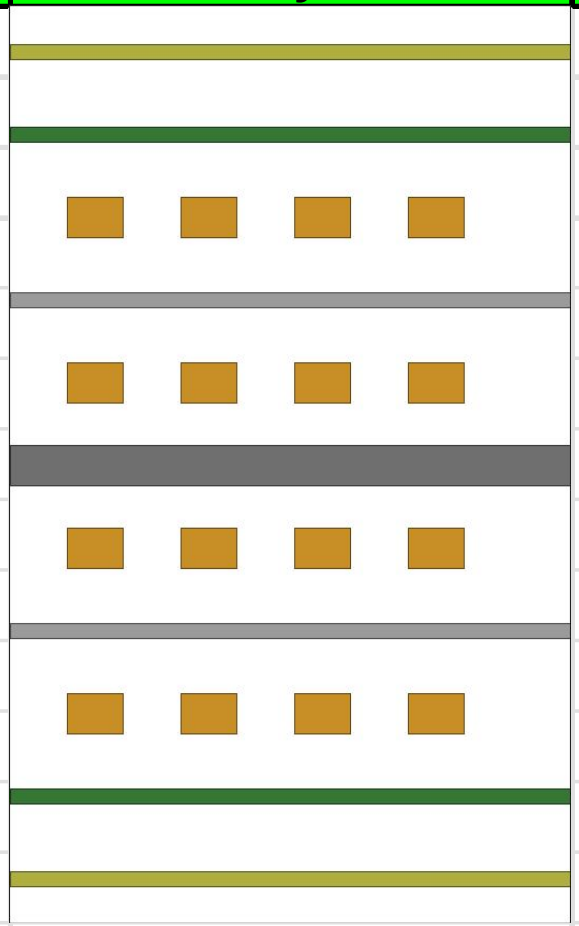
Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.508mm) (InNetClass('POWER24') And ((IsPad And (InNet('GND') Or InNet('VCC_LED'))	0
Clearance Constraint (Gap=-0.1mm) (InPadClass('AGND_TIE')),(InNet('GND') And OnBottomLaye	0
Clearance Constraint (Gap=0.127mm) (All),(All)	0
Clearance Constraint (Gap=0.2mm) (All),(IsKeepOut)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Short-Circuit Constraint (Allowed=Yes) (InPadClass('AGND_TIE')),(InNet('GND')	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.127mm) (Max=1.27mm) (Preferred=0.127mm) (All	0
Routing Layers(All)	0
Routing Via (Templates Used To Check Via: GND_VIA, POWER_VIA) (All	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.127mm) (Air Gap=0.127mm	0
Minimum Annular Ring (Minimum=0.13mm) (IsPad)	0
Minimum Annular Ring (Minimum=0.13mm) (IsVia)	0
Acute Angle Constraint [Tracks Only] (Minimum=45.000) (All)	0
Hole Size Constraint (Min=0.3mm) (Max=3mm) (All)	0
Hole To Hole Clearance (Gap=0.2mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.1mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) (InLayerClass('Electrical Layers')	0
Component Clearance Constraint (Horizontal Gap = 0.1mm, Vertical Gap = Infinite) (All),(All)	0
Component Clearance Constraint (Horizontal Gap = 0mm, Vertical Gap = 0mm) (All),(InComponentClass('TestPoint')	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All	0
Total	0


U1
J2
R8
T14
T15
T16
T17
T18
T19
J3
R11
C26
R9
C9
R10
C8
D1
D2
R3
R1
R2
J4
T1
T2
T3
T4
T5
T6
T7
R4
C14
C21
Y1
C24
C22
C15
U2
C13
C23
C12
ENCODER
S2
C20
C11
T28
R7
C16
C17
C19
C18
C10
T26
L
IC2
C2
C1
C3
C25
C7
C4
C5
U3
C6
R6
D4
D3
R5
M1
D5
T27
J1
IC1
R

Board Stack Report

Stack Up		Layer Stack			
Layer	Board Layer Stack	Name	Material	Thickness	Constant
1		Top Paste			
2		Top Overlay			
3		Top Solder	SM-001	0.025mm	4
4		Top Layer	Copper	0.035mm	
5		Dielectric 2	PP-006	0.210mm	4.1
6		Layer 1	Copper	0.015mm	
7		Dielectric 1	Core-043	1.065mm	4.3
8		Layer 2	Copper	0.015mm	
9		Dielectric 3	PP-006	0.210mm	4.1
10		Bottom Layer	Copper	0.035mm	
11		Bottom Solder	SM-001	0.025mm	4
12		Bottom Overlay			
13		Bottom Paste			
	Height : 1.637mm				