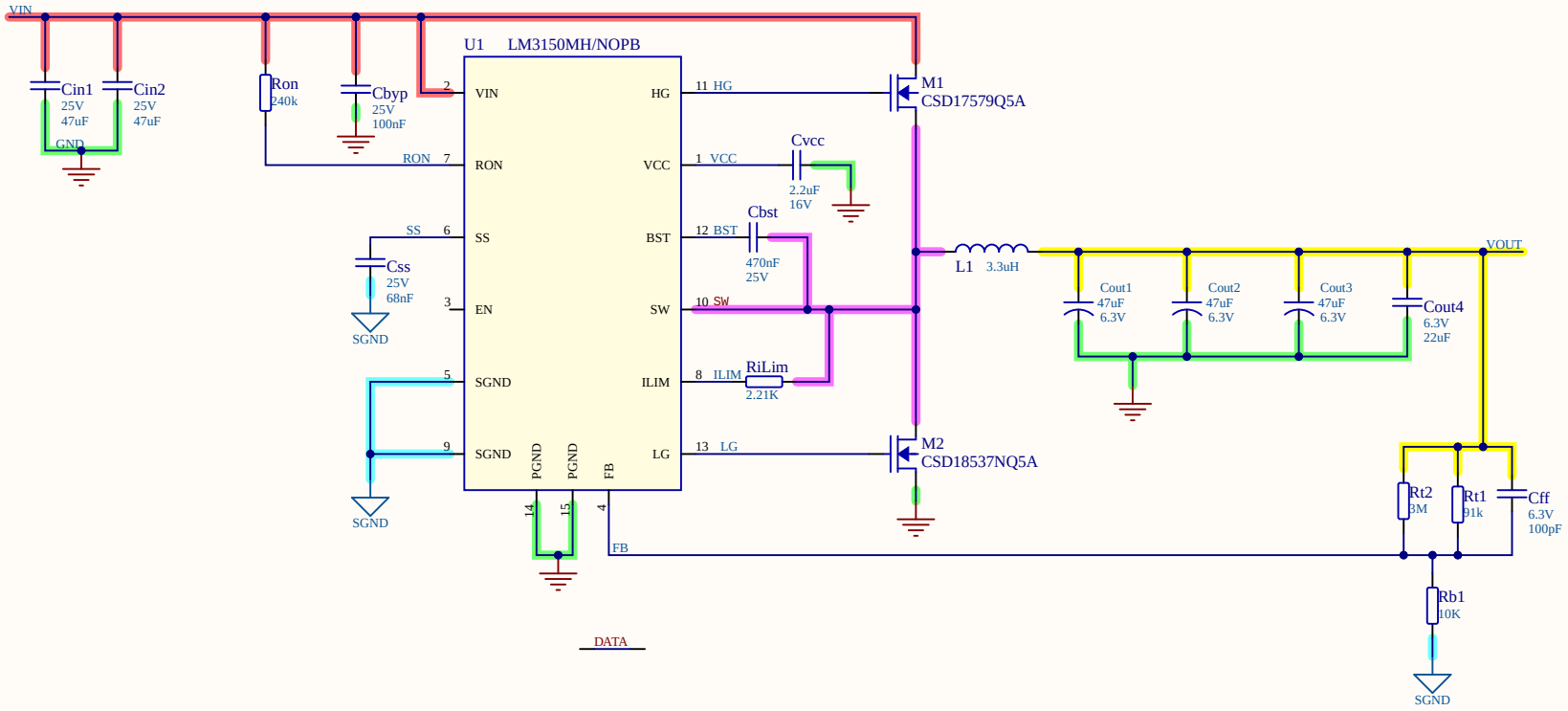

Title		
Size: A4	Number	Revision
Date: 6/22/2020		Sheet of
File: C:\Dev\..\buck4.schdoc		Drawn By:

Index	Designator	Quantity	Value	Voltage	VdsMax	Name	Description	Footprint	MPN	Vendor
1	Cbst	1	470nF	25V		MLCC	Multilayer Ceramic Capacitor	CAPC2012X12L		
2	Cbyp	1	100nF	25V		MLCC	Multilayer Ceramic Capacitor	CAPC2012X12L		
3	Cff	1	100pF	6.3V		MLCC	Multilayer Ceramic Capacitor	CAPC1608X08L		
4, 5	Cin1, Cin2	2	47uF	25V		MLCC	Multilayer Ceramic Capacitor	CAPC3225X25L	C3216X5R1E476M160AC	TDK
6, 7, 8	Cout1, Cout2, Cout3	3	47uF	6.3V		CAPACITOR	Electrolytic Capacitor	CAPMP7343X11L	EEFCS1A470R	Pansonic
9	Cout4	1	22uF	6.3V		MLCC	Multilayer Ceramic Capacitor	CAPC3216X12L		
10	Css	1	68nF	25V		MLCC	Multilayer Ceramic Capacitor	CAPC1608X08L		
11	Cvcc	1	2.2uF	16V		MLCC	Multilayer Ceramic Capacitor	CAPC2012X12L		
12	L1	1	3.3uH			744313330	Inductor	WE-HCI_1335	744313330	Wurth Elektronik
13	M1	1			30.0V	CSD17579Q5A	N Channel MOSFET	TRANS_NexFET_Q5A	CSD17579Q5A	Texas Instruments
14	M2	1			60.0	CSD18537NQ5A	N Channel MOSFET	TRANS_NexFET_Q5A	CSD18537NQ5A	Texas Instruments
15	Rb1	1	10K			RES0603	Chip Resistor	RESC1608X03L		
16	RiLim	1	2.21K			RES0603	Chip Resistor	RESC1608X03L		
17	Ron	1	240k			RES0603	Chip Resistor	RESC1608X03L		
18	Rt1	1	91k			RES0603	Chip Resistor	RESC1608X03L		
19	Rt2	1	3M			RES0603	Chip Resistor	RESC1608X03L		
20	U1	1				LM3150MH/NOPB	Buck controller	MXA14A	LM3150MH/NOPB	Texas Instruments

Design Rules Verification Report

Filename : C:\Dev\wifi-christmas-tree-lights\pcbs\buck4\buck4.PcbDoc

Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.127mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Short-Circuit Constraint (Allowed=Yes) (InNet('GND')),(InNet('SGND'))	0
Un-Routed Net Constraint ((All))	0
Width Constraint (Min=0.127mm) (Max=2.54mm) (Preferred=0.127mm) (All)	0
Routing Via (Templates Used To Check Via: connector, gnd_stitch, signal_routing, v65h40m0mx0) (All)	0
Power Plane Connect Rule(Direct Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Hole Size Constraint (Min=0.025mm) (Max=4mm) (All)	0
Pads and Vias to follow the Drill pairs settings	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.2mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) (Not (OnLayer('Top Overlay') Or OnLayer('Bottom Overlay')))	0
Component Clearance Constraint (Horizontal Gap = 0.05mm, Vertical Gap = Infinite) (All),(All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	0