







Designator	Quantity	Value	Name	Description	Footprint	Model:Footprint	LibRef
C1		1 1uF	Сар	Capacitor	108L	Chip Capacitor 0603	Сар
C2, C33		2 100nF	Сар	Capacitor	CAPC_0603_1608X 08L	Chip Capacitor 0603	Сар
C37, C38, C39, C40, C41		5 22uF	Сар	Capacitor	CAPC3224X25L	Chip Capacitor, 2-Leads, Body 3.20x2.45mm, IPC High Density	Сар
C42		1 100pF	Сар	Capacitor	CAPC_0603_1608X 08L	Chip Capacitor 0603	Сар
D1		1	Schottky 40V 3A	Schottky Diode	SODFL470X110-2L	SODFL, 2-Leads, Body 2.50x4.70mm, IPC High Density	D Schottky
ESP1		1	ESP8266 ESP-12-E	ESP8266 ESP-12-E	ESP8266 ESP-12-E	ESP8266 ESP-12-E	ESP8266 ESP-12-E
L2		1 15uH	Inductor	Inductor	INDP5150X20L	Precision Wire Wound Inductor, 2-Leads, Body 5.15x5.00mm, IPC High Density	Inductor
LED1		1	RGB LED Common anode	Dot is _not_ anode!	PLCC-4	LED	RGB_LED
Q1, Q2, Q3		3	MOSFET-P		DPAK229P994X24 1-3L	D-PAK, 3-Pads, Body 6.21x6.73mm (max), IPC High Density	MOSFET-P
Q4		1	MOSFET-N		SOT23	SOT23, 3-Leads, Body 2.90x2.45mm, Pitch 0.95mm, IPC High Density	MOSFET-N
R1, R2, R3, R4, R5, R14, R23		7 10K	Res2	Resistor		Chip Resistor, 2-Leads, Body 1.60x0.80mm, IPC High Density	Res2
R6, R7, R8, R13, R31		5 1K	Res2	Resistor	RESC_0603_1608X 08L	Chip Resistor, 2-Leads, Body 1.60x0.80mm, IPC High Density	Res2
R11		1 220K	Res2	Resistor	RESC_0603_1608X 08L	Chip Resistor, 2-Leads, Body 1.60x0.80mm, IPC High Density	Res2
R12		1 100K	Res2	Resistor	RESC_0603_1608X 08L	Chip Resistor, 2-Leads, Body 1.60x0.80mm, IPC High Density	Res2
R29		1 2.4K	Res2	Resistor	RESC_0603_1608X 08L	Chip Resistor, 2-Leads, Body 1.60x0.80mm, IPC High Density	Res2
R30		1 680	Res2	Resistor	RESC_0603_1608X 08L	Chip Resistor, 2-Leads, Body 1.60x0.80mm, IPC High Density	Res2
S_FUN1		1	4-1437565-1	Tactile switch	EVQP7C01P	Side actuated tactile switch	4-1437565-1
U1		1	M74VHC1GT125	Level shifter non inverting	SOT65P210X100- 5L	SOT23, 5-Leads, Body 2.00x2.10mm, Pitch 0.65mm, IPC High Density	M74VHC1GT125
U2		1	LDO 5V	J	Micro8 TSOP	TSOP, 8-Leads	LDO LP2950 5V
U3		1	BD9G101G-LB		TSOP95P280X125- 6L	TSOP, 6-Leads, Body 2.90x1.65mm, Pitch 0.95mm, IPC High Density	BD9G102G-LB

**Design Rules Verification Report**Filename: C:\Dev\wifi-christmas-tree-lights\pcbs\controller\_8266\controller\_8266.PcbDoc

Warnings 0 Rule Violations 0

	Warnings	
I	Total	0

Clearance Constraint (Gap=5mil) (All), (IsKeepOut)  Clearance Constraint (Gap=20mil) (InNetClass('POWER24') And ((IsPad And (InNet('GND') Or InNet('VCC_LED'))) Or Occessor Constraint (Gap=5mil) (All), (All)  Clearance Constraint (Gap=5mil) (All), (All)  Clearance Constraint (Gap=5mil) (InNet('PS_GATE') And (Not WithinRoom('LowPowerRoom'))), (InNet('VCC24'))  Clearance Constraint (Gap=20mil) (InNet('PS_GATE') And (Not WithinRoom('LowPowerRoom'))), (InNet('VCC24'))  Short-Circuit Constraint (Allowed=Yes) (InPadClass('AGND_TIE')), (InNet('GND'))  Short-Circuit Constraint (Allowed=No) (All), (All)  O Short-Circuit Constraint (Allowed=No) (All), (All)  O Jn-Routed Net Constraint (Allowed=No), (Allow shelved: No)  Modified Polygon (Allow modified: No), (Allow shelved: No)  Modified Polygon (Allow sh		
Clearance Constraint (Gap=20mil) (InNetClass('POWER24') And ((IsPad And (InNet('GND') Or InNet('VCC_LED'))) Or 0 Clearance Constraint (Gap=5mil) (All), (All) 0 Clearance Constraint (Gap=3.937mil) (InPadClass('AGND_TIE')), (InNet('GND') And OnBottomLayer) 0 Clearance Constraint (Gap=20mil) (InNet('PS_GATE') And (Not WithinRoom('LowPowerRoom'))), (InNet('VCC24')) 0 Short-Circuit Constraint (Allowed=Yes) (InPadClass('AGND_TIE')), (InNet('GND')) 0 Short-Circuit Constraint (Allowed=Yes) (InPadClass('AGND_TIE')), (InNet('GND')) 0 Jn-Routed Net Constraint (Allowed=No) (All), (All) 0 Jn-Routed Net Constraint (Allowed=No) (All), (All) 0 Middlied Polygon (Allow modified: No), (Allow shelved: No) 0 Midtlied Polygon (Allow modified: No), (Allow shelved: No) 0 Midtlied Polygon (Allow modified: No), (Allow shelved: No) 0 Midtlin Constraint (Min=5mil) (Max=50mil) (Preferred=5mil) (All) 0 Power Plane Connect Rule(Relief Connect )(Expansion=20mil) (Conductor Width=5mil) (Air Gap=5mil) (Entries=4) (All') 0 Minimum Annular Ring (Minimum=5.118mil) (IsPad) 0 Minimum Annular Ring (Minimum=5.118mil) (IsPad) 0 Minimum Annular Ring (Minimum=5.118mil) (IsVia) 0 Acute Angle Constraint (Tracks Only] (Minimum=45.000) (All) 0 Hole Size Constraint (Min=11.811mil) (Max=248.031mil) (All) 0 Hole To Hole Clearance (Gap=7.874mil) (All), (All) 0 Minimum Solder Mask Sliver (Gap=7.874mil) (All), (All) 0 Modified Mask Sliver (Gap=0mil) (InLayerClass('Electrical Layers')) 0 Modified Clearance Constraint (Gap=0mil) (InLayerClass('Electrical Layers')) 0 DowPowerRoom (Bounding Region = 39504.59mil, 40260.392mil, 40172.144mil, 40418.41mil) 0 Component Clearance Constraint (Horizontal Gap = 0mil, Vertical Gap = 0mil) (All), (InComponentClass('TestPoint')) 0 Component Clearance Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	Rule Violations	
Clearance Constraint (Gap=5mil) (All), (All) Clearance Constraint (Gap=3.937mil) (InPadClass('AGND_TIE')), (InNet('GND') And OnBottomLayer)  Clearance Constraint (Gap=20mil) (InNet('PS_GATE') And (Not WithinRoom('LowPowerRoom'))), (InNet('VCC24'))  Short-Circuit Constraint (Allowed=Yes) (InPadClass('AGND_TIE')), (InNet('GND'))  Short-Circuit Constraint (Allowed=No) (All), (All)  O  Jn-Routed Net Constraint (Allowed=No) (All), (All)  O  Width Constraint (Min=5mil) (Max=50mil) (Preferred=5mil) (All)  O  Width Constraint (Min=5mil) (Max=50mil) (Preferred=5mil) (All)  O  Wouth Constraint (Min=5mil) (Max=50mil) (Preferred=5mil) (All)  O  Wouthing Via (Templates Used To Check Via: gnd_stitch, power_via, signal_routing) (All)  Power Plane Connect Rule(Relief Connect) (Expansion=20mil) (Conductor Width=5mil) (Air Gap=5mil) (Entries=4) (All)  Winimum Annular Ring (Minimum=5.118mil) (IsPad)  Winimum Annular Ring (Minimum=5.118mil) (IsPad)  O  Winimum Annular Ring (Minimum=5.118mil) (IsVia)  O  Acute Angle Constraint (Min=11.811mil) (Max=248.031mil) (All)  O  Hole To Hole Clearance (Gap=7.874mil) (All), (All)  O  Net Antennae (Tolerance=0mil) (All)  O  Net Antennae (Tolerance=0mil) (All)  O  O  WordowerNoom (Bounding Region = (39504.59mil, 40260.392mil, 40172.144mil, 40418.41mil)  Component Clearance C constraint (Horizontal Gap = 0mil, Vertical Gap = 0mil) (All), (InComponentClass(TestPoint'))  O  Component Clearance C Constraint (Horizontal Gap = 0mil, Vertical Gap = Infinite) (All), (All)		0
Clearance Constraint (Gap=-3.937mil) (InPadClass('AGND_TIE')), (InNet('GND') And OnBottomLayer)  Clearance Constraint (Gap=20mil) (InNet('PS_GATE') And (Not WithinRoom('LowPowerRoom'))), (InNet('VCC24'))  Short-Circuit Constraint (Allowed=Yes) (InPadClass('AGND_TIE')), (InNet('GND'))  Short-Circuit Constraint (Allowed=No) (All), (All)  Jn-Routed Net Constraint (Allowed=No) (All), (All)  Modified Polygon (Allow modified: No), (Allow shelved: No)  Midth Constraint (Min=5mil) (Max=50mil) (Prefered=5mil) (All)  OROuting Via (Templates Used To Check Via: gnd_stitch, power_via, signal_routing) (All)  Power Plane Connect Rule(Relief Connect) (Expansion=20mil) (Conductor Width=5mil) (Air Gap=5mil) (Entries=4) (All')  Minimum Annular Ring (Minimum=5.118mil) (IsPad)  Minimum Annular Ring (Minimum=5.118mil) (IsPad)  Moditing Via (Templates Used To Check Via: gnd_stitch, power_via, signal_routing) (All)  Power Plane Connect Rule(Relief Connect) (Expansion=20mil) (Conductor Width=5mil) (Air Gap=5mil) (Entries=4) (All')  Minimum Annular Ring (Minimum=5.118mil) (IsPad)  Minimum Annular Ring (Minimum=5.118mil) (IsPad)  Moditing Via (Templates Used To Check Via: gnd_stitch, power_via, signal_routing) (All)  OROUTING All Ring (Minimum=5.118mil) (IsPad)  Minimum Annular Ring (Minimum=5.118mil) (IsPad)  Minimum Annular Ring (Minimum=5.118mil) (IsPad)  OROUTING All Ring (Minimum=5.118mil) (IsPad)  Minimum Solder Mask Silver (Gap=7.874mil) (All), (All)  OROUTING All Ring (Minimum=6.00mil) (InLayerClass('Electrical Layers'))  OROUTING All Ring (Minimum=6.00mil) (InLayerClass('Electrical Layers'))  OROUTING All Ring (Minimum=6.00mil) (InLayerClass('Electrical Layers'))  OROUTING Clearance Constraint (Horizontal Gap = 0mil, Vertical Gap = 0mil (All), (InComponentClass('TestPoint'))  OROUTING Clearance Constraint (Horizontal Gap = 0mil, Vertical Gap = Infinite) (All), (All)  Height Constraint (Min=0mil) (Max =1000mil) (Prefered=500mil) (All)		0
Clearance Constraint (Gap=20mil) (InNet("PS_GATE") And (Not WithinRoom("LowPowerRoom"))), (InNet("VCC24"))  Short-Circuit Constraint (Allowed=Yes) (InPadClass("AGND_TIE")), (InNet("GND"))  Short-Circuit Constraint (Allowed=No) (All), (All)  Jn-Routed Net Constraint (Allowed=No) (All), (All)  Modified Polygon (Allow modified: No), (Allow shelved: No)  Modified Polygon (Allow modified: No)  Modified Polygon (Allow modified: No), (Allow shelved: No)  Modified Polygon (Allow modified: No), (Allow shelved: No)  Modified Polygon (Allow modified: No), (Allow shelved: No)  Modified Polygon (Allow shelved: No)  Modified Polygon (Allow modified: No)  Modified Polygon (Allow shelved: No)  Modifie		0
Short-Circuit Constraint (Allowed=Yes) (inPadClass(AGND_TIE')),(inNet(GND'))  Short-Circuit Constraint (Allowed=No) (All),(All)  Un-Routed Net Constraint ((Alloy)  Modified Polygon (Allow modified: No), (Allow shelved: No)  Modified Polygon (Allow modified: No), (Allow State (Mallow State (Mallow)), (Allow State (Mallow)), (Allow State (Minimum=5.118mil) (Ispad)  Modified Polygon (Allow modified: No), (Allow State (Minimum=5.118mil) (Ispad)  Modified Polygon (Allow modified: No), (Allow State (Minimum=5.118mil) (Ispad)  Modified Polygon (Allow modified: No), (Allow State (Minimum=5.118mil) (Ispad)  Modified Polygon (Allow State (Minimum=6.118mil) (Ispad)  Modified Polygon (Minimum	Clearance Constraint (Gap=-3.937mil) (InPadClass('AGND_TIE')),(InNet('GND') And OnBottomLayer)	0
Short-Circuit Constraint (Allowed=No) (All), (All)  Jn-Routed Net Constraint ( (All) )  Modified Polygon (Allow modified: No), (Allow shelved: No)  Modified Polygon (Allow modified: No), (Allow shelved: No)  Moth Constraint (Min=5mil) (Max=50mil) (Preferred=5mil) (All)  Routing Via (Templates Used To Check Via: gnd_stitch, power_via, signal_routing) (All)  Power Plane Connect Rule(Relief Connect )(Expansion=20mil) (Conductor Width=5mil) (Air Gap=5mil) (Entries=4) (All)  Minimum Annular Ring (Minimum=5.118mil) (IsPad)  Minimum Annular Ring (Minimum=5.118mil) (IsVia)  Acute Angle Constraint [Tracks Only] (Minimum=45.000) (All)  Hole Size Constraint (Min=11.811mil) (Max=248.031mil) (All)  Hole To Hole Clearance (Gap=7.874mil) (All), (All)  Minimum Solder Mask Sliver (Gap=7.874mil) (All), (All)  Net Antennae (Tolerance=0mil) (All)  Board Clearance Constraint (Gap=0mil) (InLayerClass(Electrical Layers'))  LowPowerRoom (Bounding Region = (39504.59mil, 40260.392mil, 40172.144mil, 40418.41mil)  Component Clearance Constraint ( Horizontal Gap = 0mil, Vertical Gap = 0mil) (All), (All), (All)  Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All), (All)	Clearance Constraint (Gap=20mil) (InNet('PS_GATE') And (Not WithinRoom('LowPowerRoom'))), (InNet('VCC24'))	0
Un-Routed Net Constraint ((All))  Modified Polygon (Allow modified: No), (Allow shelved: No)  Midth Constraint (Min=5mil) (Max=50mil) (Preferred=5mil) (All)  Routing Via (Templates Used To Check Via: gnd_stitch, power_via, signal_routing) (All)  Power Plane Connect Rule(Relief Connect) (Expansion=20mil) (Conductor Width=5mil) (Air Gap=5mil) (Entries=4) (All)  Minimum Annular Ring (Minimum=5.118mil) (IsPad)  Minimum Annular Ring (Minimum=5.118mil) (IsVia)  Acute Angle Constraint [Tracks Only] (Minimum=45.000) (All)  Hole Size Constraint (Min=11.811mil) (Max=248.031mil) (All)  Hole Clearance (Gap=7.874mil) (All),(All)  Minimum Solder Mask Sliver (Gap=7.874mil) (All),(All)  Net Antennae (Tolerance=0mil) (All)  Soard Clearance Constraint (Gap=0mil) (InLayerClass('Electrical Layers'))  LowPowerRoom (Bounding Region = (39504.59mil, 40260.392mil, 40172.144mil, 40418.41mil)  Component Clearance Constraint (Horizontal Gap = 0mil, Vertical Gap = 0mil) (All),(InComponentClass('TestPoint'))  Component Clearance Constraint (Horizontal Gap = 0mil, Vertical Gap = 1nfinite) (All),(All)  Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	Short-Circuit Constraint (Allowed=Yes) (InPadClass('AGND_TIE')),(InNet('GND'))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)  Midth Constraint (Min=5mil) (Max=50mil) (Preferred=5mil) (All)  Routing Via (Templates U sed To Check Via: gnd_stitch, power_via, signal_routing) (All)  Power Plane Connect Rule(Relief Connect) (Expansion=20mil) (Conductor Width=5mil) (Air Gap=5mil) (Entries=4) (All)  Minimum Annular Ring (Minimum=5.118mil) (IsPad)  Minimum Annular Ring (Minimum=5.118mil) (IsVia)  Acute Angle Constraint [Tracks Only] (Minimum=45.000) (All)  Hole Size Constraint (Min=11.811mil) (Max=248.031mil) (All)  Hole Clearance (Gap=7.874mil) (All),(All)  Minimum Solder Mask Sliver (Gap=7.874mil) (All),(All)  Wet Antennae (Tolerance=0mil) (All)  One of Clearance Constraint (Gap=0mil) (InLayerClass('Electrical Layers'))  One of Clearance Constraint (Horizontal Gap=0mil, Vertical Gap=0mil) (All),(All)  Component Clearance Constraint (Horizontal Gap=0mil, Vertical Gap=0mil) (All),(All)  Component Clearance Constraint (Horizontal Gap=0mil, Vertical Gap=1nfinite) (All),(All)  Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	Short-Circuit Constraint (Allowed=No) (All),(All)	0
Midth Constraint (Min=5mil) (Max=50mil) (Preferred=5mil) (All)  Routing Via (Templates Used To Check Via: gnd_stitch, power_via, signal_routing) (All)  Power Plane Connect Rule(Relief Connect) (Expansion=20mil) (Conductor Width=5mil) (Air Gap=5mil) (Entries=4) (All)  Minimum Annular Ring (Minimum=5.118mil) (IsPad)  Minimum Annular Ring (Minimum=5.118mil) (IsVai)  Acute Angle Constraint [Tracks Only] (Minimum=45.000) (All)  Hole Size Constraint (Min=11.811mil) (Max=248.031mil) (All)  Hole To Hole Clearance (Gap=7.874mil) (All), (All)  Minimum Solder Mask Sliver (Gap=7.874mil) (All), (All)  Net Antennae (Tolerance=0mil) (All)  Board Clearance Constraint (Gap=0mil) (InLayerClass('Electrical Layers'))  LowPowerRoom (Bounding Region = (39504.59mil, 40260.392mil, 40172.144mil, 40418.41mil)  Component Clearance Constraint ( Horizontal Gap = 0mil, Vertical Gap = 0mil) (All), (All)  Component Clearance Constraint ( Horizontal Gap = 0mil, Vertical Gap = Infinite ) (All), (All)  Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	Un-Routed Net Constraint ( (All) )	0
Routing Via (Templates Used To Check Via: gnd_stitch, power_via, signal_routing) (AII)  Power Plane Connect Rule(Relief Connect) (Expansion=20mil) (Conductor Width=5mil) (Air Gap=5mil) (Entries=4) (AII)  Minimum Annular Ring (Minimum=5.118mil) (IsPad)  Minimum Annular Ring (Minimum=5.118mil) (IsVia)  Acute Angle Constraint [Tracks Only] (Minimum=45.000) (AII)  Hole Size Constraint (Min=11.811mil) (Max=248.031mil) (AII)  Hole To Hole Clearance (Gap=7.874mil) (AII), (AII)  Minimum Solder Mask Sliver (Gap=7.874mil) (AII), (AII)  Net Antennae (Tolerance=0mil) (AII)  Board Clearance Constraint (Gap=0mil) (InLayerClass('Electrical Layers'))  LowPowerRoom (Bounding Region = (39504.59mil, 40260.392mil, 40172.144mil, 40418.41mil)  Component Clearance Constraint ( Horizontal Gap = 0mil, Vertical Gap = 0mil ) (AII), (AII)  Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (AII)	Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Power Plane Connect Rule(Relief Connect )(Expansion=20mil) (Conductor Width=5mil) (Air Gap=5mil) (Entries=4) (All)  Minimum Annular Ring (Minimum=5.118mil) (IsPad)  Outlinimum Annular Ring (Minimum=5.118mil) (IsVia)  Acute Angle Constraint [Tracks Only] (Minimum=45.000) (All)  Hole Size Constraint (Min=11.811mil) (Max=248.031mil) (All)  Hole To Hole Clearance (Gap=7.874mil) (All),(All)  Minimum Solder Mask Sliver (Gap=7.874mil) (All),(All)  Net Antennae (Tolerance=0mil) (All)  Board Clearance Constraint (Gap=0mil) (InLayerClass('Electrical Layers'))  LowPowerRoom (Bounding Region = (39504.59mil, 40260.392mil, 40172.144mil, 40418.41mil)  Component Clearance Constraint ( Horizontal Gap = 0mil, Vertical Gap = 0mil ) (All),(InComponentClass('TestPoint'))  Component Clearance Constraint ( Horizontal Gap = 0mil, Vertical Gap = Infinite ) (All),(All)  Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	Width Constraint (Min=5mil) (Max=50mil) (Preferred=5mil) (All)	0
Minimum Annular Ring (Minimum=5.118mil) (IsPad)  Minimum Annular Ring (Minimum=5.118mil) (IsVia)  Acute Angle Constraint [Tracks Only] (Minimum=45.000) (All)  Hole Size Constraint (Min=11.811mil) (Max=248.031mil) (All)  Hole To Hole Clearance (Gap=7.874mil) (All), (All)  Minimum Solder Mask Sliver (Gap=7.874mil) (All), (All)  Met Antennae (Tolerance=0mil) (All)  Board Clearance Constraint (Gap=0mil) (InLayerClass('Electrical Layers'))  LowPowerRoom (Bounding Region = (39504.59mil, 40260.392mil, 40172.144mil, 40418.41mil)  Component Clearance Constraint ( Horizontal Gap = 0mil, Vertical Gap = 0mil ) (All), (InComponentClass('TestPoint'))  Component Clearance Constraint ( Horizontal Gap = 0mil, Vertical Gap = Infinite ) (All), (All)  Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	Routing Via (Templates Used To Check Via: gnd_stitch, power_via, signal_routing) (All)	0
Minimum Annular Ring (Minimum=5.118mil) (IsVia)  Acute Angle Constraint [Tracks Only] (Minimum=45.000) (All)  Hole Size Constraint (Min=11.811mil) (Max=248.031mil) (All)  Hole To Hole Clearance (Gap=7.874mil) (All),(All)  Minimum Solder Mask Sliver (Gap=7.874mil) (All),(All)  Net Antennae (Tolerance=0mil) (All)  Board Clearance Constraint (Gap=0mil) (InLayerClass('Electrical Layers'))  LowPowerRoom (Bounding Region = (39504.59mil, 40260.392mil, 40172.144mil, 40418.41mil)  Component Clearance Constraint ( Horizontal Gap = 0mil, Vertical Gap = 0mil ) (All),(InComponentClass('TestPoint'))  Component Clearance Constraint ( Horizontal Gap = 0mil, Vertical Gap = Infinite ) (All),(All)  Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	Power Plane Connect Rule(Relief Connect )(Expansion=20mil) (Conductor Width=5mil) (Air Gap=5mil) (Entries=4) (All)	0
Acute Angle Constraint [Tracks Only] (Minimum=45.000) (All) Hole Size Constraint (Min=11.811mil) (Max=248.031mil) (All) Hole To Hole Clearance (Gap=7.874mil) (All),(All) Minimum Solder Mask Sliver (Gap=7.874mil) (All),(All) Net Antennae (Tolerance=0mil) (All) Soard Clearance Constraint (Gap=0mil) (InLayerClass('Electrical Layers')) LowPowerRoom (Bounding Region = (39504.59mil, 40260.392mil, 40172.144mil, 40418.41mil) Component Clearance Constraint ( Horizontal Gap = 0mil, Vertical Gap = 0mil ) (All),(InComponentClass('TestPoint')) Component Clearance Constraint ( Horizontal Gap = 0mil, Vertical Gap = Infinite ) (All),(All) Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	Minimum Annular Ring (Minimum=5.118mil) (IsPad)	0
Hole Size Constraint (Min=11.811mil) (Max=248.031mil) (All) Hole To Hole Clearance (Gap=7.874mil) (All),(All) Minimum Solder Mask Sliver (Gap=7.874mil) (All),(All) Net Antennae (Tolerance=0mil) (All) Board Clearance Constraint (Gap=0mil) (InLayerClass('Electrical Layers')) LowPowerRoom (Bounding Region = (39504.59mil, 40260.392mil, 40172.144mil, 40418.41mil) Component Clearance Constraint ( Horizontal Gap = 0mil, Vertical Gap = 0mil ) (All),(InComponentClass('TestPoint')) Component Clearance Constraint ( Horizontal Gap = 0mil, Vertical Gap = Infinite ) (All),(All) Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	Minimum Annular Ring (Minimum=5.118mil) (IsVia)	0
Hole To Hole Clearance (Gap=7.874mil) (All),(All)  Minimum Solder Mask Sliver (Gap=7.874mil) (All),(All)  Net Antennae (Tolerance=0mil) (All)  Board Clearance Constraint (Gap=0mil) (InLayerClass('Electrical Layers'))  LowPowerRoom (Bounding Region = (39504.59mil, 40260.392mil, 40172.144mil, 40418.41mil)  Component Clearance Constraint ( Horizontal Gap = 0mil, Vertical Gap = 0mil) (All),(InComponentClass('TestPoint'))  Component Clearance Constraint ( Horizontal Gap = 0mil, Vertical Gap = Infinite ) (All),(All)  Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	Acute Angle Constraint [Tracks Only] (Minimum=45.000) (All)	0
Minimum Solder Mask Sliver (Gap=7.874mil) (All), (All)  Net Antennae (Tolerance=0mil) (All)  Board Clearance Constraint (Gap=0mil) (InLayerClass('Electrical Layers'))  LowPowerRoom (Bounding Region = (39504.59mil, 40260.392mil, 40172.144mil, 40418.41mil)  Component Clearance Constraint ( Horizontal Gap = 0mil, Vertical Gap = 0mil ) (All), (InComponentClass('TestPoint'))  Component Clearance Constraint ( Horizontal Gap = 0mil, Vertical Gap = Infinite ) (All), (All)  Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	Hole Size Constraint (Min=11.811mil) (Max=248.031mil) (All)	0
Net Antennae (Tolerance=0mil) (All)  Board Clearance Constraint (Gap=0mil) (InLayerClass('Electrical Layers'))  LowPowerRoom (Bounding Region = (39504.59mil, 40260.392mil, 40172.144mil, 40418.41mil)  Component Clearance Constraint ( Horizontal Gap = 0mil, Vertical Gap = 0mil ) (All), (InComponentClass('TestPoint'))  Component Clearance Constraint ( Horizontal Gap = 0mil, Vertical Gap = Infinite ) (All), (All)  Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	Hole To Hole Clearance (Gap=7.874mil) (All),(All)	0
Board Clearance Constraint (Gap=0mil) (InLayerClass('Electrical Layers'))  LowPowerRoom (Bounding Region = (39504.59mil, 40260.392mil, 40172.144mil, 40418.41mil)  Component Clearance Constraint ( Horizontal Gap = 0mil, Vertical Gap = 0mil) (All), (InComponentClass('TestPoint'))  Component Clearance Constraint ( Horizontal Gap = 0mil, Vertical Gap = Infinite ) (All), (All)  Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)  O	Minimum Solder Mask Sliver (Gap=7.874mil) (All),(All)	0
LowPowerRoom (Bounding Region = (39504.59mil, 40260.392mil, 40172.144mil, 40418.41mil)  Component Clearance Constraint ( Horizontal Gap = 0mil, Vertical Gap = 0mil ) (All), (InComponentClass('TestPoint'))  Component Clearance Constraint ( Horizontal Gap = 0mil, Vertical Gap = Infinite ) (All), (All)  Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)  O	Net Antennae (Tolerance=0mil) (All)	0
Component Clearance Constraint ( Horizontal Gap = 0mil, Vertical Gap = 0mil ) (All),(InComponentClass('TestPoint'))  Component Clearance Constraint ( Horizontal Gap = 0mil, Vertical Gap = Infinite ) (All),(All)  Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)  0	Board Clearance Constraint (Gap=0mil) (InLayerClass('Electrical Layers'))	0
Component Clearance Constraint ( Horizontal Gap = 0mil, Vertical Gap = Infinite ) (All),(All) 0 Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All) 0	LowPowerRoom (Bounding Region = (39504.59mil, 40260.392mil, 40172.144mil, 40418.41mil)	0
Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	Component Clearance Constraint ( Horizontal Gap = 0mil, Vertical Gap = 0mil ) (All),(InComponentClass('TestPoint'))	0
•	Component Clearance Constraint ( Horizontal Gap = 0mil, Vertical Gap = Infinite ) (All),(All)	0
Total 0	Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	0
	Total	0

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