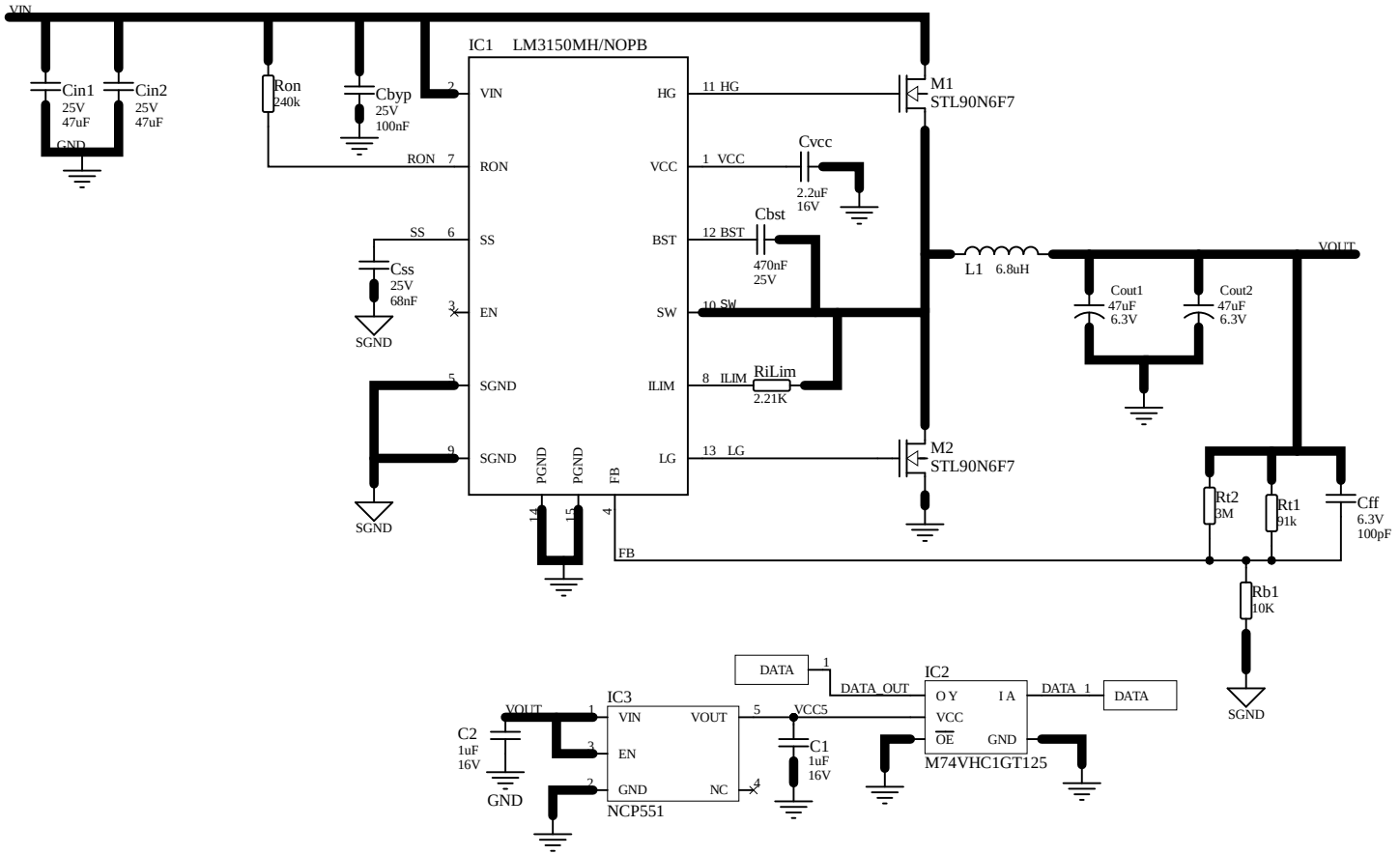
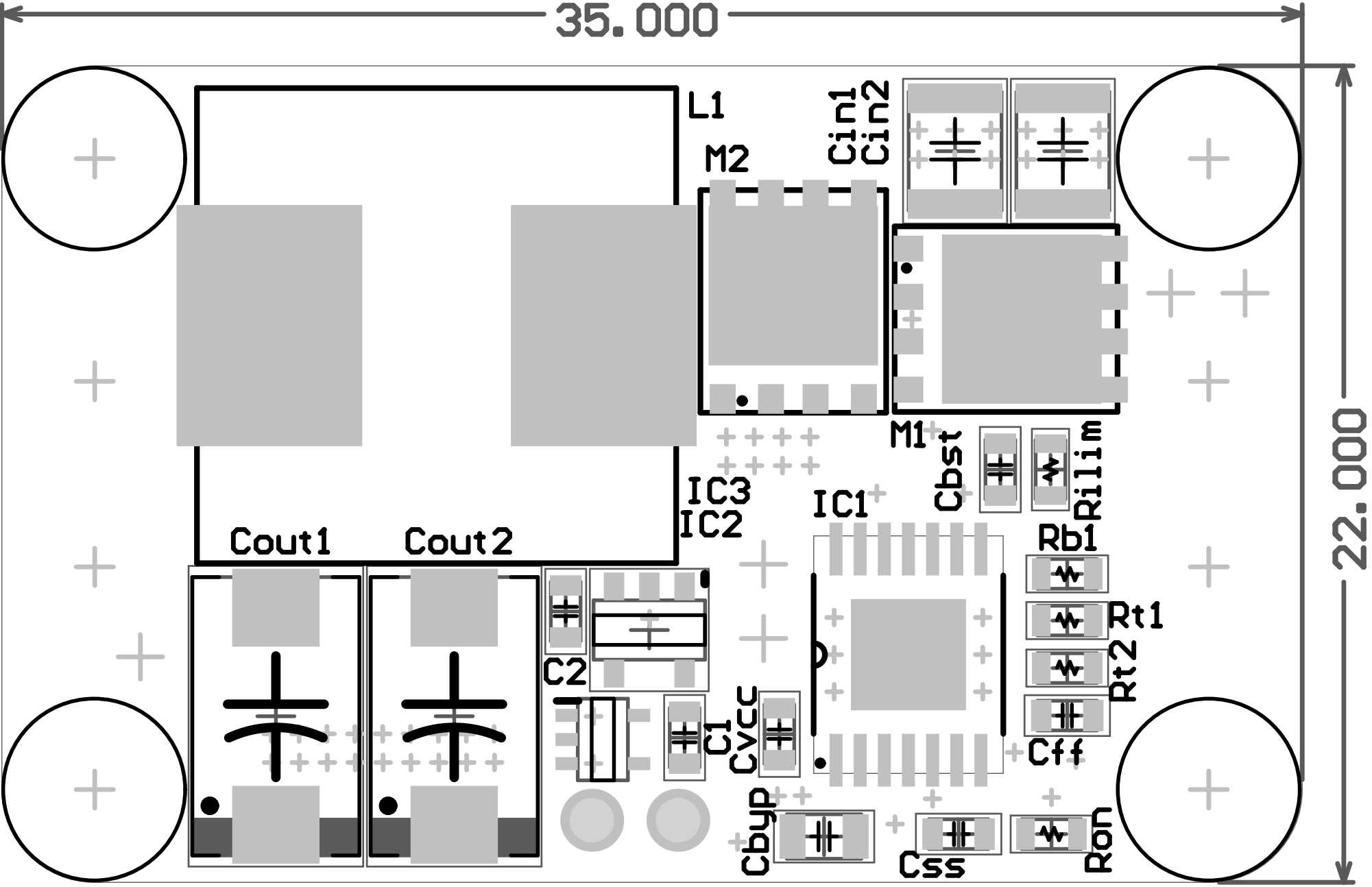


Title		
Size: A4	Number	Revision
Date: 7/28/2020		Sheet of
File: C:\Dev\..\buck4.schdoc		Drawn By:


35.000
22.000
L1
M2
Cin1
Cin2
M1
Cbst
Rilim
IC3
IC2
IC1
Rb1
Rt1
Rt2
Cout1
Cout2
C2
C1
Cvcc
Cff
Cbyp
Css
Ron

Name	Designator	Quantity	MPN	Vendor	Footprint	Description	Voltage	Value
MLCC	C1, C2	2			CAPC1608X08L	Multilayer Ceramic Capacitor	16V	1uF
MLCC	Cbst	1			CAPC1608X08L	Multilayer Ceramic Capacitor	25V	470nF
MLCC	Cbyp	1			CAPC2012X12L	Multilayer Ceramic Capacitor	25V	100nF
MLCC	Cff	1			CAPC1608X08L	Multilayer Ceramic Capacitor	6.3V	100pF
MLCC	Cin1, Cin2	2	C3216X5R1E476M160AC	TDK	CAPC3225X25L	Multilayer Ceramic Capacitor	25V	47uF
CAPACITOR	Cout1, Cout2	2	EEFCS1A470R	Pansonic	CAPMP7343X11L	Electrolytic Capacitor	6.3V	47uF
MLCC	Css	1			CAPC1608X08L	Multilayer Ceramic Capacitor	25V	68nF
MLCC	Cvcc	1			CAPC1608X08L	Multilayer Ceramic Capacitor	16V	2.2uF
LM3150MH/NOPB	IC1	1	LM3150MH/NOPB	Texas Instruments	MXA14A	Buck controller		
M74VHC1GT125	IC2	1			SOT65P210X100-5L	Level shifter non inverting		
NCP551	IC3	1			SOT95P260X90-5L			
744313330	L1	1	744313330	Wurth Elektronik	WE-HCI_1335	Inductor		6.8uH
STL90N6F7	M1	1	CSD17579Q5A	Texas Instruments	TRANS_NexFET_Q5A	N Channel MOSFET		
STL90N6F7	M2	1	CSD18537NQ5A	Texas Instruments	TRANS_NexFET_Q5A	N Channel MOSFET		
RES0603	Rb1	1			RESC1608X03L	Chip Resistor		10K
RES0603	RiLim	1			RESC1608X03L	Chip Resistor		2.21K
RES0603	Ron	1			RESC1608X03L	Chip Resistor		240k
RES0603	Rt1	1			RESC1608X03L	Chip Resistor		91k
RES0603	Rt2	1			RESC1608X03L	Chip Resistor		3M

Design Rules Verification Report

Filename : C:\Dev\wifi-christmas-tree-lights\pcbs\buck4\buck4.PcbDoc

Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.127mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Short-Circuit Constraint (Allowed=Yes) (InNet('GND')),(InNet('SGND'))	0
Un-Routed Net Constraint ((All))	0
Width Constraint (Min=0.127mm) (Max=2.54mm) (Preferred=0.127mm) (All)	0
Routing Via (Templates Used To Check Via: connector, gnd_stitch, signal_routing, v65h40m0mx0) (All)	0
Power Plane Connect Rule(Direct Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Hole Size Constraint (Min=0.025mm) (Max=4mm) (All)	0
Pads and Vias to follow the Drill pairs settings	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.2mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) (Not (OnLayer('Top Overlay') Or OnLayer('Bottom Overlay')))	0
Component Clearance Constraint (Horizontal Gap = 0.05mm, Vertical Gap = Infinite) (All),(All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	0