Design Rules Verification Report

Filename : S:\dev\ws2811\pcbs\buck3\buck3.PcbDoc

Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=15.748mil) (InNet('24V') Or InNet('VOUT')),(InNet('24V') Or InNet('VOUT'))	0
Clearance Constraint (Gap=5mil) (IsStitchingVia and InNet('SGND')),((IsVia and (Not IsStitchingVia)) Or IsPad)	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Net Antennae (Tolerance=0mil) (All)	0
Silk to Silk (Clearance=0mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=2mil) (All),(All)	0
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Hole Size Constraint (Min=11.811mil) (Max=100mil) (All)	0
Pads and Vias to follow the Drill pairs settings	0
Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	0
Component Clearance Constraint (Horizontal Gap = 10mil, Vertical Gap = 10mil) (All),(All)	0
Routing Via (MinHoleWidth=11.811mil) (MaxHoleWidth=39.37mil) (PreferredHoleWidth=11.811mil)	0
Routing Layers(All)	0
Width Constraint (Min=5mil) (Max=50mil) (Preferred=5mil) (All)	0
Power Plane Connect Rule(Direct Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4)	0
Clearance Constraint (Gap=5mil) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Short-Circuit Constraint (Allowed=Yes) (InNet('GND')),(InNet('SGND'))	0
Board Clearance Constraint (Gap=0mil) (All)	0
Board Clearance Constraint (Gap=0mil) (OnLayer('Top Overlay') or OnLayer('Bottom Overlay'))	0
Clearance Constraint (Gap=7.874mil) (InNet('SW') Or InNet('24V') Or InNet('VOUT') Or InNet('?DRV') Or InNet('GND')	0
Minimum Annular Ring (Minimum=3mil) (All)	0
Clearance Constraint (Gap=10mil) (InNet('HDRV') Or InNet('LDRV') Or InNet('SW')),(InNet('HDRV') Or InNet('LDRV') Or	0
Clearance Constraint (Gap=5mil) (IsStitchingVia and InNet('GND')),((IsVia and (Not IsStitchingVia)) Or IsPad)	0
Total	0