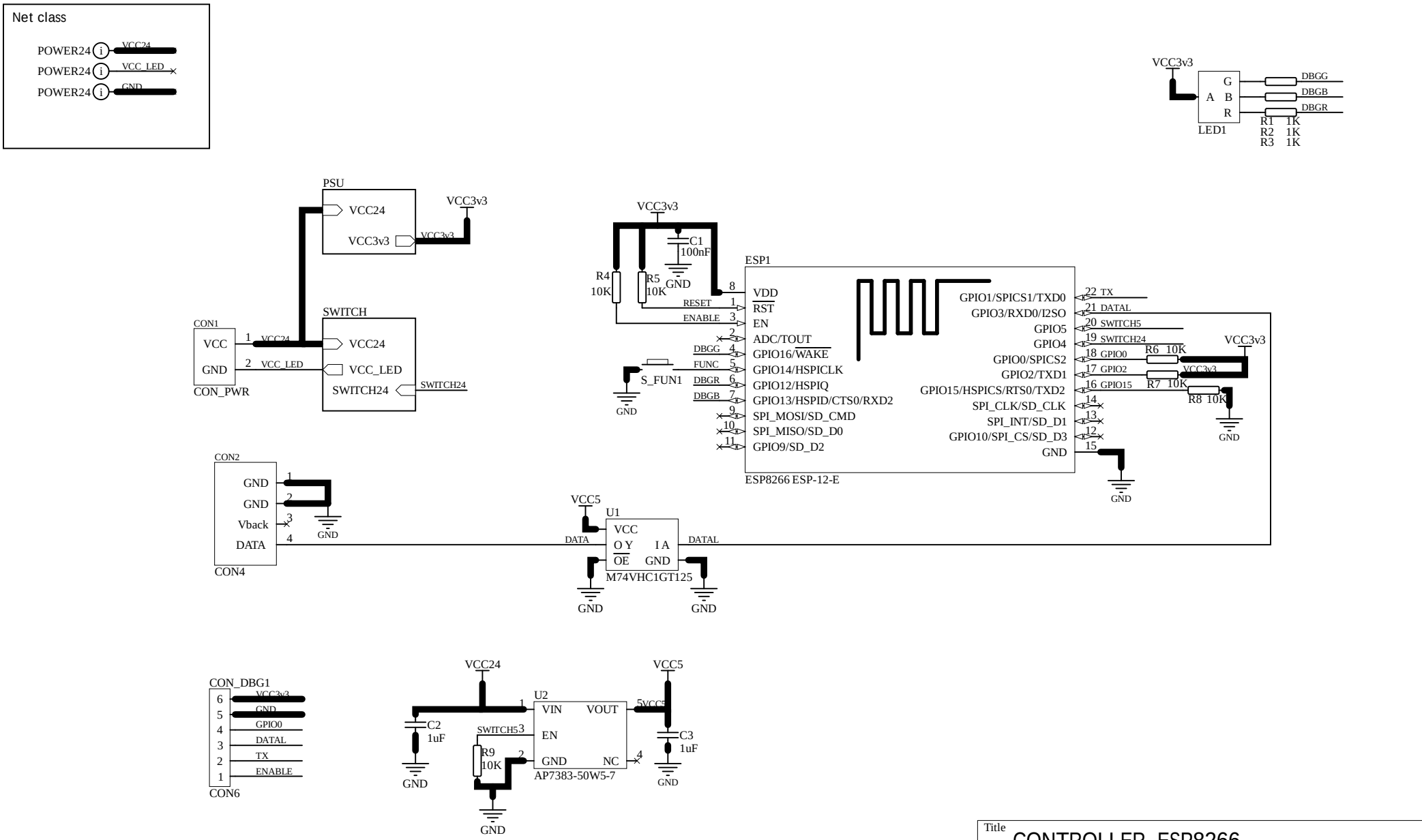
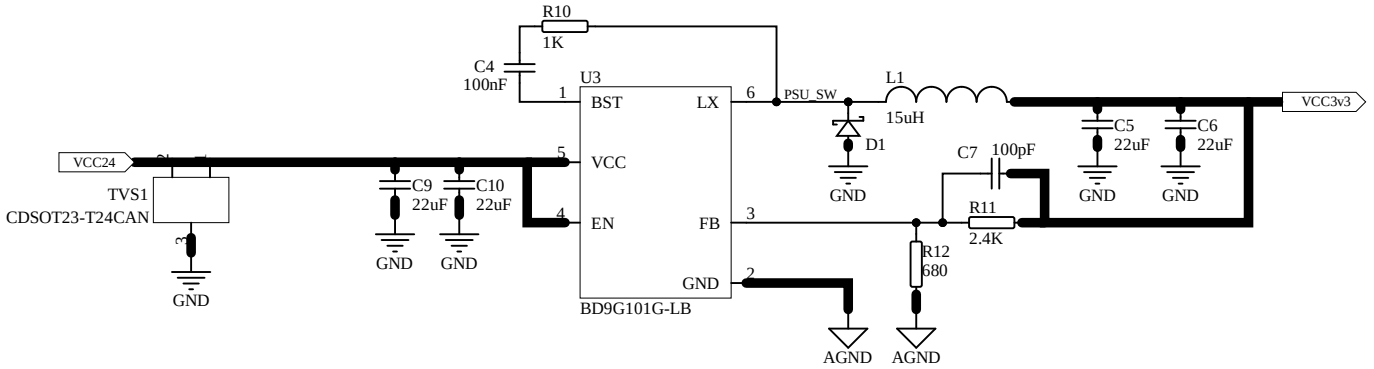


Title	CONTROLLER_ESP8266	
Size: A4	Number:	Revision:
Date: 8/14/2020		Sheet of
File: C:\Dev\..\controller_8266.SchDoc		Drawn By:



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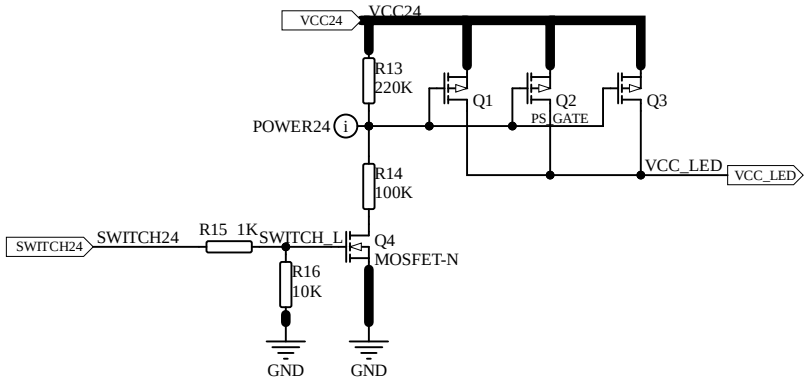
Size: A4	Number:	Revision:
Date: 8/14/2020		Sheet of
File: C:\Dev\..\controller_8266_psu.SchDoc		Drawn By:



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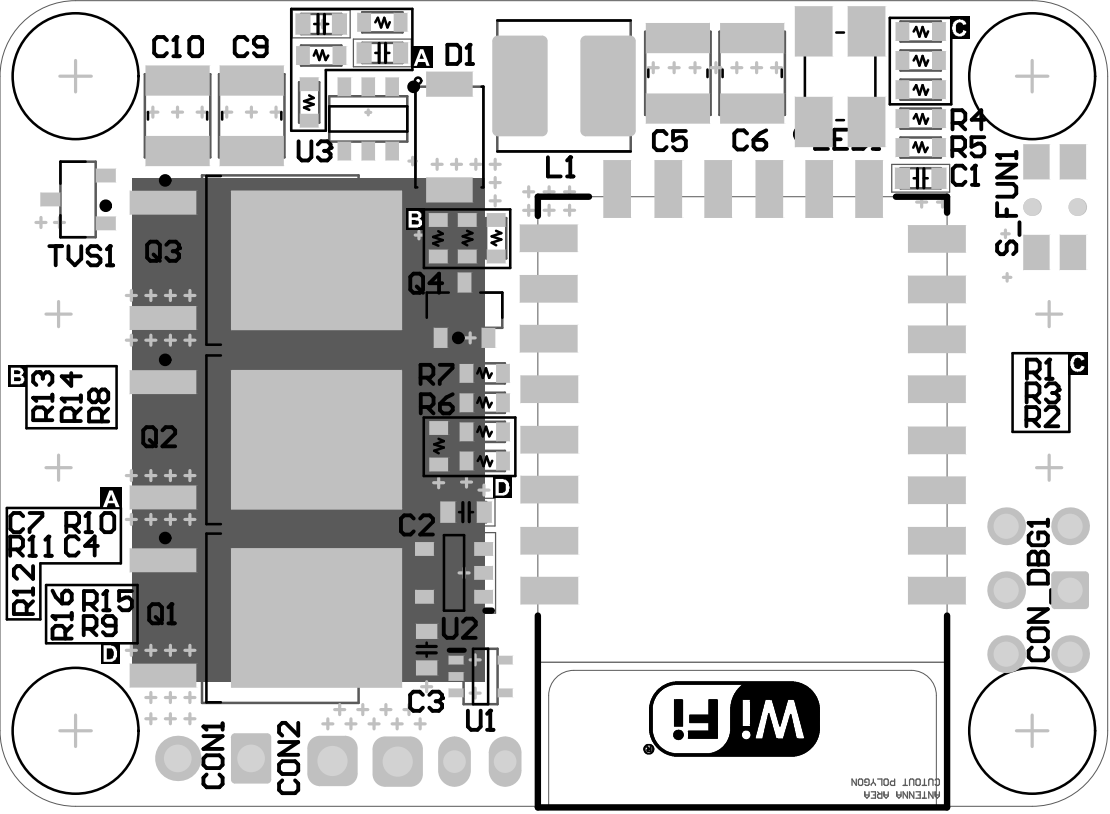
Size: A4	Number:	Revision:
Date: 8/14/2020	Sheet of	
File: C:\Dev\..\controller_8266_switch.SchDoc	Drawn By:	


C10
C9
U3
D1
A
C5
C6
L1
C
R4
R5
C1
S_FUN1
TVS1
Q3
B
Q4
R13
R14
R8
R7
R6
R1
R3
R2
Q2
D
C7
R10
C11
C4
A
C2
R12
R16
R15
R9
Q1
U2
CON_DBG1
C3
U1
CON1
CON2
ANTENNA AREA
CUTOUT POLYGON

Name	Designator	Quantity	MPN	Vendor	Footprint	Description	Voltage	Value
Cap	C1, C4	2			CAPC_0603_1608X08L	Capacitor		100nF
Cap	C2, C3	2			CAPC_0603_1608X08L	Capacitor		1uF
Cap	C5, C6, C9, C10	4			CAPC3224X25L	Capacitor		22uF
Cap	C7	1			CAPC_0603_1608X08L	Capacitor		100pF
Schottky 40V 3A	D1	1			SODFL470X110-2L	Schottky Diode		
ESP8266 ESP-12-E	ESP1	1			ESP8266 ESP-12-E	ESP8266 ESP-12-E		
Inductor	L1	1			INDP5150X20L	Inductor		15uH
RGB LED Common anode	LED1	1			PLCC-4	Dot is _not_ anode!		
MOSFET-P	Q1, Q2, Q3	3			DPAK229P994X241-3L			
MOSFET-N	Q4	1			SOT23			
Res2	R1, R2, R3, R10, R15	5			RESC_0603_1608X08L	Resistor		1K
Res2	R4, R5, R6, R7, R8, R9, R16	7			RESC_0603_1608X08L	Resistor		10K
Res2	R11	1			RESC_0603_1608X08L	Resistor		2.4K
Res2	R12	1			RESC_0603_1608X08L	Resistor		680
Res2	R13	1			RESC_0603_1608X08L	Resistor		220K
Res2	R14	1			RESC_0603_1608X08L	Resistor		100K
4-1437565-1	S_FUN1	1			EVQP7C01P	Tactile switch		
CDSOT23-T24CAN	TVS1	1			SOT23	Dual 24V TVS Diode		
M74VHC1GT125	U1	1			SOT65P210X100-5L	Level shifter non inverting		
AP7383-50W5-7	U2	1			SOT95P260X90-5L	5V LDO Vin_max 33V 150mA		
BD9G101G-LB	U3	1			TSOP95P280X125-6L			

Design Rules Verification Report

Filename : C:\Dev\wifi-christmas-tree-lights\pcbs\controller_8266\controller_8266.PcbDoc

Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=5mil) (All),(IsKeepOut)	0
Clearance Constraint (Gap=20mil) (InNetClass('POWER24') And ((IsPad And (InNet('GND') Or InNet('VCC_LED'))) Or	0
Clearance Constraint (Gap=5mil) (All),(All)	0
Clearance Constraint (Gap=-3.937mil) (InPadClass('AGND_TIE')),(InNet('GND') And OnBottomLayer)	0
Clearance Constraint (Gap=20mil) (InNet('PS_GATE') And (Not WithinRoom('LowPowerRoom'))),(InNet('VCC24'))	0
Short-Circuit Constraint (Allowed=Yes) (InPadClass('AGND_TIE')),(InNet('GND'))	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=5mil) (Max=50mil) (Preferred=5mil) (All)	0
Routing Via (Templates Used To Check Via: gnd_stitch, power_via, signal_routing) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=20mil) (Conductor Width=5mil) (Air Gap=5mil) (Entries=4) (All)	0
Minimum Annular Ring (Minimum=5.118mil) (IsPad)	0
Minimum Annular Ring (Minimum=5.118mil) (IsVia)	0
Acute Angle Constraint [Tracks Only] (Minimum=45.000) (All)	0
Hole Size Constraint (Min=11.811mil) (Max=248.031mil) (All)	0
Hole To Hole Clearance (Gap=7.874mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=7.874mil) (All),(All)	0
Net Antennae (Tolerance=0mil) (All)	0
Board Clearance Constraint (Gap=0mil) (InLayerClass('Electrical Layers'))	0
LowPowerRoom (Bounding Region = (39504.59mil, 40260.392mil, 40172.144mil, 40418.41mil)	0
Component Clearance Constraint (Horizontal Gap = 0mil, Vertical Gap = 0mil) (All),(InComponentClass('TestPoint'))	0
Component Clearance Constraint (Horizontal Gap = 0mil, Vertical Gap = Infinite) (All),(All)	0
Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	0
Total	0