Fault-finding the ETI-660 Learner's Microcomputer

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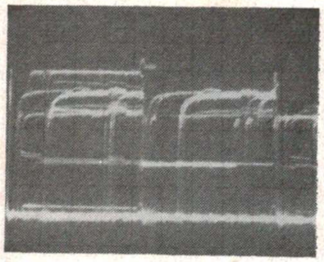
Having trouble firing up your '660? Has your '660 developed a fault? Or do you just want to learn more about the beast's internal workings? This article illustrates some techniques of fault-finding for this project as well as showing you more about its internal operation.

THIS ARTICLE endeavours to give constructors of the ETI-660 Learner's Microcomputer some fault-finding techniques to narrow down the *area* where a fault may exist, whether you are attempting to get your project up and running or trying to fix a problem which has developed later.

For many constructors, the ETI-660 is probably the most ambitious project ever undertaken. It would probably be the most difficult to fault-find!

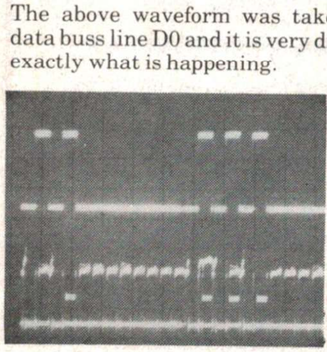
I will have to assume here that you have carried out the tests recommended during assembly. An oscilloscope was the only instrument used in preparing this article. If you possibly can, get hold of one, or access to one. The oscilloscope needs to be a dual beam type and have a vertical amplifier bandwidth of 10 MHz or greater. I used a Hewlett-Packard model 1740A 100 MHz oscilloscope for the tests illustrated here, mainly to obtain good results to photograph. However, you won't need anything as sophisticated or as costly as that! A dual beam 'scope is really a *must* because it allows you to view synchronised data from two sources or trigger the 'scope on one signal while investigating a related signal.

As a first example, have a look at what is *not* going to help you!



Looking at a data buss line (D0)

The above waveform was taken from the data buss line D0 and it is very difficult to see exactly what is happening.



Now here's something a bit more useful! This trace is still of the data buss, except that the CRO was triggered from the SC0 state code line pin 6, of the 1802 CPU. When using the 'scope on the '660, *always* have the Y amps switch to *dc*, so that you can see 'high' and 'low' levels immediately.

Flow chart

Fault-finding is a logical procedure where you work from *common* or *general* elements of the circuitry, toward *specific* elements. Fault symptons will give you a starting point. How does this work? To illustrate the procedure, and to give you a specific guide, I have drawn up a *fault-finding flow chart* for the '660.

Go through it carefully to see how it is structured. You may well have done some of the checks already. This chart won't lead you directly to the component or chip at fault, but it will certainly narrow down the area of the fault. From there you have relatively few things to check, which makes life considerably easier and fault-finding much less frustrating.

Note 1: At this stage we can assume that the initialisation software is running and that the 6821 (IC5) has been initialised also. The CPU is waiting for you to press one of the following keys:

$\boxed{0}$ $\boxed{2}$ $\boxed{4}$ $\boxed{8}$

Note 2: If a sound is heard in the speaker, the CPU must have acknowledged that you pressed key 0. Pressing the keys from 0 to F should produce an increasing-length tone with each successive key pressed.

In response to key 0 being pressed, the data in the address field (i.e: on the left of the bar along the bottom of the screen) of the display should be updated each time you press a key between 0 and F.

Note 3: If the keyboard doesn't cause a CPU response, then check the conditions on the 'A' port of the 6821 — I/O lines PA0-PA7. i.e: pins 2 — 9 of IC5.

The keyboard is divided into a 4 x 4 matrix with normally open contacts (note: constructors using the FES-310 pushbuttons should check that pin 1 of each button is aligned to the pin 1 dot indicator on the pc board).

Pins 2 to 5 of the 6821 connect to the 'columns' of the keyboard matrix, while pins 6 to 9 connect to the 'rows'. The column inputs are software programmed to be inputs, the internal pull-up resistors make pins 2-5 at logic 1 (high). Using the CRO, check that pins 2-5 are high. The remaining pins — 6 to 9 — are continually toggled inputs or outputs. Refer to Figure 1 for typical waveform.

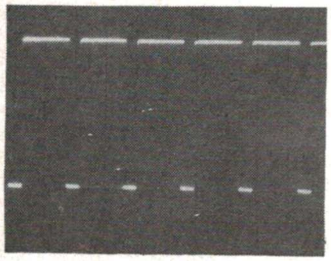


Figure 1.

Timebase set to 0.5 ms/cm

Y amp. set to 1 V/cm

Maintain the same timebase setting but change both Y amp sensitivities to 2 V/cm. Connect them to pins 9 and 5. Press the RESET key followed by the 0 key. Note the change in pulse rate on pin 9 and the changing of pin 5 to a low output. The software is endeavouring to locate the key depressed.

Pressing RESET followed by 8 will cause the CPU to run a CHIP 8 program, hence the keyboard scan subroutine is no longer used. Pins 6 to 9 of the 6821 drop to 0 (low).

The timing signals of the 6821 'read' cycle can be observed by connecting the CRO Y amp inputs to pins 22 (or 24) and 21. A 'chip select' (CS) for the 6821 is generated from the encoded 'N' lines of the 1802 (pins 17, 18, 19). The input code generated by the 1802 is decoded by IC17. (Note: on the circuit diagram, page 36 Nov. '81 ETI, pin 2 of IC17 is connected to pins 22/24 of IC5. Pin 21 of IC5 is the read/write line. When it is high and pins 22/24 high, data is transferred from the keyboard matrix to the data buss.)

Refer to Figure 2. The top trace is the 'select' pulse on pins 22/24 of IC5. The bottom trace is the read/write (R/W) signal generated by A2. With these two pulses going high together one can assume that the 6821 is being *read* by the CPU.

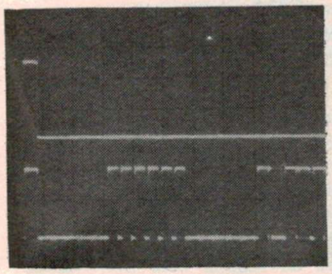


Figure 2.

Pins 22/24, IC5

A2

T/B 10 us/cm
Y amp 2 V/cm

To carry out a comparison, it is essential to trigger the 'scope on the top trace (pin 22/24, IC5) and look at the bottom trace for the condition of address line 2 (A2 — R/W for the 6821). At this stage, the 6821 appears to be working as expected. It is now necessary to check that the 1864 (IC4) is also selected by the decoded N lines. (An error in labelling appears at IC17 on the circuit diagram. Pins 1/14 of IC17 are shown to go to pins 17/19 of IC3 — that should be IC4.)

The tone generator latch in the 1864 is loaded by a '64' output instruction. To obtain any output from the AUDIO pin (pin 39) of the 1864, it is also necessary to activate the AUDIO OUTPUT ENABLE pin (AOE — pin 4). Referring to the circuit diagram you will see that pin 4 of IC4 is connected to pin 4 of IC3 (Q output). To allow the internal counter to toggle freely, pin 4 of the 1864 must be high. The frequency input to the audio generator is the TPB pulse generated by the 1802.

Connect the 'scope to pin 34 of the 1864 and you should observe a short duration positive-going pulse train. The TPA and TPB pulses occur once in each machine cycle and are used by I/O devices to interpret codes and to time interaction with the data buss. Set the CRO timebase to 2 us/cm to observe TPA or TPB.

Connect one Y amp of the 'scope to pin 4 of the 1864 and the other to pin 39. Repeated pressing of the RESET key should result in an audio frequency square wave appearing and should be heard from the speaker. If not, check the value of R20 (390R) and wiring to the speaker. Trace the track from R20 to the speaker. Just adjacent to pin 20 of IC5 is a through-board link. See that it's in place and properly soldered on both sides. If all is OK, replace the speaker with a *known good* one.

Note 4: The 1864 generates both composite and separate horizontal and vertical sync. signals. For monochrome operation, the composite sync. output ($\overline{\text{CSYNC}}$, pin 30) is combined with the RED video output (pin 29) in a simple resistive network to produce composite video output. Note that this is a high impedance output and cannot be connected directly to the 75 ohm input common to most video monitors. The video refresh cycle of the display section of the 1864 is synchronised with the 1802 using $\overline{\text{INT}}$ (pin 36 on both chips), $\overline{\text{EF}}$ (pin 18, IC4) and $\overline{\text{EF1}}$ (pin 24, IC3) and the state code lines SC0 and SC1 (pins 5 and 6 of IC3).

Pin 18 on the 1864 pulses at twice the frame frequency, goes low for four horizontal lines prior to the start of display and low again for four horizontal lines prior to the end of display.

Connect one Y amp of the 'scope to pin 18 and the other to pin 36 of the 1864 and observe these pulsing lines. The pulsing lines indicate that the 1864 is requesting a display update. Now connect the 'scope inputs to pins 5 and 6 on the 1864. Your waveform should look something like that in Figure 3.

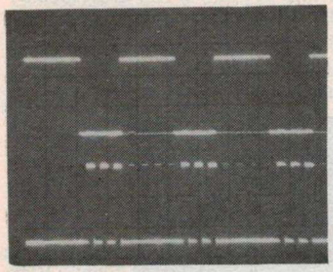


Figure 3.

SC1

SC0

T/B 10 us/cm
Y amps
2 V/cm

Pin 30 of the 1864 has the composite sync. output on it. Connect the 'scope to this pin and you should get something like Figure 4.

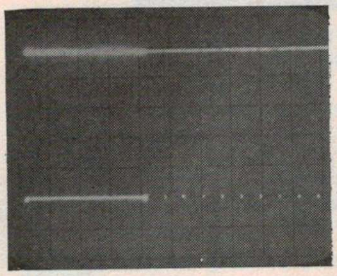


Figure 4.

T/Ba
20 ms/cm
T/Bb
0.1 ms/cm
Y amp 1 V/cm

You should observe little bright-up dots 20 ms apart (50 Hz), the frame frequency sync. pulses (actually, they're 19.8 ms apart — 50.6 Hz). Now speed up the CRO time base to 0.1 ms/cm or faster. You should observe the horizontal sync. pulses. Figure 4 shows both frame and horizontal sync. pulses. This was achieved using the expanded timebase feature of the 'scope I used. Change the input lead over to pin 29 of IC4. Set the timebase back to 5 ms/cm. Figure 5 shows the RED video output signal, in this case as the luminance output signal.

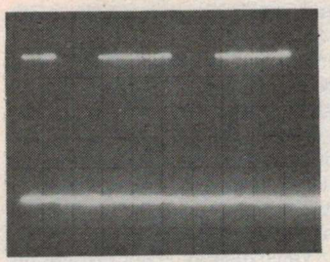


Figure 5.

Red video output, 1864

T/B 5 ms/cm
Y amp 1 V/cm

The signals from pins 29 and 30 are combined in the resistor matrix R11-7-10 to produce a composite video signal of the right sync.-to-video levels. Figure 6 shows the resulting combination.

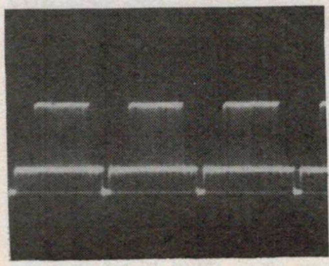
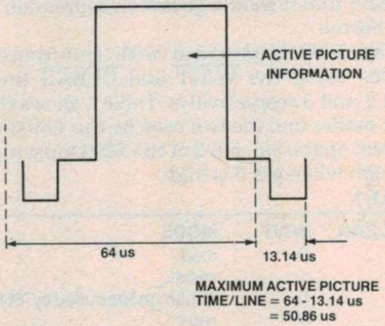


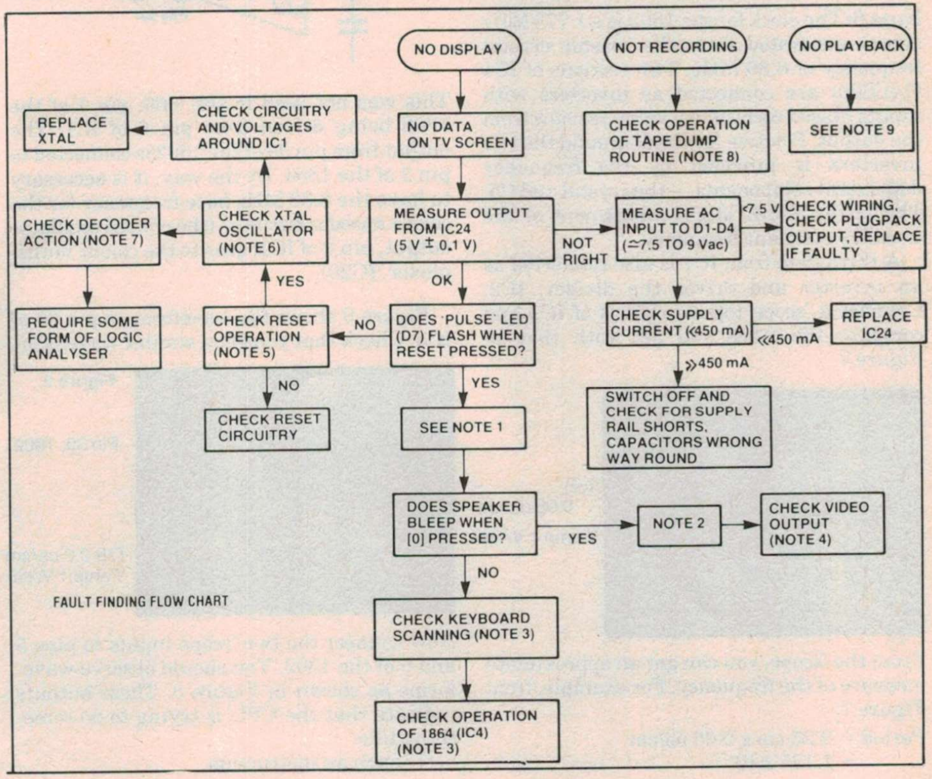
Figure 6.

Composite video.

T/B 5 ms/cm

Y amp
0.5 V/cm





FAULT FINDING FLOW CHART

NO DISPLAY
NOT RECORDING
NO PLAYBACK
NO DATA ON TV SCREEN
CHECK OPERATION OF TAPE DUMP ROUTINE (NOTE 8)
SEE NOTE 9
REPLACE XTAL
CHECK CIRCUITRY AND VOLTAGES AROUND IC1
CHECK DECODER ACTION (NOTE 7)
CHECK XTAL OSCILLATOR (NOTE 6)
MEASURE OUTPUT FROM IC24 (5 V ± 0.1 V)
NOT RIGHT
MEASURE AC INPUT TO D1-D4 (≃7.5 TO 9 Vac)
<7.5 V
CHECK WIRING, CHECK PLUGPACK OUTPUT, REPLACE IF FAULTY
YES
OK
REQUIRE SOME FORM OF LOGIC ANALYSER
CHECK RESET OPERATION (NOTE 5)
NO
DOES 'PULSE' LED (D7) FLASH WHEN RESET PRESSED?
CHECK SUPPLY CURRENT (≪450 mA)
≪450 mA
REPLACE IC24
≫450 mA
NO
YES
CHECK RESET CIRCUITRY
SEE NOTE 1
SWITCH OFF AND CHECK FOR SUPPLY RAIL SHORTS, CAPACITORS WRONG WAY ROUND
DOES SPEAKER BLEEP WHEN [0] PRESSED?
YES
NOTE 2
CHECK VIDEO OUTPUT (NOTE 4)
NO
CHECK KEYBOARD SCANNING (NOTE 3)
CHECK OPERATION OF 1864 (IC4) (NOTE 3)

Connect the 'scope input to the junction of resistors R7, 11 and 10, set the Y amp to 0.5 V/cm and compare your results with ours, shown in Figure 6.

The maximum dc level of the waveform represents *peak white* on the screen and the bottom of the sync. pulses represents black level or zero volts dc. This is why an inverter is required in the ETI-760 video modulator (Q2) when a composite video signal is fed into the FET output modulator (Q3). If you are obtaining the same amplitude signal as in Figure 6, but video display is not present on your TV, check your modulator. (Note: R11 is shown on the '660 circuit diagram as 2k2, but in the text it is given as 5k6. A value of 2k2 should be used to give proper sync. levels.)

Note 5: The 1802 receives a reset signal from the 1864 controller chip. On power-up, capacitor C3 pulls pin 38, the $\overline{\text{CLRIN}}$ input of IC4, low (0) for the approximate period of 3 x R2C3 time constant. The low level input into the Schmitt trigger on pin 38 of IC4 will cause $\overline{\text{CLROUT}}$, pin 3, to go low also. $\overline{\text{CLROUT}}$ is connected to the $\overline{\text{CLEAR}}$ input of the 1802, pin 3. The post-Schmitt trigger output provides the 1802 with a clean, clear signal.

Connect one 'scope input to pin 3 of the 1802. There should be a 'high' here. Press RESET and it should go low on depression of the button.

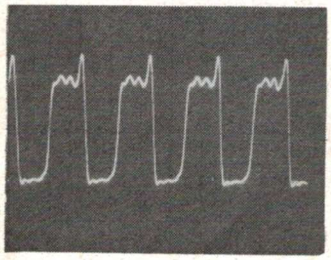
The 1802 is provided with four control modes using the $\overline{\text{WAIT}}$ and $\overline{\text{CLEAR}}$ lines (pin 2 and 3 respectively). Table 1 shows the four modes and the two used by the '660. For correct operation, pin 2 of the 1802 must also be high when pin 3 is high.

TABLE 1.

CLEAR	WAIT	MODE
0	0	load
0	1	reset
1	0	pause modes used by '660
1	1	run

Note 6: The clock for the 1802 is a 1.773 MHz signal generated from the master crystal frequency of 8.86 MHz. Two sections of IC1 (74LS00) are connected as inverters with inputs biased up by a low value resistor from the output. Positive feedback around the two inverters is provided by the frequency dependant components — the crystal and C5. The latter allows slight adjustment of the crystal's resonant frequency.

A third gate from IC1 is also connected as an inverter and drives the divider, IC2. Connect a 'scope input to pin 3 of IC1 and compare the trace you get with that in Figure 7.



T/B 0.05 us/cm
Y amp 1 V/cm

From the 'scope, you can get an approximate measure of the frequency. For example, from Figure 7:

Period = 2.25 cm x 0.05 us/cm
= 1.125×10^{-7}

$$\text{Frequency} = \frac{1}{\text{Period}}$$
$$= 8.88 \times 10^6$$
$$= 8.88 \text{ MHz}$$

Which is pretty close to the intended 8.86 MHz, showing you the oscillator's operating in the right ballpark.

The waveform at pin 3 of IC1 is divided by five in IC2. Change the 'scope input now to pin 1 of IC3. Change the timebase to 0.2 us/cm and compare your waveform with that in Figure 8.

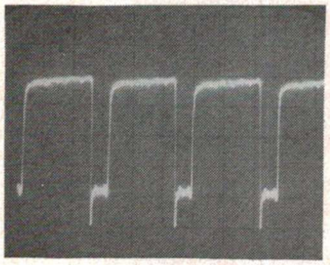


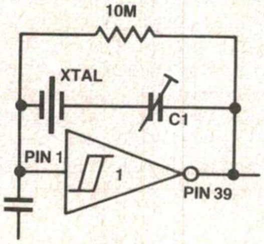
Figure 8.

Pin 1, 1802

T/B 0.2 us/cm
Y amp 1 V/cm

It is normal practice to supply the clock input of a microprocessor with a 1:1 mark/space ratio pulse. However, in this case it is not possible because of the odd division ratio from the crystal frequency to generate the necessary 1.773 MHz clock. The 1802 would not accept the output pulse from IC2 directly, but did accept the inverted version, hence the need for IC1d.

The crystal is normally connected between pins 1 and 39 of the 1802 (clock and $\overline{\text{XTAL}}$), in parallel with a resistance of typically 10 M.



This was not used in the '660, pin 1 of the 1802 being driven from pin 6 of IC1. The output from pin 39 of the 1802 is connected to pin 2 of the 1864. By the way, it is necessary to have the 8.86 MHz base frequency for the colour encoder circuitry (the crystal oscillator output, pin 8 of IC1, goes to the colour multiplexer, IC20).

Figure 9 shows the waveform on pin 39 of IC3. Check that you get a similar waveform.

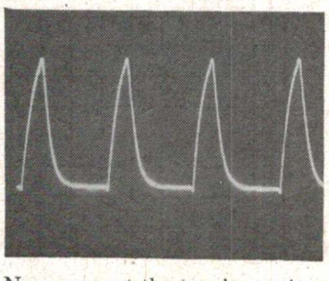


Figure 9.

Pin 39, 1802

T/B 0.2 us/cm
Y amp 1 V/cm

Now connect the two 'scope inputs to pins 5 and 6 of the 1802. You should observe waveforms as shown in Figure 3. These outputs indicate that the CPU is trying to do something like:

(1) fetch an instruction
(2) execute an instruction
(3) acknowledge an interrupt request
(4) process a DMA request

The latter two are normally used as a result of the 1864 causing a display update.

Note 7: With the 1802, the 16-bit address data is multiplexed onto a common eight lines, MA0-7. i.e: pins 25 to 32 of IC3. The higher order byte of a 16-bit memory address appears on the memory address lines first. Those bits required by the memory system, A8-A11, can be stored into an external address latch (IC6) by the timing pulse TPA.

Connect the 'scope inputs to pins 4 and 15 (MA10) of IC6 and trigger the 'scope on the TPA pulse. Compare your waveforms with Figure 10.

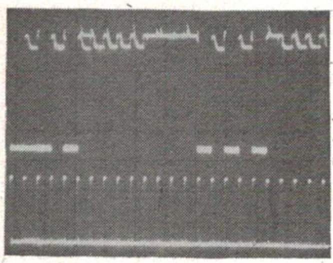


Figure 10.

MA10

T/B 10 us/cm
Y amp 2 V/cm

TPA

The data presented to IC6 is latched when the TPA pulse is low. The high address lines A10 and A11, from the latch, are supplied to the address decoder, IC8. While the monitor is running and scanning the keyboard, the chip select lines of IC11 (pin 20) and ICs 9 and 10 (pin 14 on each) should be pulsing. Connect the 'scope inputs to pins 14 and 15 (address decoder outputs) and check your waveforms against those in Figure 11.

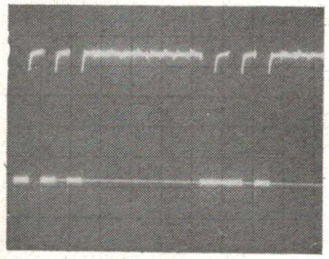


Figure 11.

Pin 20, IC11

T/B 10 us/cm
Y amp 1 V/cm

See that you get the chip select signal on IC11 pin 20.

The RAM chips IC9 and IC10 are selected because the display data is stored here, along with monitor 'scratch pad' data, in the memory block 0400 to 07FF. Table 2 shows the chip select logic — which memory block is selected by which output (chip select line) of IC8.

TABLE 2.

A11	A10	CHIP SELECT ACTIVE	MEMORY BLOCK
0	0	pin 15, IC8	0000 — 03FF
0	1	pin 14, IC8	0400 — 07FF
1	0	pin 13, IC8	0800 = 0BFF
1	1	pin 12, IC8	0C00 — 0FFF

Using the 'scope, observe pin 20 of IC11 while you press and hold down the RESET button. Pin 20 should go low and remain low. On reset, the memory address lines are reset to 0000, therefore the address decoder will generate a chip select for the bottom memory block, 0000 — 03FF. Failure to achieve this will indicate a fault in the address latch (IC6) or decoder (IC8).

The monitor EPROM (IC11) must be selected by a RESET otherwise the 1802 will run on some other addressed random data. The decoder chip, IC8, divides the lower memory block into 1K blocks by using A10 as the least significant bit (LSB).

If the problem has not been found by any of the test sequences described here, it is now necessary to locate someone that has a logic analyser. This instrument is connected onto the data buss and several timing pulse outputs. It tracks and stores in its own memory the microprocessor's operation after a certain trigger 'word'. The stored information is displayed on a terminal or 'scope. This then allows the user to determine whether the microprocessor is following the monitor program or where it went to instead.

Note 8: The code for the tape load routine is generated in software and sent out from the 1802 using the Q output, pin 4. Pressing RESET followed by 2 should cause —

(1) audio tone to be heard from the speaker
(2) the pulse LED to flash at a high rate.

If you look at pin 4 of the 1802, you should see a waveform as shown in Figure 12.

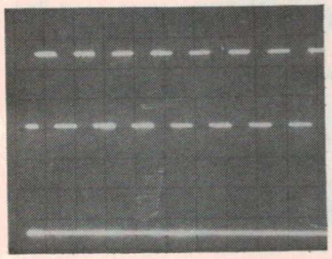


Figure 12.

Pin 4, 1802

After 6 — 10 seconds, the leader tone gives way to the actual data from memory being loaded in 256-byte lumps as a two-tone FSK signal. A 'scope connected to pin 5 of IC7 should produce a signal amplitude of approximately 2.4 V peak-to-peak. If no sound output occurs, refer to note 3 on the operation of the 1864. No Q output pulse (pin 4) will indicate a fault in the EPROM software. Take your EPROM to someone that has a microprocessor system that will allow you to check the listing contained in IC11, the 2716.

Note 9: The signal from the tape recorder is fed into one of the op-amp sections of IC7. Output from this is used to drive the flag input ($\overline{EF2}$) of the 1802. For the CMOS input to recognise a change in state, the signal from the op-amp (pin 9) must exceed about 3.5 V. Connect your tape recorder output to the tape input socket of the '660 and start it running (with a tape installed!). Using the 'scope, observe the amplitude of the waveform on pin 23 of IC3. Remember, it must exceed 3.5 V peak for the 1802 flag input to change state. If not, look for insufficient gain from the op-amp or lack of recorder level. Check the values of R31, 32 and 33.

Conclusion

Here's hoping this article has led you along the right path to find faults in your '660 and perhaps shown you a thing or two more about its operation that you didn't know before.