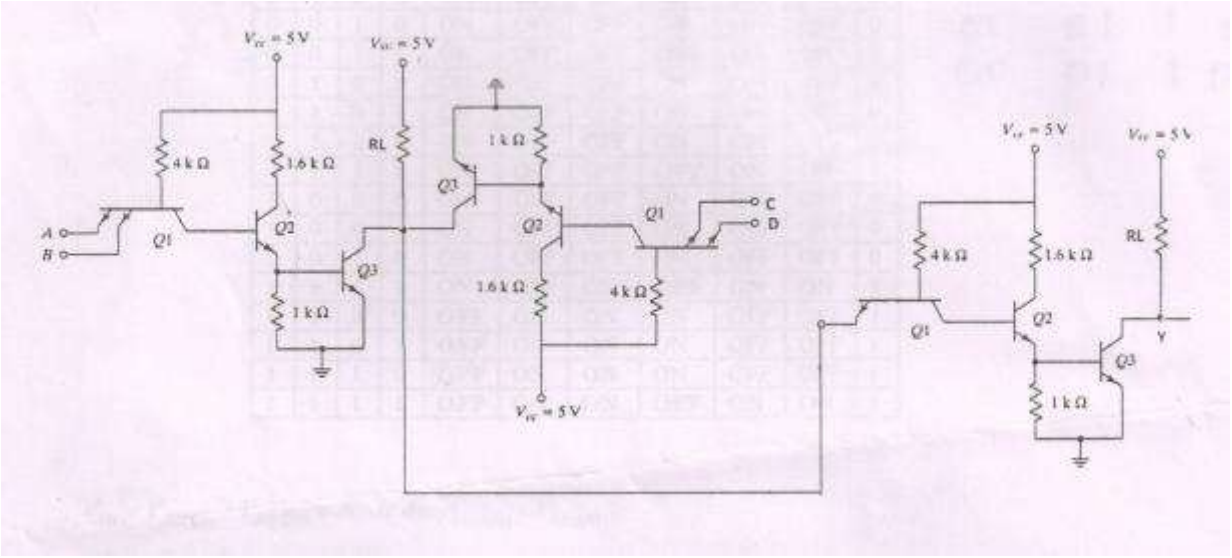
Birla Institute of Technology and Science, Pilani, Rajasthan
Digital Design (EEE F215/INSTR F215/ECE F215/CS F215)
I Semester (2025-2026)
Tutorial-11 (28th and 31st Nov 2025)

Q1.

a) Find the Boolean logic function (Y) for the given TTL logic circuit in terms of inputs A, B, C, and D

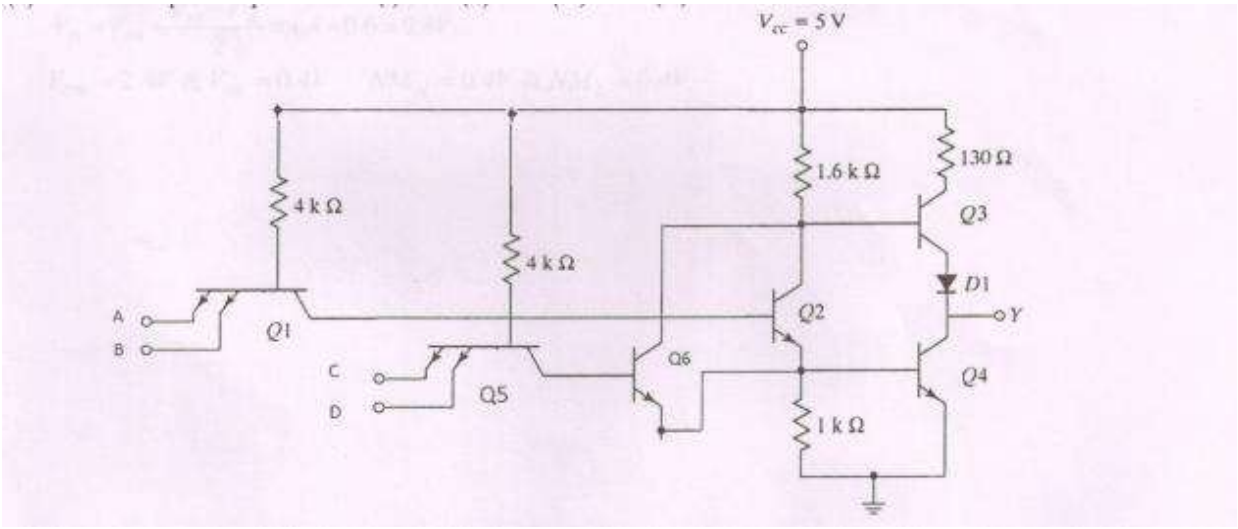
b) If the diode drop in the base collector junction of Q_1 is 0.7 V and $V_{BE(SAT)}$ =0.7V, determine the minimum input voltage that can be interpreted as logic '1', i.e. V IH and the maximum input voltage that can be interpreted as logic '0', i.e., V_{IL}. (Given: V_{1H}-V_{1L}= 1.2 V)

c) Also calculate noise margin high and noise margin low if V_{OH}=2.4 and V_{OL}=0.4.



Q2.

(a) For the following TTL logic circuit, find the Boolean logic function (Y) in terms of inputs A, B, C, and D. (b) Write the output if input 'ABCD' (i) 0000 (ii) 0011 (iii) 0101 (iv) 1111.


V_{cc} = 5 V
4 k Ω
4 k Ω
1.6 k Ω
130 Ω
Q3
D1
Y
A
B
Q1
Q2
C
D
Q5
Q6
Q4
1 k Ω