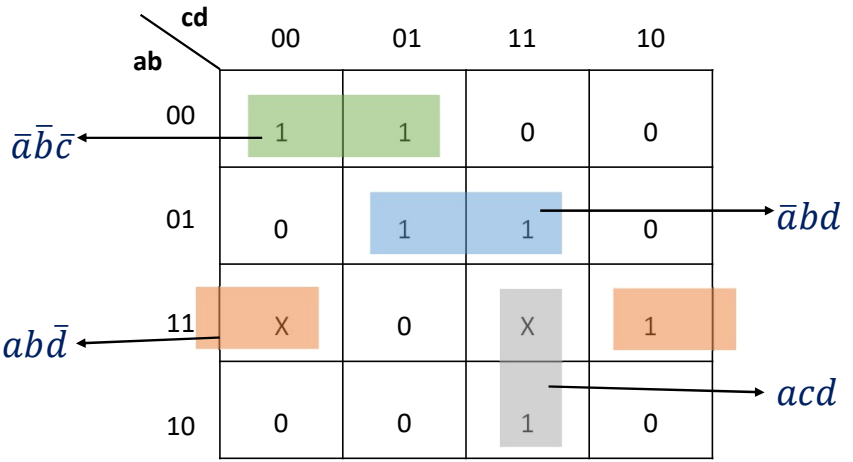
Ques 1: Given a Boolean function

$$f(a,b,c,d) = \sum m(0,1,5,7,11,14) + d(12,15)$$

Implement the function with a minimal network of 2:1 multiplexer. Consider that true and false forms of inputs are available.

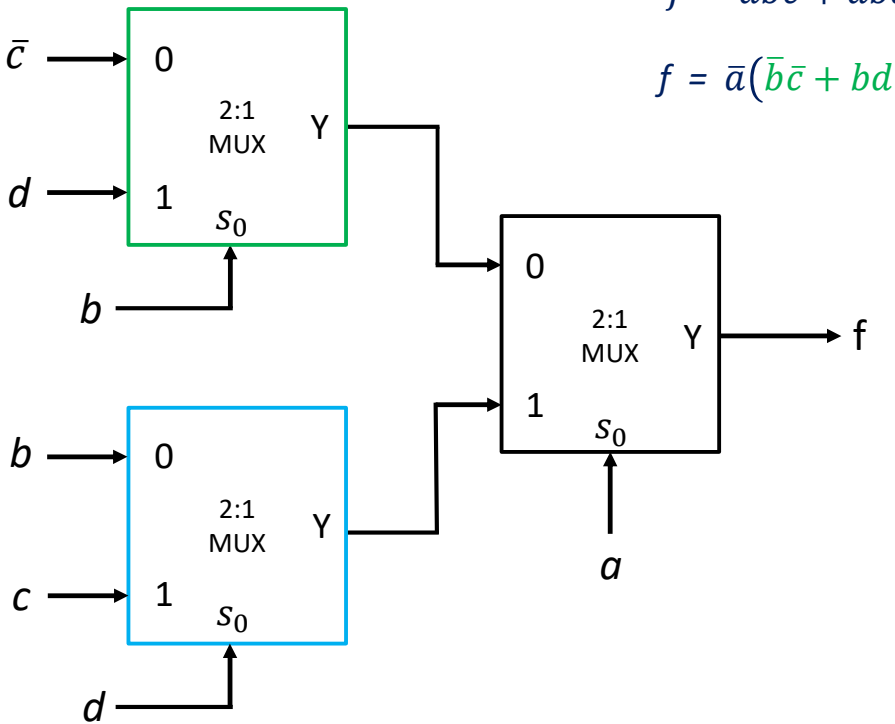
$$f(a,b,c,d) = \sum m(0,1,5,7,11,14) + d(12,15)$$



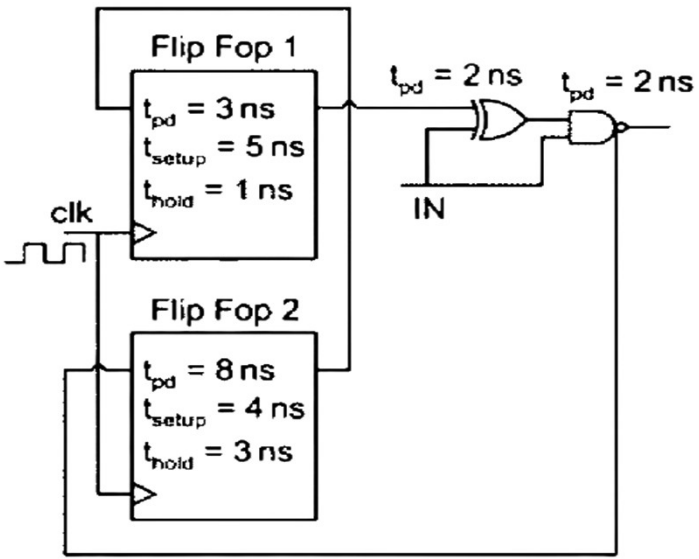
$$\boldsymbol{f(a,b,c,d) = \bar{a}\bar{b}\bar{c} + \bar{a}bd + ab\bar{d} + acd}$$

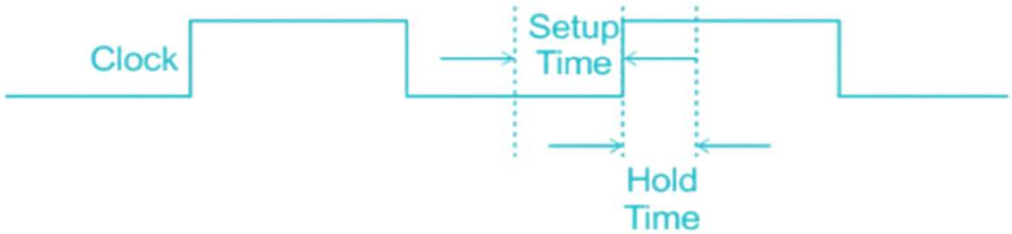
$$f = \bar{a}\bar{b}\bar{c} + \bar{a}bd + ab\bar{d} + acd$$

$$f = \bar{a}\left(\bar{b}\bar{c} + bd\right) + a(b\bar{d} + cd)$$



Ques 2: For the sequential circuit shown below, t_{pd} is the propagation delay, t_{setup} is the setup time, and t_{hold} is the hold time. Find the maximum clock frequency at which this circuit can operate reliably.





Setup Time: It is the amount of time for which the data at the synchronous input must be stable before the active edge of the clock.

Hold Time: It is the amount of time for which the data of the synchronous input must be stable after the active edge of the clock.

Maximum clock frequency = The minimum time after which the next clock edge arrives

For Flip-Flop 1:

After the arrival of a clock edge, the output becomes stable after t_{pd} = 8 ns.

The output is then passed through on XOR gate and a NAND gate.

The net delay will be: 3ns + 2ns + 2ns = 7ns

This output from the NAND gate after 7 nsec must remain stable for at least t_{setup} time of FF2

So, the minimum time after which the next clock edge should arrive at FF 1 is

$(T_{min})_{FF1}$ = 7 ns +4ns **= 11 ns**

For Flip-Flop 2:

After the arrival of a clock edge, the output becomes stable after $\mathbf{t_{hold}}$ = 3 ns.

The output of FF2 is the input to FF1, this output after tpd = 8 ns must remain stable for at least (t_{setup}) time of FF1, i.e.. for 5 ns, before the next clock edge should arrive at FF1.

The minimum time after which the next clock should arrive at FF1 should be:

$(T_{min})_{FF2}$ = 8 ns + 5ns = **13 ns**

For the given circuit to operate reliably, the minimum clock time

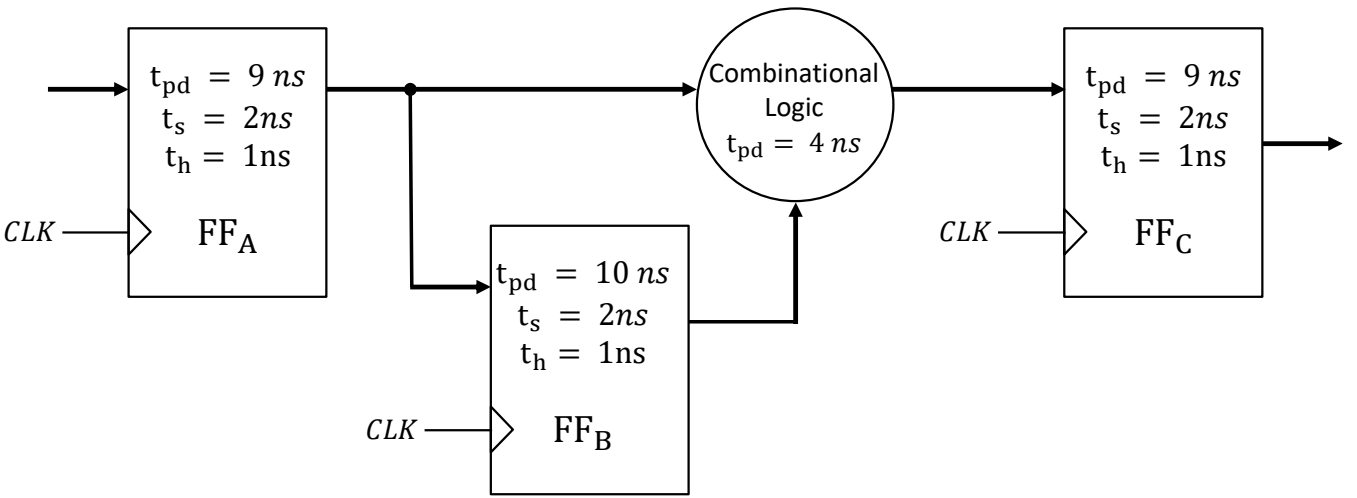
$$(T_{min})_{CLK} = \max[(T_{min})_{FF1}\ , (T_{min})_{FF2}] = 13 \text{ ns}$$

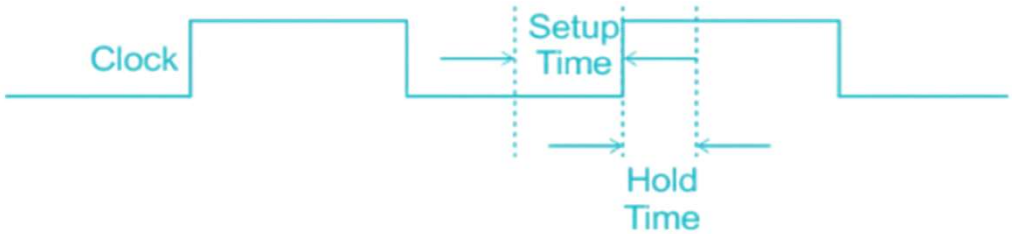
The maximum clock frequency will be

$$(f_{clk})max = \frac{1}{(T_{min})_{CLK}}$$

$$(f_{clk})max = \frac{1}{13 \text{ ns}} = \mathbf{76.92\ MHz}$$

Ques 3: For the sequential circuit shown below, t_{pd} is the propagation delay, t_{setup} is the setup time, and t_{hold} is the hold time. Find the maximum clock frequency at which this circuit can operate reliably.





Setup Time: It is the amount of time for which the data at the synchronous input must be stable before the active edge of the clock.

Hold Time: It is the amount of time for which the data of the synchronous input must be stable after the active edge of the clock.

Input is applied at FF_A and output is obtained at FF_C.

Two possible routes from input to output:

1. $FF_A \longrightarrow$ Comb. logic $\longrightarrow FF_C$

Minimum time required for stable output at FF_c :

$$9\text{ ns} + 4\text{ ns} + 2\text{ ns} = 15\text{ ns}$$

2. $FF_A \longrightarrow FF_B \longrightarrow$ Comb. logic $\longrightarrow FF_C$

Minimum time required for stable output at FF_c :

$$10\text{ ns} + 4\text{ ns} + 2\text{ ns} = 16\text{ ns}$$

$(T_{min})_{CLK}$ = max[(T_{min})FF1 , (T_{min})FF2] = 16 ns

The maximum clock frequency will be

$$(f_{clk})max = \frac{1}{(Tmin)CLK}$$

$$(f_{clk})max = \frac{1}{16\text{ ns}} = \boldsymbol{62.5\ MHz}$$

Ques 4: Transform the S-R flip flop to

a) T flip flop
b) J-K flip flop
c) D flip flop

Characteristics equation of SR Flip-flop: $S + \overline{R}\,Q_n = Q_{n+1}$ (applied S.R = 0)

Characteristics equation of T Flip-flop: $T + Q_n = Q_{n+1}$

Characteristics equation of JK Flip-flop: $J\,\overline{Q}_n + \overline{K}Q_n = Q_{n+1}$

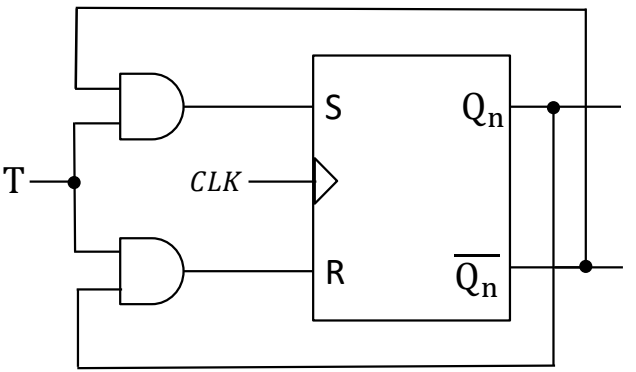
Characteristics equation of D Flip-flop: $D = Q_{n+1}$

Transforming SR Flip-flop to T Flip-flop

Characteristic Table of T Flip-flop			Excitation Table of SR Flip-flop	
T	Q_n	Q_{n+1}	**S**	**R**
0	0	0	0	X
0	1	1	X	0
1	0	1	1	0
1	1	0	0	1

Solving K-map for S and R separately with T and Q_n as inputs, we get:

$\boldsymbol{S = T\overline{Q_n}}$ and $\boldsymbol{R = TQ_n}$

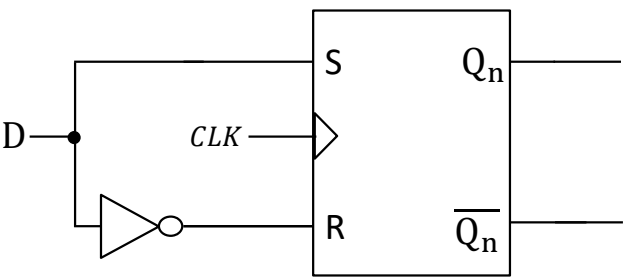


Transforming SR Flip-flop to D Flip-flop

Characteristic Table of D Flip-flop			Excitation Table of SR Flip-flop	
D	Q_n	Q_{n+1}	**S**	**R**
0	0	0	0	X
0	1	0	0	1
1	0	1	1	0
1	1	1	X	0

Solving K-map for S and R separately with D and Q_n as inputs, we get:

$\boldsymbol{S = D}$ and $\boldsymbol{R = \overline{D}}$



Transforming SR Flip-flop to JK Flip-flop

Characteristic Table of JK Flip-flop				Excitation Table of SR Flip-flop	
J	**K**	Q_n	Q_{n+1}	**S**	**R**
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	X	0
1	1	0	1	1	0
1	1	1	0	0	1

Solving K-map for S and R separately with D and Q_n as inputs, we get:

$$\boldsymbol{S = J\overline{Q_n}} \text{ and } \boldsymbol{R = K\,Q_n}$$