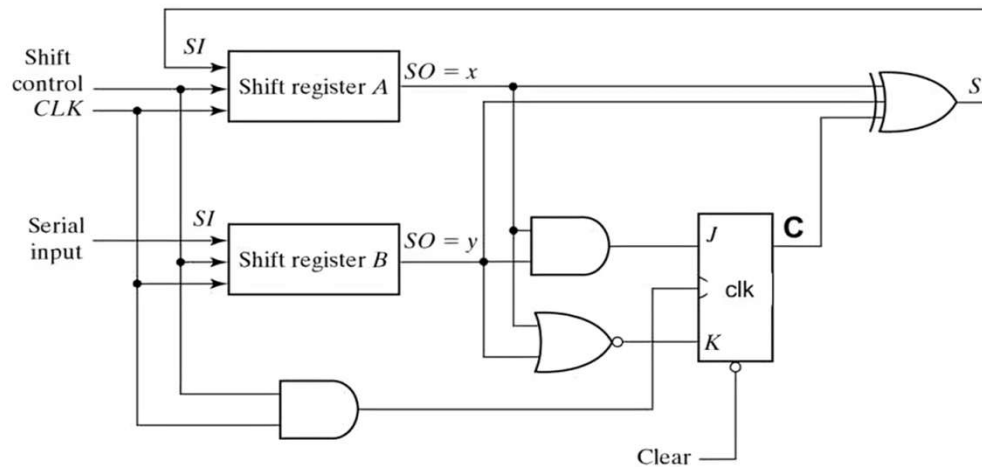Ques. Shift Reg B in the circuit below receives alternating 0 and 1 at SI at each clock cycle. Shift Reg A is loaded with value 1010 at t = 0 (the state of all memory elements at t = 0 is shown in the partial timing diagram on the right).

Draw the timing diagram for register A. What is the sequence of values taken by register A for the next 20 cycles?

SI	0				
A3	1				
A2	0				
A1	1				
A0	0				
B0	0				
C	0				

Ques: Realize F1 and F2 below using a minimum size PLA. Give the size of and draw the PLA table.

$$F_1(W,X,Y,Z) = \sum m(1,2,4,5,6,8,10,12,14)$$

$$F_2(W,X,Y,Z) = \sum m(2,4,6,8,10,11,12,14,15)$$

Ques. Design a 1-bit serial in and serial output (SISO) subtractor circuit using shift registers and J-K Flipflops.