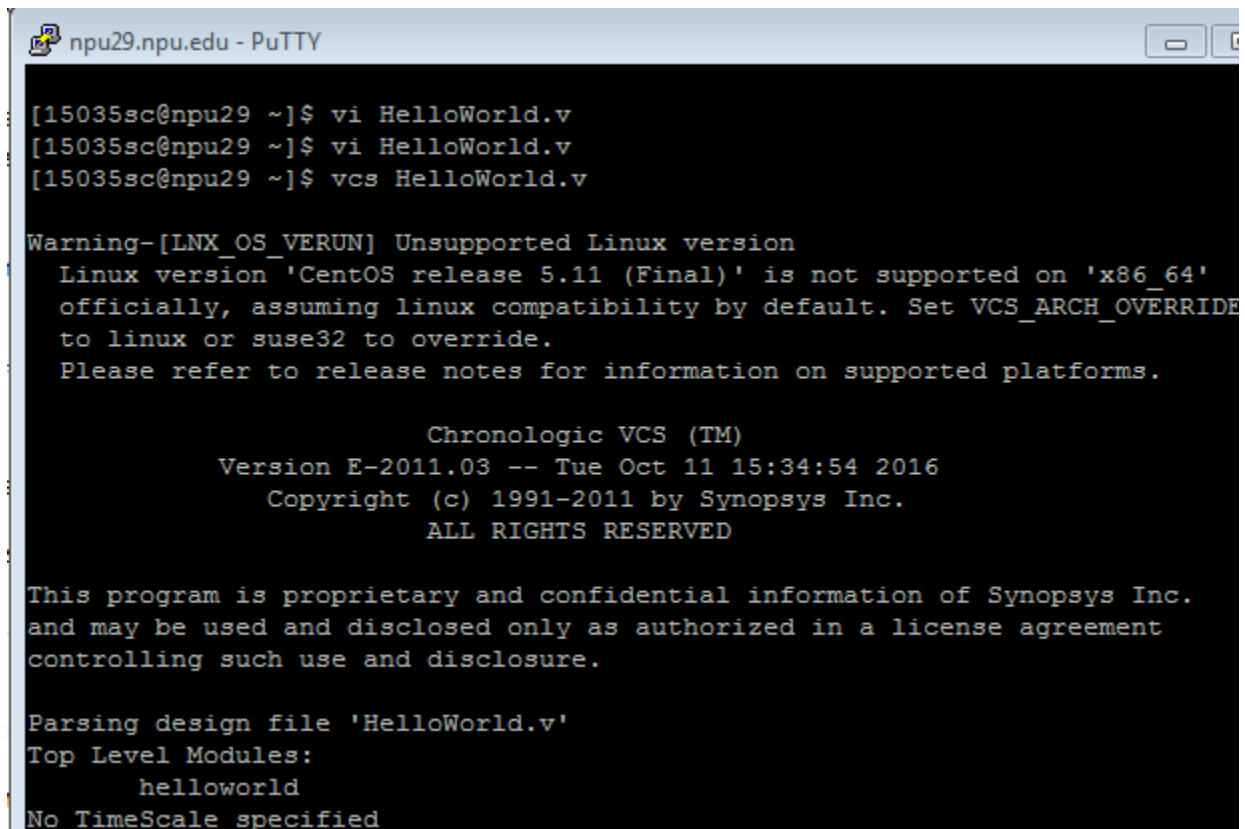


Chiragkumar solanki

15035

1. Write the program to verify whether white space "Carriage Return" and "Formfeed" in "helloWorld.v" work or not, and show the result.



```
npu29.npu.edu - PuTTY

[15035sc@npu29 ~]$ vi HelloWorld.v
[15035sc@npu29 ~]$ vi HelloWorld.v
[15035sc@npu29 ~]$ vcs HelloWorld.v

Warning-[LNX_OS_VERUN] Unsupported Linux version
Linux version 'CentOS release 5.11 (Final)' is not supported on 'x86_64'
officially, assuming linux compatibility by default. Set VCS_ARCH_OVERRIDE
to linux or suse32 to override.
Please refer to release notes for information on supported platforms.

Chronologic VCS (TM)
Version E-2011.03 -- Tue Oct 11 15:34:54 2016
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Parsing design file 'HelloWorld.v'
Top Level Modules:
    helloworld
No TimeScale specified
```

```

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Parsing design file 'HelloWorld.v'
Top Level Modules:
    helloworld
No TimeScale specified
Starting vcs inline pass...
1 module and 0 UDP read.
recompiling module helloworld because:
    This module or some inlined child module(s) has/have been modified.
if [ -x ../simv ]; then chmod -x ../simv; fi
g++ -o ../simv -melf_i386 -m32 -Wl,-whole-archive -Wl,-no-whole-archive
vcsobj_1_1.o 5NrI_d.o 5NrIB_d.o SIM_1.o rmapats_mop.o rmapats.o /ee/t
ols/synopsys/vcs/E-2011.03/linux/lib/libvirsim.so /ee/tools/synopsys/vcs/E-2011
03/linux/lib/librterrorinf.so /ee/tools/synopsys/vcs/E-2011.03/linux/lib/libsnp
malloc.so /ee/tools/synopsys/vcs/E-2011.03/linux/lib/libvcsnew.so /ee/tools
synopsys/vcs/E-2011.03/linux/lib/libuclnactive.so /ee/tools/synopsys/vc
/E-2011.03/linux/lib/vcs_save_restore_new.o /ee/tools/synopsys/vcs/E-2011.03/li

```

```

[15035sc@npu29 ~]$ ./simv
Chronologic VCS simulator copyright 1991-2011
Contains Synopsys proprietary information.
Compiler version E-2011.03; Runtime version E-2011.03; Oct 11 15:40 2016
hello world
      V C S   S i m u l a t i o n   R e p o r t
Time: 0
CPU Time:      0.480 seconds;      Data structure size:  0.0Mb
Tue Oct 11 15:40:35 2016

```

```

[15035sc@npu29 ~]$ ./simv
Chronologic VCS simulator copyright 1991-2011
Contains Synopsys proprietary information.
Compiler version E-2011.03; Runtime version E-2011.03; Oct 11 15:42 2016
Carriage return formfeed
      V C S   S i m u l a t i o n   R e p o r t
Time: 0
CPU Time:      0.470 seconds;      Data structure size:  0.0Mb
Tue Oct 11 15:42:56 2016
[15035sc@npu29 ~]$ █

```

FAULT: See VCS ARCH OVERRIDE

2. If a variable name is defined using a keyword, write a code snippet to look at what will happen and show error/warning information.

```
npu29.npu.edu - PuTTY
to linux or suse32 to override.
Please refer to release notes for information on supported platforms.

Chronologic VCS (TM)
Version E-2011.03 -- Tue Oct 11 15:45:25 2016
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Parsing design file 'HelloWorld.v'

Error-[UST] Undefined System Task Call
HelloWorld.v, 4
  Undefined System Task call to '$keyword'.

1 error
CPU time: .039 seconds to compile
[15035sc@npu29 ~]$ ./simv
./simv: Command not found.
[15035sc@npu29 ~]$
```

3. When a module name is &\$\$abc_123, how to make it pass compilation by writing a program to verify?

```
npu29.npu.edu - PuTTY
Please refer to release notes for information on supported platforms

Chronologic VCS (TM)
Version E-2011.03 -- Tue Oct 11 16:04:36 2016
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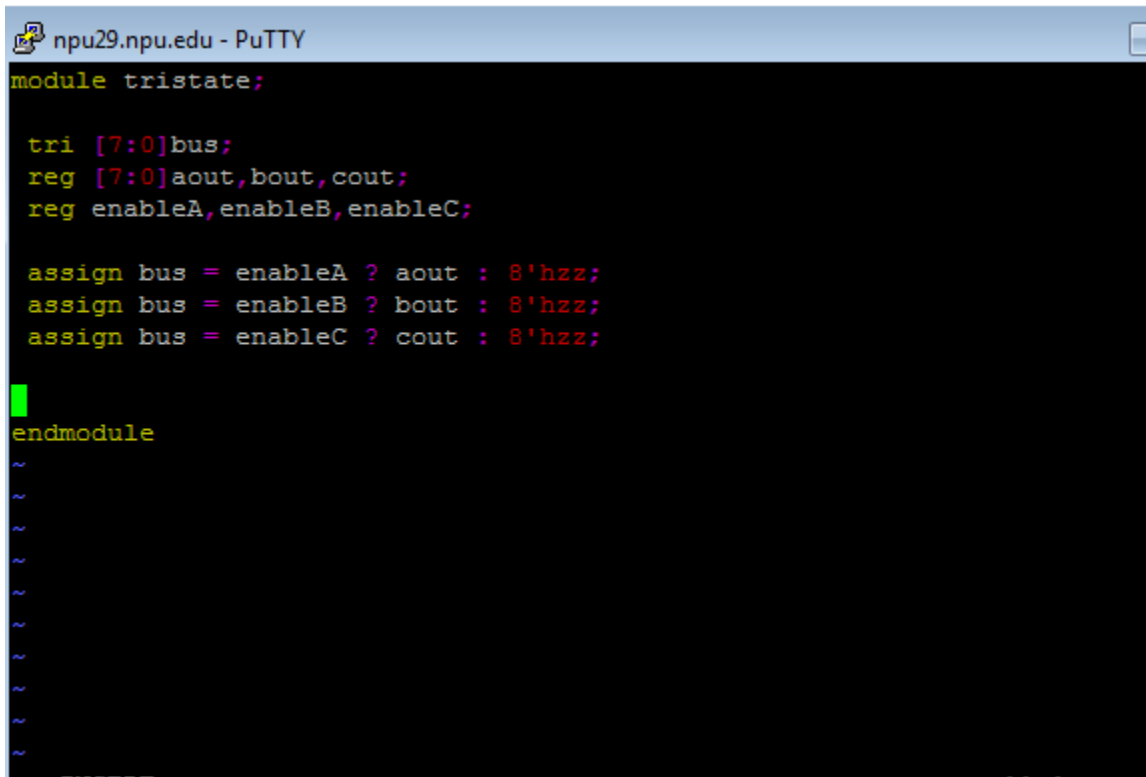
This program is proprietary and confidential information of Synopsys Inc.
and may be used and disclosed only as authorized in a license agreement
controlling such use and disclosure.

Parsing design file 'moduletest.v'

Error-[SE] Syntax error
Following verilog source has syntax error :
"moduletest.v", 1: token is '&'
module &$$abc_123
    ^

1 error
CPU time: .040 seconds to compile
[15035sc@npu29 ~]$ ./simv
```

4. Define a variable type “tri”, and make two devices in the same value(e.g. 1, 1) and different value(e.g. z, x) to drive it, what do you get and show running results? Take an example on the handout as reference.



```
npu29.npu.edu - PuTTY
module tristate;

    tri [7:0]bus;
    reg [7:0]aout,bout,cout;
    reg enableA,enableB,enableC;

    assign bus = enableA ? aout : 8'hzz;
    assign bus = enableB ? bout : 8'hzz;
    assign bus = enableC ? cout : 8'hzz;

endmodule
~
~
~
~
~
~
~
~
~
~
```

```
npu29.npu.edu - PuTTY
1 module and 0 UDP read.
recompiling module tristate because:
    Generated file (BHP2_1) not found, or not incremental.
if [ -x ../simv ]; then chmod -x ../simv; fi
g++ -o ../simv -melf_i386 -m32 -Wl,-whole-archive -Wl,-no-whole-archive
vcsobj_1_1.o 5NrI_d.o 5NrIB_d.o SIM_1.o rmapats_mop.o rmapats.o /ee
ols/synopsys/vcs/E-2011.03/linux/lib/libvirsim.so /ee/tools/synopsys/vcs/E-20
03/linux/lib/librterrorinf.so /ee/tools/synopsys/vcs/E-2011.03/linux/lib/lib
malloc.so /ee/tools/synopsys/vcs/E-2011.03/linux/lib/libvcsnew.so /ee/too
synopsys/vcs/E-2011.03/linux/lib/libuclimative.so /ee/tools/synopsys/
/E-2011.03/linux/lib/vcs_save_restore_new.o /ee/tools/synopsys/vcs/E-2011.03/
ux/lib/ctype-stubs_32.a -ldl -lc -lm -lpthread -ldl
../simv up to date
CPU time: .046 seconds to compile + .027 seconds to elab + .125 seconds to li
[15035sc@npu29 ~]$ ./simv
Chronologic VCS simulator copyright 1991-2011
Contains Synopsys proprietary information.
Compiler version E-2011.03; Runtime version E-2011.03; Oct 11 16:31 2016
V C S S i m u l a t i o n R e p o r t
Time: 0
CPU Time: 0.470 seconds; Data structure size: 0.0Mb
Tue Oct 11 16:31:49 2016
[15035sc@npu29 ~]$
```

5.

5. Retype “wor/trior” and “wand/triand” test programs on the handout and assign all 16- combination values to them. Compare the results with the values in truth table. And show results.

npu29.npu.edu - PuTTY

```
if [ -x ../simv ]; then chmod -x ../simv; fi
g++ -o ../simv -melf_i386 -m32 -Wl,-whole-archive -Wl,-no-whole-archive
vcsobj_1_1.o 5NrI_d.o 5NrIB_d.o SIM_1.o rmapats_mop.o rmapats.o /ee/
ols/synopsys/vcs/E-2011.03/linux/lib/libvirsim.so /ee/tools/synopsys/vcs/E-20
03/linux/lib/librterrorinf.so /ee/tools/synopsys/vcs/E-2011.03/linux/lib/libst
malloc.so /ee/tools/synopsys/vcs/E-2011.03/linux/lib/libvcsnew.so /ee/too
synopsys/vcs/E-2011.03/linux/lib/libuclivative.so /ee/tools/synopsys/v
/E-2011.03/linux/lib/vcs_save_restore_new.o /ee/tools/synopsys/vcs/E-2011.03/
ux/lib/ctype-stubs_32.a -ldl -lc -lm -lpthread -ldl
../simv up to date
CPU time: .054 seconds to compile + .039 seconds to elab + .158 seconds to li
[15035sc@npu29 ~]$ ./simv
Chronologic VCS simulator copyright 1991-2011
Contains Synopsys proprietary information.
Compiler version E-2011.03; Runtime version E-2011.03; Oct 13 18:53 2016
$time = 0 , bus =0
$time = 1 , bus =1
$finish called from file "wortrior.v", line 19.
$finish at simulation time 4
V C S S i m u l a t i o n R e p o r t
Time: 4
CPU Time: 0.470 seconds; Data structure size: 0.0Mb
Thu Oct 13 18:53:37 2016
[15035sc@npu29 ~]$
```

npu29.npu.edu - PuTTY

```
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Parsing design file 'wortrior.v'
Top Level Modules:
    Testtrior
No TimeScale specified
Starting vcs inline pass...
1 module and 0 UDP read.
recompiling module Testtrior because:
    Generated file (Jx3B_1) not found, or not incremental.
if [ -x ../simv ]; then chmod -x ../simv; fi
g++ -o ../simv -melf_i386 -m32 -Wl,-whole-archive -Wl,-no-whole-archive _
vcsobj_1_1.o 5NrI_d.o 5NrIB_d.o SIM_1.o rmapats_mop.o rmapats.o /ee/to
ols/synopsys/vcs/E-2011.03/linux/lib/libvirsim.so /ee/tools/synopsys/vcs/E-2011.
03/linux/lib/librterrorinf.so /ee/tools/synopsys/vcs/E-2011.03/linux/lib/libsnps
malloc.so /ee/tools/synopsys/vcs/E-2011.03/linux/lib/libvcsnew.so /ee/tools/
synopsys/vcs/E-2011.03/linux/lib/libuclivative.so /ee/tools/synopsys/vcs
/E-2011.03/linux/lib/vcs_save_restore_new.o /ee/tools/synopsys/vcs/E-2011.03/lin
ux/lib/ctype-stubs_32.a -ldl -lc -lm -lpthread -ldl
../simv up to date
CPU time: .054 seconds to compile + .039 seconds to elab + .158 seconds to link
[15035sc@npu29 ~]$
```

```
npu29.npu.edu - PuTTY
```

```
module Testtrior;  
    trior bus;  
  
    reg Aout,Bout;  
    reg EnableA,EnableB;  
  
    assign bus = EnableA ? Aout:8'hz;  
    assign bus = EnableB ? Bout:8'hz;  
  
    initial begin  
  
        $monitor ("Time = %g , bus =%b" , $time ,bus );  
        EnableA=1;  
        EnableB=1;  
        Aout=0;  
        Bout=0;  
        #1 Aout=1;  
        #1 Bout=1;  
        #2 $finish;  
  
    end  
endmodule
```

```
"wortrior.v" 23L, 352C                22,1                All
```

6. Generate variable type "tri0/tri1", and assign 4 different values (0, 1, X, Z) to observe what you are going to

```
npu29.npu.edu - PuTTY
module tristate();

    tri [7:0]bus;
    reg [7:0]Aout,Bout,Cout,Dout;

reg EnableA,EnableB,EnableX,EnableZ;

assign bus = EnableA ? Aout : 8'hzz;
assign bus = EnableB ? Bout : 8'hzz;
assign bus = EnableX ? Cout : 8'hzz;
assign bus = EnableZ ? Dout : 8'hzz;

endmodule

~
~
~
~
~
~
~
~
~
~
~
```

```
npu29.npu.edu - PuTTY

Please refer to release notes for information on supported platforms.

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      Version E-2011.03 -- Wed Oct 12 16:08:11 2016
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The design hasn't changed and need not be recompiled.
If you really want to, delete file simv.daidir/.vcs.timestamp and
run VCS again.

[15035sc@npu29 ~]$ ./simv
Chronologic VCS simulator copyright 1991-2011
Contains Synopsys proprietary information.
Compiler version E-2011.03; Runtime version E-2011.03;  Oct 12 16:08 2016
      V C S   S i m u l a t i o n   R e p o r t
Time: 0
CPU Time:      0.470 seconds;      Data structure size:  0.0Mb
```

7. Retype “trireg” example code and provide the results.


```
npu29.npu.edu - PuTTY
module testtreg();

treg [7:0] data;
reg [1:0] flag;

assign data = (flag==1)? 10:
              (flag==0)? 8'bzz:
              (flag==3)? 30 : 255;

initial begin
    flag = 1;
    #200 flag = 0;
    #200 flag = 3;
    #200 flag = 0;
    #200 flag = 2;
    #200 flag = 0;
    $monitor ("time = %g, data = %d" , $time , data );

    #10 $finish;
end
endmodule
~
"testtreg.v" 21L, 384C 21,1
```

```
npu29.npu.edu - PuTTY
if [ -x ../simv ]; then chmod -x ../simv; fi
g++ -o ../simv -melf_i386 -m32 -Wl,-whole-archive -Wl,-no-whole-archive
vcsobj_1_1.o 5NrI_d.o 5NrIB_d.o SIM_1.o rmapats_mop.o rmapats.o /ee
ols/synopsys/vcs/E-2011.03/linux/lib/libvirsim.so /ee/tools/synopsys/vcs/E-20
03/linux/lib/librterrorinf.so /ee/tools/synopsys/vcs/E-2011.03/linux/lib/libe
malloc.so /ee/tools/synopsys/vcs/E-2011.03/linux/lib/libvcsnew.so /ee/too
synopsys/vcs/E-2011.03/linux/lib/libuclinative.so /ee/tools/synopsys/
/E-2011.03/linux/lib/vcs_save_restore_new.o /ee/tools/synopsys/vcs/E-2011.03/
ux/lib/ctype-stubs_32.a -ldl -lc -lm -lpthread -ldl
../simv up to date
CPU time: .050 seconds to compile + .025 seconds to elab + .121 seconds to li
[15035sc@npu29 ~]$ ./simv
Chronologic VCS simulator copyright 1991-2011
Contains Synopsys proprietary information.
Compiler version E-2011.03; Runtime version E-2011.03; Oct 11 17:35 2016
time = 1000, data = 255
$finish called from file "testtreg.v", line 19.
$finish at simulation time 1010
V C S S i m u l a t i o n R e p o r t
Time: 1010
CPU Time: 0.480 seconds; Data structure size: 0.0Mb
Tue Oct 11 17:35:04 2016
```

8. Retype “testInteger” program and give the results.

```

npu29.npu.edu - PuTTY
module testinteger;

wire pwrGood,pwrOn,pwrStable;

integer i;
time t;
real r;

assign pwrStable = 1'b1;
assign pwrOn = 1'b1;
assign pwrGood = pwrOn & pwrStable;

initial begin
    i = 123.456;
    r = 123456e-3;
    t = 123456e-3;
    $display("i=%0g",i,"t=%6.2f",t,"r=%f",r);
    #2 $display ("TIME = %0d " , $time , " ON = " , pwrOn, "STABLE = " ,pwrStable , "GOOD=" ,pwrGood);
    $finish;
end
endmodule

"testinteger.v" 21L, 405C 18,2 All

```

```

npu29.npu.edu - PuTTY
1 module and 0 UDP read.
recompiling module testinteger because:
    Generated file (INab_1) not found, or not incremental.
if [ -x ../simv ]; then chmod -x ../simv; fi
g++ -o ../simv -melf_i386 -m32 -Wl,-whole-archive -Wl,-no-whole-archive -L
E-2011.03/linux/lib/libvirsim.so /ee/tools/synopsys/vcs/E-2011.03/linux/lib/libr
cs/E-2011.03/linux/lib/libvcsnew.so /ee/tools/synopsys/vcs/E-2011.03/linux/lib/l
ls/synopsys/vcs/E-2011.03/linux/lib/ctype-stubs_32.a -ldl -lc -lm -lpthread -ld
../simv up to date
CPU time: .054 seconds to compile + .026 seconds to elab + .113 seconds to link
[15035sc@npu29 ~]$ ./simv
Chronologic VCS simulator copyright 1991-2011
Contains Synopsys proprietary information.
Compiler version E-2011.03; Runtime version E-2011.03; Oct 11 17:50 2016
i=123t=123.00r=123.456000
TIME = 2 ON = 1STABLE = 1GOOD=1
$finish called from file "testinteger.v", line 19.
$finish at simulation time 2
V C S S i m u l a t i o n R e p o r t
Time: 2
CPU Time: 0.470 seconds; Data structure size: 0.0Mb
Tue Oct 11 17:50:53 2016

```

9. Create a "time" variable type and assign it values from \$stime and \$realtime, what will you get?

```
npu29.npu.edu - PuTTY
This program is proprietary and confidential information of Synopsys Inc.
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Parsing design file 'realtime.v'
Top Level Modules:
    testTime
No TimeScale specified
Starting vcs inline pass...
1 module and 0 UDP read.
recompiling module testTime because:
    Generated file (2Kbv_1) not found, or not incremental.
if [ -x ../simv ]; then chmod -x ../simv; fi
g++ -o ../simv -melf_i386 -m32 -Wl,-whole-archive -Wl,-no-whole-archive _
vcsobj_1_1.o 5NrI_d.o 5NrIB_d.o SIM_1.o rmapats_mop.o rmapats.o /ee/to
ols/synopsys/vcs/E-2011.03/linux/lib/libvirsim.so /ee/tools/synopsys/vcs/E-2011.
03/linux/lib/librterrorinf.so /ee/tools/synopsys/vcs/E-2011.03/linux/lib/libsnps
malloc.so /ee/tools/synopsys/vcs/E-2011.03/linux/lib/libvcsnew.so /ee/tools/
synopsys/vcs/E-2011.03/linux/lib/libuclivariate.so /ee/tools/synopsys/vcs
/E-2011.03/linux/lib/vcs_save_restore_new.o /ee/tools/synopsys/vcs/E-2011.03/lin
ux/lib/ctype-stubs_32.a -ldl -lc -lm -lpthread -ldl
../simv up to date
CPU time: .050 seconds to compile + .041 seconds to elab + .158 seconds to link
[15035sc@npu29 ~]$
```

```
npu29.npu.edu - PuTTY
module testTime;
    time t;
    initial begin
        t = $time;
        #1 t = $time;
        #1 t = $time;
        #2 $finish;
    end
    initial begin
        $monitor ("t=%6.2f", t);
        #2 $display ("TIME =%0d", $time);
    end
endmodule
~
~
~
~
~
~
~
~
~
~
"realtime.v" 15L, 208C 15,1 All
```

```
npu29.npu.edu - PuTTY
ols/synopsys/vcs/E-2011.03/linux/lib/libvirsim.so /ee/tools/synopsys/vcs/E-2011.
03/linux/lib/librterrorinf.so /ee/tools/synopsys/vcs/E-2011.03/linux/lib/libsnps
malloc.so /ee/tools/synopsys/vcs/E-2011.03/linux/lib/libvcsnew.so /ee/tools/
synopsys/vcs/E-2011.03/linux/lib/libuclivative.so /ee/tools/synopsys/vcs
/E-2011.03/linux/lib/vcs_save_restore_new.o /ee/tools/synopsys/vcs/E-2011.03/lin
ux/lib/ctype-stubs_32.a -ldl -lc -lm -lpthread -ldl
../simv up to date
CPU time: .050 seconds to compile + .041 seconds to elab + .158 seconds to link
[15035sc@npu29 ~]$ vi realtime.v
[15035sc@npu29 ~]$ ./simv
Chronologic VCS simulator copyright 1991-2011
Contains Synopsys proprietary information.
Compiler version E-2011.03; Runtime version E-2011.03; Oct 13 19:01 2016
t= 0.00
t= 1.00
TIME =2
t= 2.00
$finish called from file "realtime.v", line 7.
$finish at simulation time 4
V C S S i m u l a t i o n R e p o r t
Time: 4
CPU Time: 0.470 seconds; Data structure size: 0.0Mb
Thu Oct 13 19:01:18 2016
[15035sc@npu29 ~]$
```

10. Define a time scale like `timescale 10ns/100ps, if a delay is #2.71828, calculate the real delay and compare what the difference between \$display result in \$time and your calculation is.

```
npu29.npu.edu - PuTTY
This program is proprietary and confidential information of Synopsys Inc.
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Parsing design file 'timeunit.v'
Top Level Modules:
    sampleDesign
TimeScale is 100 ps / 10 ps
Starting vcs inline pass...
1 module and 0 UDP read.
recompiling module sampleDesign because:
    Compilation options of module have been changed.
if [ -x ../simv ]; then chmod -x ../simv; fi
g++ -o ../simv -melf_i386 -m32 -Wl,-whole-archive -Wl,-no-whole-archive
vcsobj_1_1.o 5NrI_d.o 5NrIB_d.o SIM_1.o rmapats_mop.o rmapats.o /ee/
ols/synopsys/vcs/E-2011.03/linux/lib/libvirsim.so /ee/tools/synopsys/vcs/E-201
03/linux/lib/librterrorinf.so /ee/tools/synopsys/vcs/E-2011.03/linux/lib/libsn
malloc.so /ee/tools/synopsys/vcs/E-2011.03/linux/lib/libvcsnew.so /ee/tool
synopsys/vcs/E-2011.03/linux/lib/libuclivative.so /ee/tools/synopsys/v
/E-2011.03/linux/lib/vcs_save_restore_new.o /ee/tools/synopsys/vcs/E-2011.03/
ux/lib/ctype-stubs_32.a -ldl -lc -lm -lpthread -ldl
../simv up to date
CPU time: .054 seconds to compile + .027 seconds to elab + .128 seconds to lin
```

```
npu29.npu.edu - PuTTY
Starting vcs inline pass...
1 module and 0 UDP read.
recompiling module sampleDesign because:
    Compilation options of module have been changed.
if [ -x ../simv ]; then chmod -x ../simv; fi
g++ -o ../simv -melf_i386 -m32 -Wl,-whole-archive -Wl,-no-whole-arc
vcsobj_1_1.o 5NrI_d.o 5NrIB_d.o SIM_1.o rmapats_mop.o rmapats.o
ols/synopsys/vcs/E-2011.03/linux/lib/libvirsim.so /ee/tools/synopsys/vcs/
03/linux/lib/librterrorinf.so /ee/tools/synopsys/vcs/E-2011.03/linux/lib/
malloc.so /ee/tools/synopsys/vcs/E-2011.03/linux/lib/libvcsnew.so /ee
synopsys/vcs/E-2011.03/linux/lib/libuclivative.so /ee/tools/synop
/E-2011.03/linux/lib/vcs_save_restore_new.o /ee/tools/synopsys/vcs/E-2011
ux/lib/ctype-stubs_32.a -ldl -lc -lm -lpthread -ldl
../simv up to date
CPU time: .054 seconds to compile + .027 seconds to elab + .128 seconds t
[15035sc@npu29 ~]$ ./simv
Chronologic VCS simulator copyright 1991-2011
Contains Synopsys proprietary information.
Compiler version E-2011.03; Runtime version E-2011.03; Oct 12 15:15 2016
VCS Simulation Report
Time: 00 ps
CPU Time: 0.470 seconds; Data structure size: 0.0Mb
Wed Oct 12 15:15:43 2016
```

11. Retype "signedNumber" module, and observe the running results.

```
npu29.npu.edu - PuTTY
module signednumber;

    reg [31:0] a;

    initial begin

        a = 14'h1234;
        $display (" current value of a = %h ", a );
        a = -14'h1234;
        $display (" cuurent value of a = %h ", a );
        a = -32'hDEAD_BEEF;
        $display (" current value of a = %h" ,a );
        a = -32'hDEAD_BEEF;
        $display (" current value of a = %h" , a );
        #10 $finish;

    end
endmodule
~
~
~
~
~
"signednumber.v" 18L, 349C 14,2 All
```

```
npu29.npu.edu - PuTTY
Linux version 'CentOS release 5.11 (Final)' is not supported on 'x86_64'
officially, assuming linux compatibility by default. Set VCS_ARCH_OVERRIDE
to linux or suse32 to override.
Please refer to release notes for information on supported platforms.

Chronologic VCS (TM)
Version E-2011.03 -- Wed Oct 12 14:57:36 2016
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Parsing design file 'signednumber.v'

Error-[UST] Undefined System Task Call
signednumber.v, 10
  Undefined System Task call to '$dispalY'.

1 error
CPU time: .041 seconds to compile
```

12. Take “helloWorld.v” as an example, write program to print double quote, percent character and @ character in ASCII code number.

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Parsing design file 'helloworld.v'

Top Level Modules:

strings

No TimeScale specified

Starting vcs inline pass...

1 module and 0 UDP read.

recompiling module strings because:

Generated file (zrTa_1) not found, or not incremental.

if [-x ../simv]; then chmod -x ../simv; fi

g++ -o ../simv -melf_i386 -m32 -Wl,-whole-archive -Wl,-no-whole-archive
vcsobj_1_1.o 5NrI_d.o 5NrIB_d.o SIM_1.o rmapats_mop.o rmapats.o /ee/t
ols/synopsys/vcs/E-2011.03/linux/lib/libvirsim.so /ee/tools/synopsys/vcs/E-2011
03/linux/lib/librterrorinf.so /ee/tools/synopsys/vcs/E-2011.03/linux/lib/libsnp
malloc.so /ee/tools/synopsys/vcs/E-2011.03/linux/lib/libvcsnew.so /ee/tools
synopsys/vcs/E-2011.03/linux/lib/libuclinative.so /ee/tools/synopsys/vc
/E-2011.03/linux/lib/vcs_save_restore_new.o /ee/tools/synopsys/vcs/E-2011.03/li
ux/lib/ctype-stubs_32.a -ldl -lc -lm -lpthread -ldl

../simv up to date

CPU time: .059 seconds to compile + .046 seconds to elab + .160 seconds to link

[15035sc@npu29 ~]\$

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vcsobj_1_1.o 5NrI_d.o 5NrIB_d.o SIM_1.o rmapats_mop.o rmapats.o /ee/t
ols/synopsys/vcs/E-2011.03/linux/lib/libvirsim.so /ee/tools/synopsys/vcs/E-2011
03/linux/lib/librterrorinf.so /ee/tools/synopsys/vcs/E-2011.03/linux/lib/libsnp
malloc.so /ee/tools/synopsys/vcs/E-2011.03/linux/lib/libvcsnew.so /ee/tools
synopsys/vcs/E-2011.03/linux/lib/libuclinative.so /ee/tools/synopsys/vc
/E-2011.03/linux/lib/vcs_save_restore_new.o /ee/tools/synopsys/vcs/E-2011.03/li
ux/lib/ctype-stubs_32.a -ldl -lc -lm -lpthread -ldl

../simv up to date

CPU time: .059 seconds to compile + .046 seconds to elab + .160 seconds to link

[15035sc@npu29 ~]\$./simv

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Compiler version E-2011.03; Runtime version E-2011.03; Oct 13 19:10 2016

this is sample string

V C S S i m u l a t i o n R e p o r t

Time: 0

CPU Time: 0.490 seconds; Data structure size: 0.0Mb

Thu Oct 13 19:10:58 2016

[15035sc@npu29 ~]\$



The image shows a PuTTY terminal window with the title bar 'npu29.npu.edu - PuTTY'. The terminal displays Verilog code for a module named 'variables'. The code defines several variables: an integer 'i', a time variable 't', a string 'string', and two 32-bit registers 'a' and 'b'. It assigns values to these variables: 'i' is 123, 't' is 123446e-3, 'a' is the hexadecimal value 14'h1234, and 'b' is 0.5. The code includes an 'initial' block that uses '\$display' to print the values of 'i', 't', 'string', 'a' (in hex), and 'b' (in decimal). The code ends with 'end' and 'endmodule'. At the bottom of the terminal, there is a status bar with the text '-- INSERT --', the coordinates '9,2', and the text 'All'.

```
module variables();

    integer i;
    time t;
    reg [8*21:0] string;
    reg [31:0] a;
    reg [31:0] b;

    i = 123;
    t = 123446e-3;
    a = 14'h1234;
    b = 0.5;
    initial begin

        string = "This is sample string";
        $display ("i = %0g\n" ,i);
        $display ("t = %6.2f",t);
        $display ("%s \n" , string );
        $display (" hexa = %h" ,a);
        $display (" deci = %d" ,b);

    end
endmodule
-- INSERT --
```

9,2 All

14. Compare \$display, \$write and \$monitor system tasks by a program, and give the running result

