Northwestern Polytechnic University

EE461 Lab Verilog-HDL

Lab Assignment #2

Due day: 10/18/2016

Instruction:

1. Print your program for each question in "word" file and paste running results in screen shot on it. Printing results or electrical copies from monitor can't be accepted.
2. Please follow the code style rule like programs on handout.
3. Overdue homework submission could not be accepted.
4. Takes academic honesty and integrity seriously (Zero Tolerance of Cheating & Plagiarism)

1. If a = 4'b1111 and b = -5'b00010, write the program to check what the values with 4 bits are when you want to calculate "a (+/-/*/%) b". How about b = -5'b01xz ?

2. When a = 2'b1z and b = 3'b11z, verify the values for (a>b), (a>=b), (a<b) and (a<=b) by a program. If a = 4'b01xz, check again.

3. Write a program to see results for 4 questions on "Equality Operators" page in the handout.

4. Verify the results by a program for the following "A's values".

A	!A
1'bx	
1'bz	
2'b1z	
2'b0z	
2'bxz	
3'bxxx	
3'b1xx	
3'b0xx	

5. Write a program to see what you will get for 1'bx && 2'bxz , 2'b0x || 1'bz , 2'b00 && 2'b1z and 2'b0z || 4'b01xz.

6. What are the results in the following operations and verify them by Verilog code?

~4'b01xz = ?
4'b01xz & 4'bzx01 = ?
4'b01xz | 4'bzx01 = ?
4'b01xz ^ 4'bzx01 = ?
4'b01xz ^~ 4'bzx01 = ?
4'b01xz ^~ 2'bz1 = 4'b?
4'b01xz ^~ 2'bz1 = 2'b?

7. What are you going to get for “& 4’b01xz” , “~| 4’b01xz” , “^ 4’b01xz” and “~^ 4’b01xz”.

8. What are the new values after bit shifting for “4'b01xz << 1'bz” and “4'b01xz >>2'bxx” ?

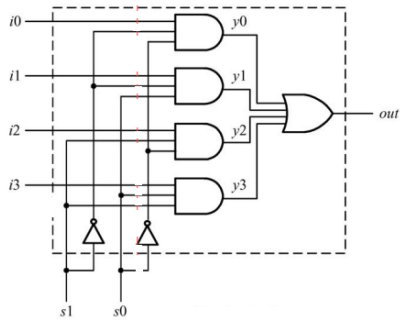
9. In this expression A = B ? 4’b1100 : 5’b11ZX0 and if B = 2’b1x, What is A(4-bit number)? How about B= 3’b1xz? Write a program to verify your answers.

10. Complete the following Verilog modules and display the output strength. Explain why.

```
module testStrength1();
        ... ...                 // Data type declaration for a, b and y
        buf (strong1, weak0) g1 (y, a)
        buf (weak1, strong0) g2 (y, b);

        initial begin
                a = 1;
                b = 1;
                $display(“y = ..., a =... , b = ...”, y, a, b);
        end
endmodule
module testStrength2();
        ... ...                 // Data type declaration for a, b and y
        bufif0 (strong1, weak0) g1 (y, i1, ctrl);
        bufif0 (strong1, weak0) g2 (y, i2, ctrl);
        initial begin
                ctrl = x;
                i1 = 0;
                i1 = 1;
                $display(“y = ...”);
        end
endmodule
```

11. Design Verilog program for 4 to 1 mux in gate level and write the testbench to verify.



```
module fourOneMux(
                        i0_i,
                        i1_i,
                        i2_i,
                        i3_i,
                        s0_i,
                        s1_i,
                        out_o
);
            ... ... ;
endmodule

`include "foutOneMux"
module fourOneMuxTB;
            ... ... ;
endmodule
```

Note: please save two modules in two different files with the same name as module under the one directory.

12. Write nor gate verilog module using switch devices and testbench to verify it.