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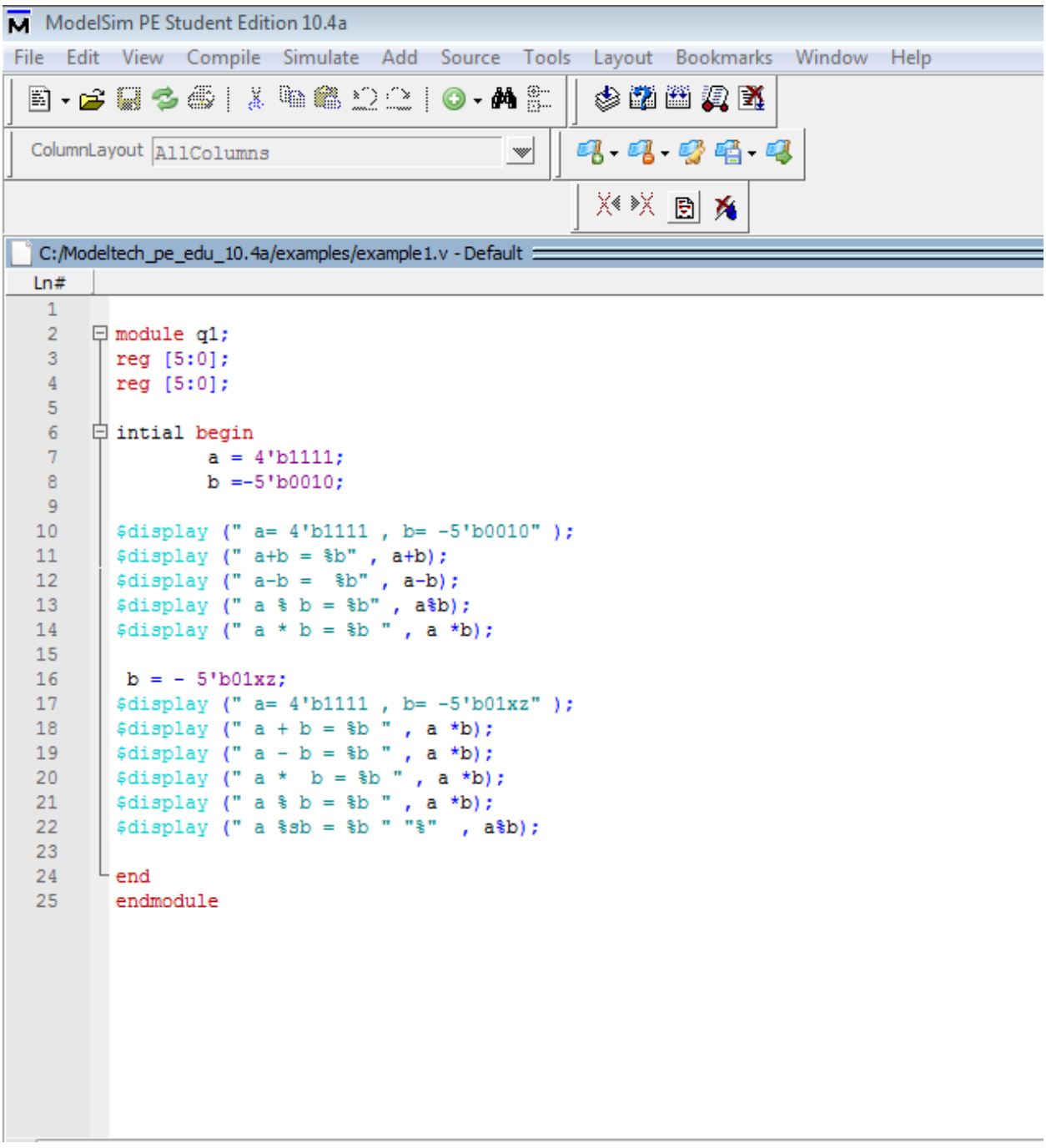
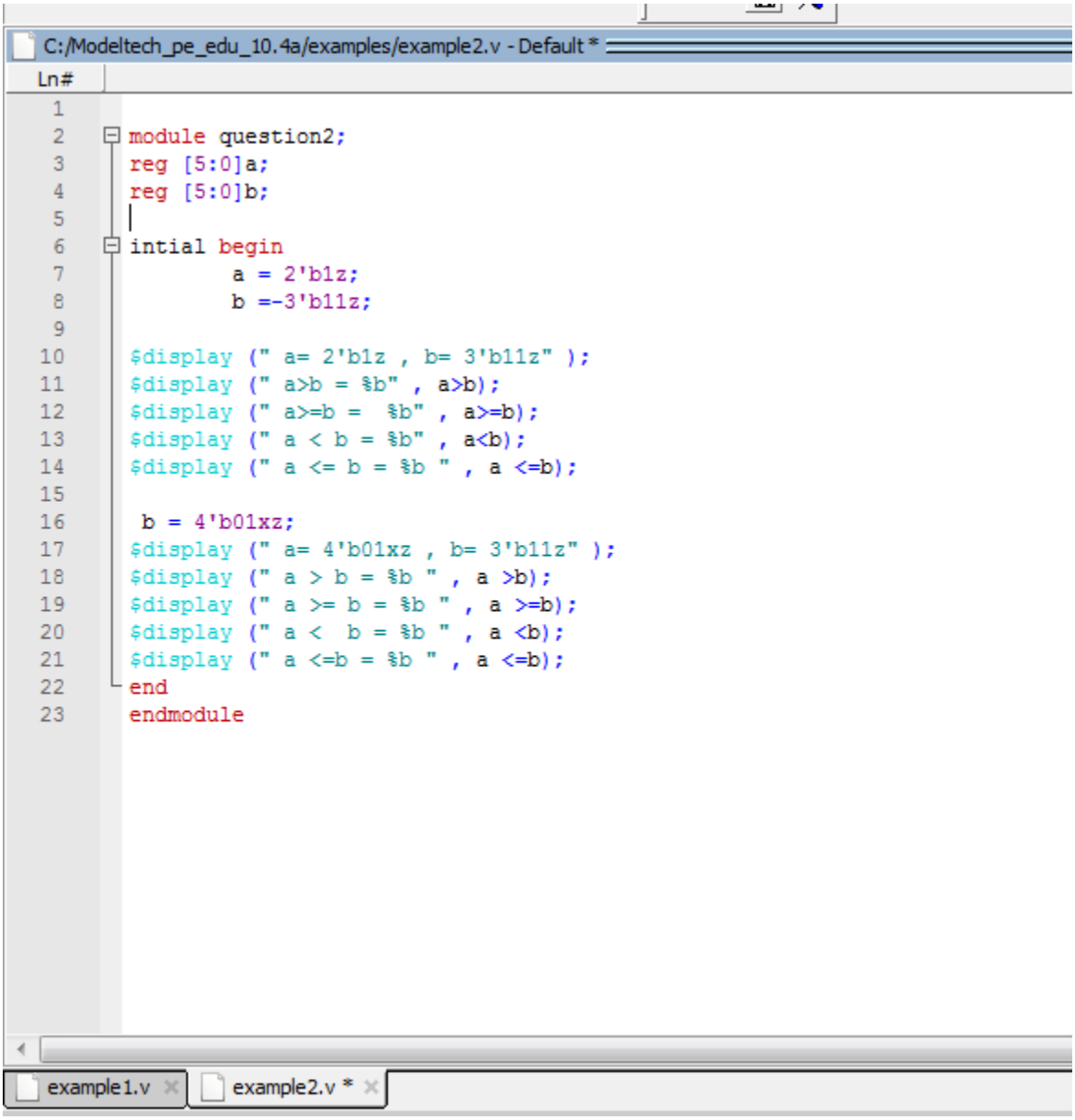
Lab assignment 2

Answers 1



```
module q1;

reg [5:0];

reg [5:0];


intial begin

            a = 4'b1111;

       b =-5'b0010;


$display (" a= 4'b1111 , b= -5'b0010" );

$display (" a+b = %b" , a+b);

$display (" a-b =  %b" , a-b);

$display (" a % b = %b" , a%b);

$display (" a * b = %b " , a *b);


 b = - 5'b01xz;

$display (" a= 4'b1111 , b= -5'b01xz" );

$display (" a + b = %b " , a *b);

$display (" a - b = %b " , a *b);

$display (" a *  b = %b " , a *b);

$display (" a % b = %b " , a *b);

$display (" a %sb = %b " "%"  , a%b);


end

endmodule
```

Answer 2



module question2;

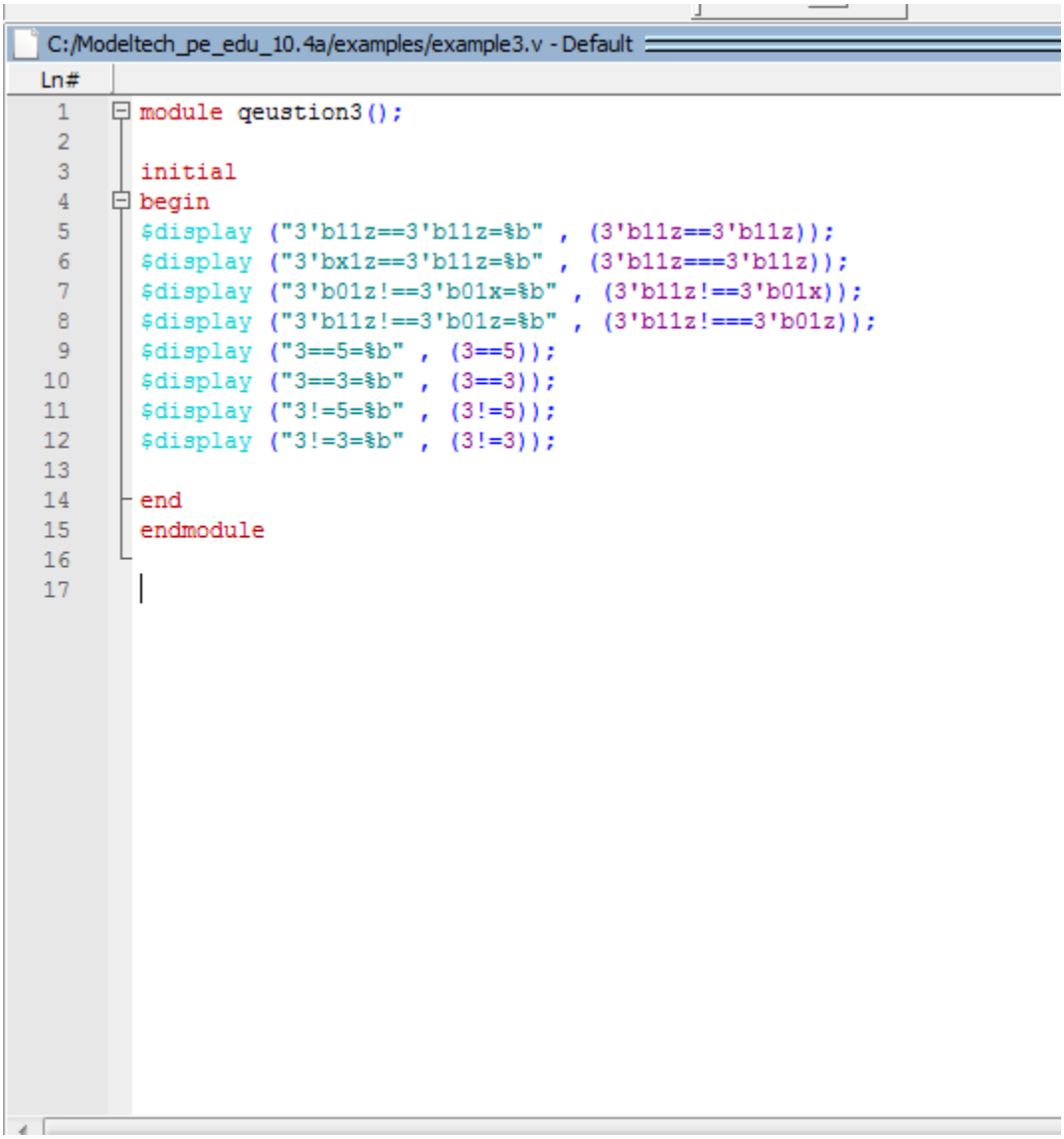
reg [5:0]a;

reg [5:0]b;

intial begin

```
        a = 2'b1z;
    b =-3'b11z;

$display (" a= 2'b1z , b= 3'b11z" );
$display (" a>b = %b" , a>b);
$display (" a>=b =  %b" , a>=b);
$display (" a < b = %b" , a<b);
$display (" a <= b = %b " , a <=b);

 b = 4'b01xz;
$display (" a= 4'b01xz , b= 3'b11z" );
$display (" a > b = %b " , a >b);
$display (" a >= b = %b " , a >=b);
$display (" a <  b = %b " , a <b);
$display (" a <=b = %b " , a <=b);
end
endmodule
```

Answers 3



module qeustion3();

initial

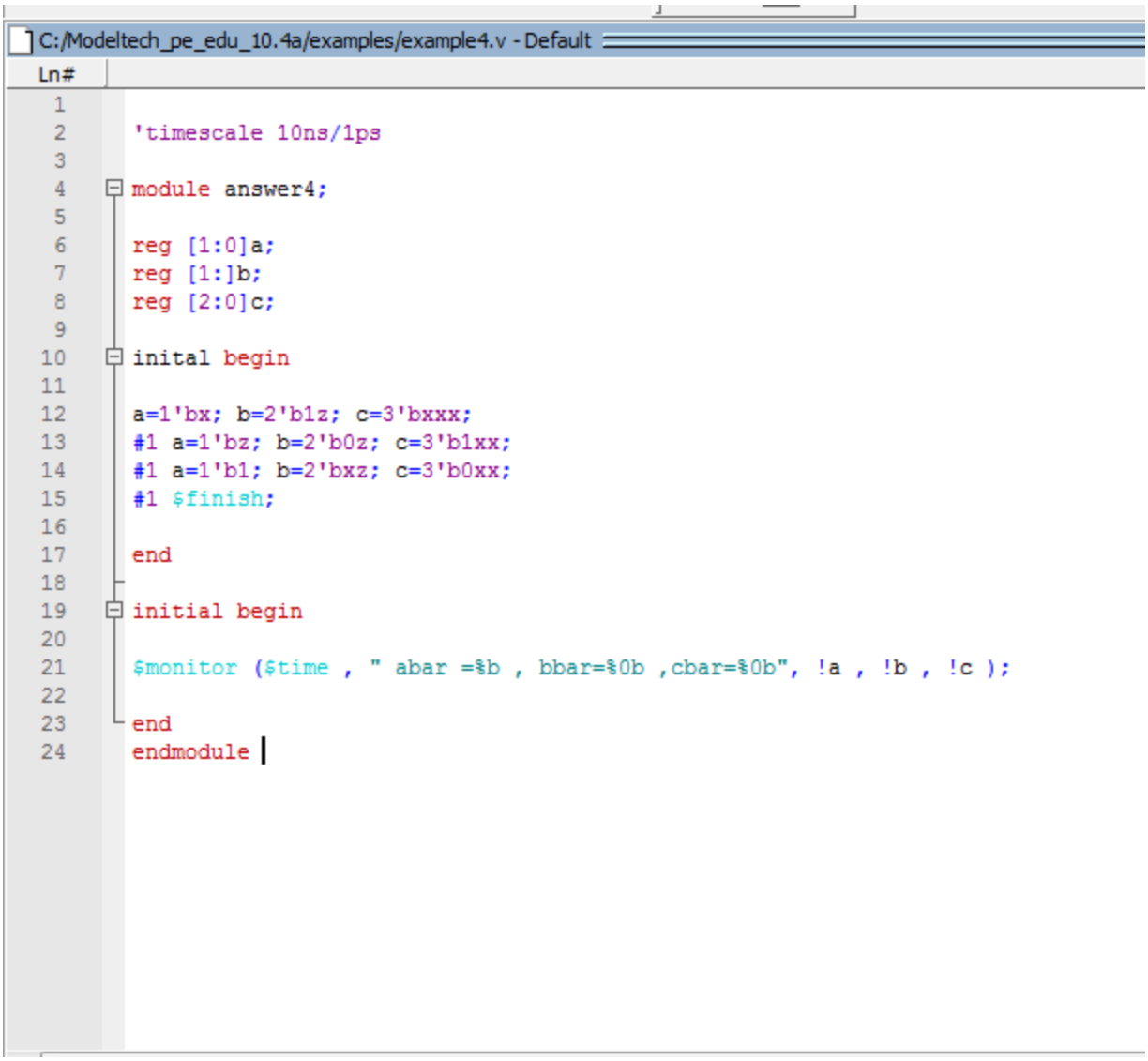
begin

$display ("3'b11z==3'b11z=%b" , (3'b11z==3'b11z));

$display ("3'bx1z==3'b11z=%b" , (3'b11z===3'b11z));

```
$display ("3'b01z!==3'b01x=%b" , (3'b11z!==3'b01x));

$display ("3'b11z!==3'b01z=%b" , (3'b11z!===3'b01z));

$display ("3==5=%b" , (3==5));

$display ("3==3=%b" , (3==3));

$display ("3!=5=%b" , (3!=5));

$display ("3!=3=%b" , (3!=3));


end

endmodule
```

example 4



'timescale 10ns/1ps

module answer4;

reg [1:0]a;

reg [1:]b;

reg [2:0]c;

```
inital begin

a=1'bx; b=2'b1z; c=3'bxxx;
#1 a=1'bz; b=2'b0z; c=3'b1xx;
#1 a=1'b1; b=2'bxz; c=3'b0xx;
#1 $finish;

end

initial begin

$monitor ($time , " abar =%b , bbar=%0b ,cbar=%0b", !a , !b , !c );

end
endmodule
```

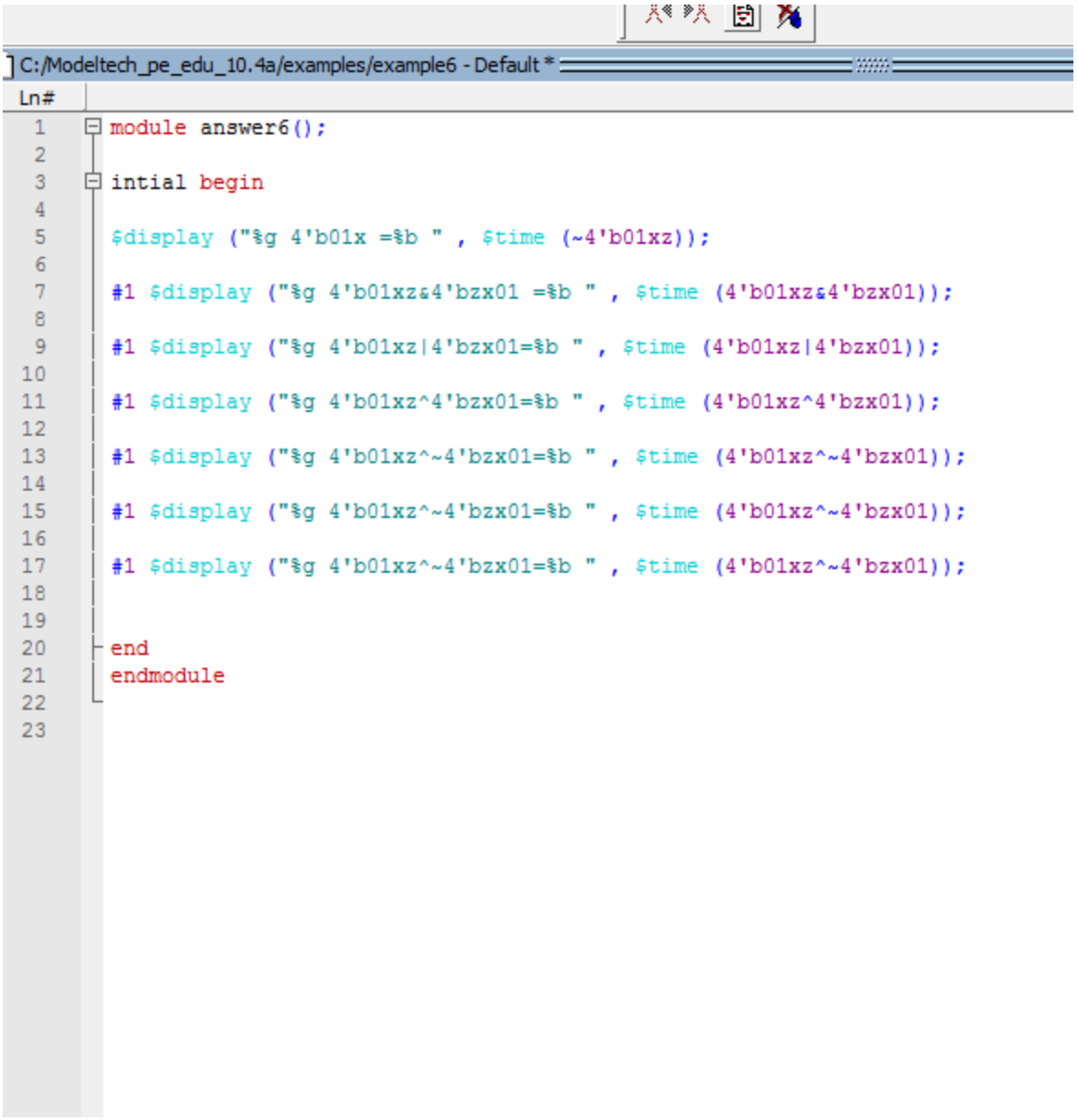
example 5

C:/Modeltech_pe_edu_10.4a/examples/example5.v - Default

```
Ln#
 1  module answer5();
 2
 3  intial begin
 4
 5  $display ("%g 1'bx&&2'bxz =%b " , $time (1'bx&&2'bxz));
 6
 7  #1 $display ("%g 2'b0x||2'bxz =%b " , $time (2'b0x||1'b1z));
 8
 9  #1 $display ("%g 2'b001&&2'b1z=%b " , $time (2'b001&&2'b1z));
10
11  #1 $display ("%g 2'b001&&2'b1z =%b " , $time (2'b001&&2'b1z));
12
13  #1 $display ("%g 2'b0z|| 4'b01xz =%b " , $time (2'b0z|| 4'b01xz));
14
15  end
16  endmodule
17
18
19
20
21
22
```

```
module answer5();

intial begin

$display ("%g 1'bx&&2'bxz =%b " , $time (1'bx&&2'bxz));

#1 $display ("%g 2'b0x||2'bxz =%b " , $time (2'b0x||1'b1z));

#1 $display ("%g 2'b001&&2'b1z=%b " , $time (2'b001&&2'b1z));

#1 $display ("%g 2'b001&&2'b1z =%b " , $time (2'b001&&2'b1z));

#1 $display ("%g 2'b0z|| 4'b01xz =%b " , $time (2'b0z|| 4'b01xz));

end

endmodule
```

answer 6



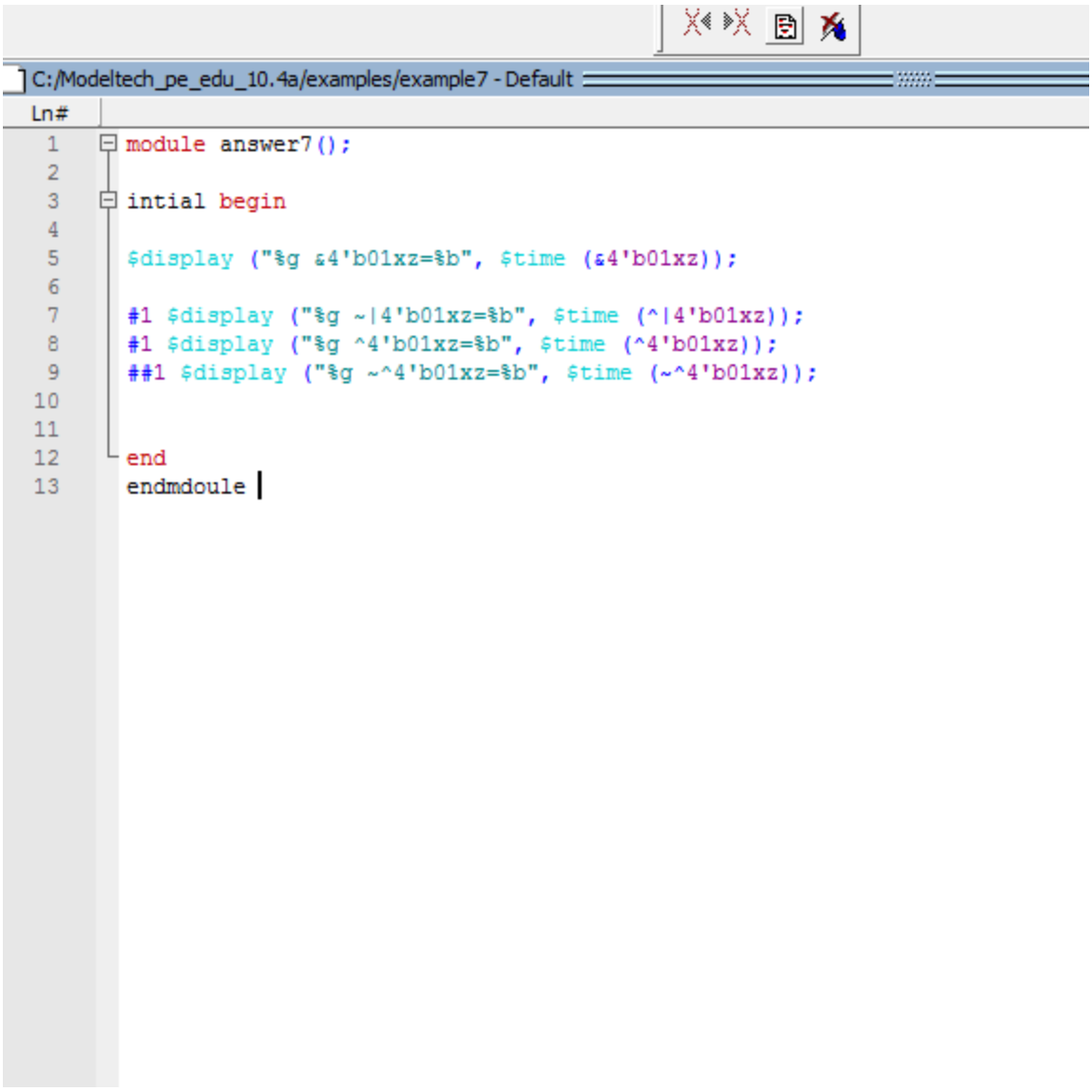
module answer6();

intial begin

$display ("%g 4'b01x =%b " , $time (~4'b01xz));

```
#1 $display ("%g 4'b01xz&4'bzx01 =%b " , $time (4'b01xz&4'bzx01));

#1 $display ("%g 4'b01xz|4'bzx01=%b " , $time (4'b01xz|4'bzx01));

#1 $display ("%g 4'b01xz^4'bzx01=%b " , $time (4'b01xz^4'bzx01));

#1 $display ("%g 4'b01xz^~4'bzx01=%b " , $time (4'b01xz^~4'bzx01));

#1 $display ("%g 4'b01xz^~4'bzx01=%b " , $time (4'b01xz^~4'bzx01));

#1 $display ("%g 4'b01xz^~4'bzx01=%b " , $time (4'b01xz^~4'bzx01));



end

endmodule
```

answer 7


C:/Modeltech_pe_edu_10.4a/examples/example7 - Default
Ln#
1 module answer7();
2
3 intial begin
4
5 $display ("%g &4'b01xz=%b", $time (&4'b01xz));
6
7 #1 $display ("%g ~|4'b01xz=%b", $time (^|4'b01xz));
8 #1 $display ("%g ^4'b01xz=%b", $time (^4'b01xz));
9 ##1 $display ("%g ~^4'b01xz=%b", $time (~^4'b01xz));
10
11
12 end
13 endmdoule

module answer7();

intial begin

$display ("%g &4'b01xz=%b", $time (&4'b01xz));

#1 $display ("%g ~|4'b01xz=%b", $time (^|4'b01xz));

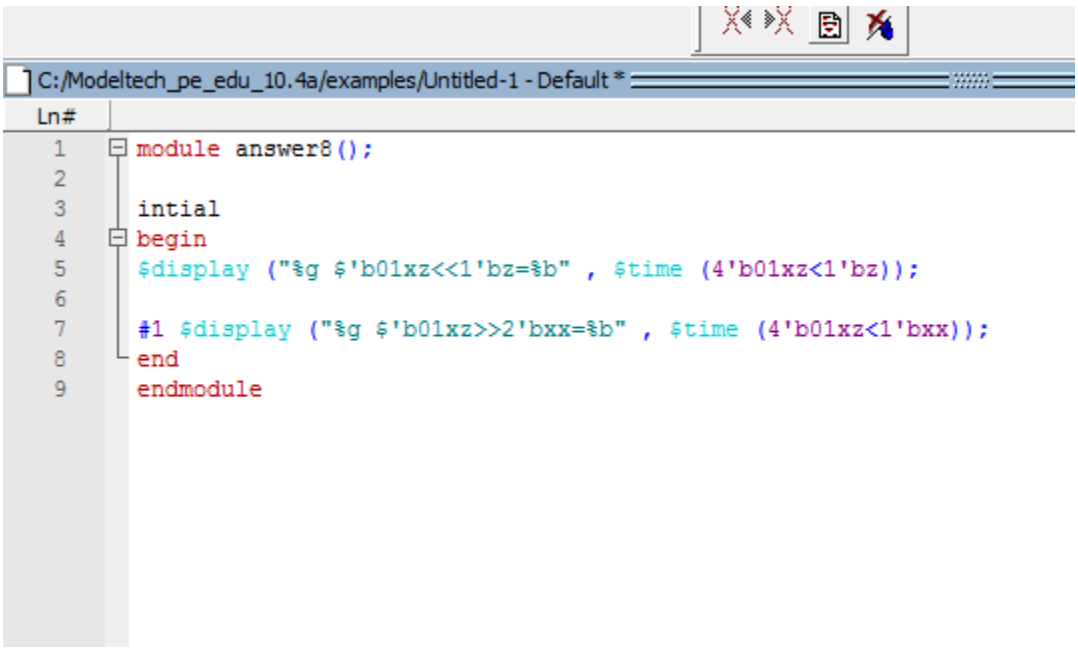
#1 $display ("%g ^4'b01xz=%b", $time (^4'b01xz));

##1 $display ("%g ~^4'b01xz=%b", $time (~^4'b01xz));

end

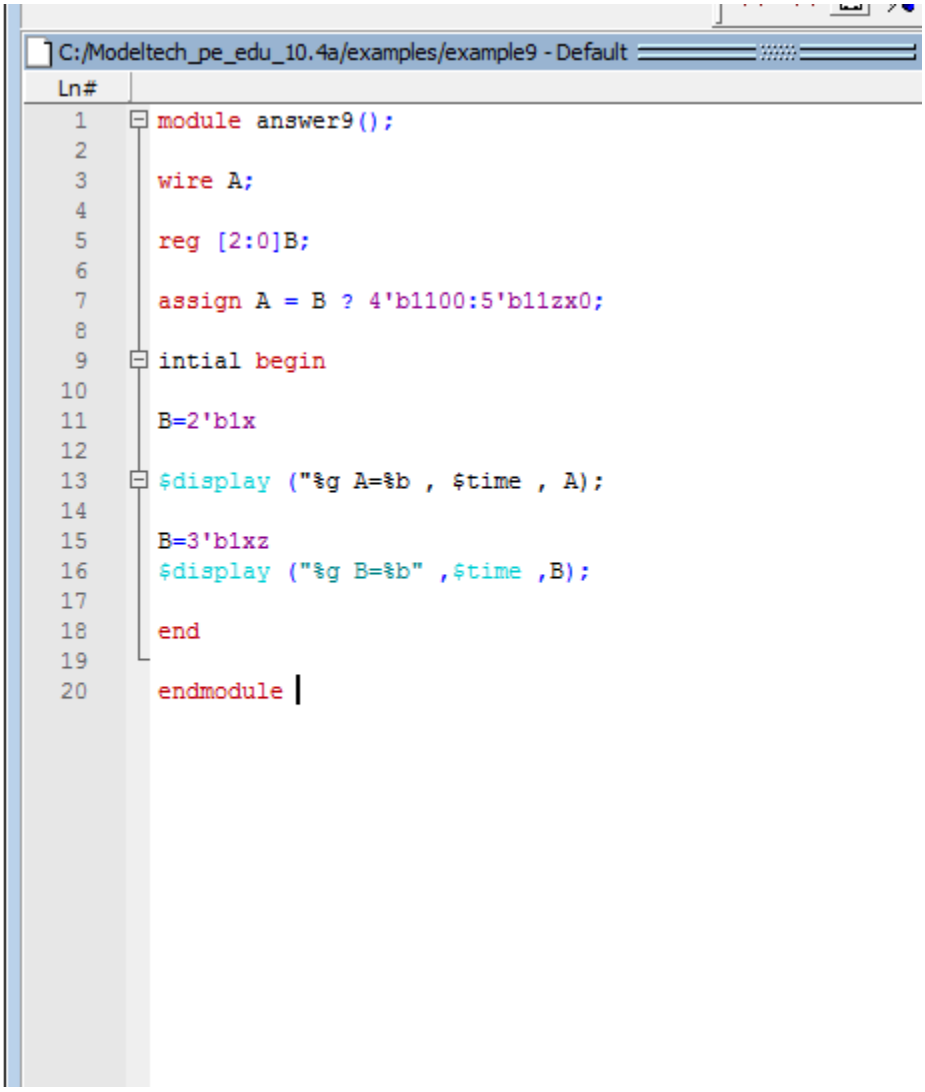
endmdoule

answer 8



```
module answer8();


intial

begin

$display ("%g $'b01xz<<1'bz=%b" , $time (4'b01xz<1'bz));


#1 $display ("%g $'b01xz>>2'bxx=%b" , $time (4'b01xz<1'bxx));

end

endmodule
```

example 9



module answer9();

wire A;

reg [2:0]B;

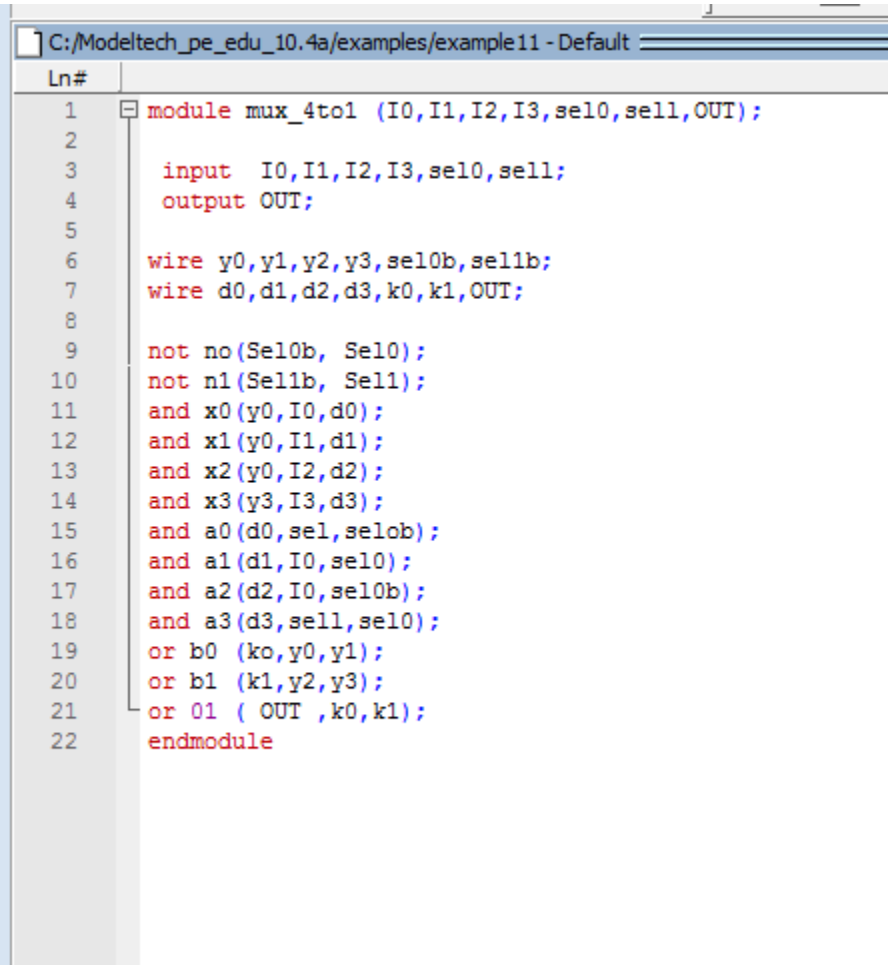
```
assign A = B ? 4'b1100:5'b11zx0;

intial begin

B=2'b1x

$display ("%g A=%b , $time , A);

B=3'b1xz

$display ("%g B=%b" ,$time ,B);

end

endmodule
```

example 10

C:/Modeltech_pe_edu_10.4a/examples/example10 - Default

```
Ln#
 1  `timescale 10ns/100ps
 2
 3  module teststrength1();
 4
 5  reg A,B;
 6  wire X;
 7
 8  buf (strong1,weak0) g1(X,A);
 9  buf ( weak1,strong0) g2 (X,B);
10
11  intial
12   begin
13
14   A=1;
15   B=1;
16
17  $display (" X = %b ,A = %b ,B = %b " , X,A,B);
18
19  end
20  endmodule
21
22  module teststrength2();
23
24  reg i1,i2,ctrl;
25  wire X;
26
27  bufif0 (strong1,weak0) g1 (X,il,ctrl);
28  bufifo (strong1, weak0) g2 (X,i2,ctrl);
29
30  intial
31  begin
32    ctrl=1;
33  il=0;
34  il=1;
35  $display (" X =%b , il =%b ,ctrk =%b,ctrl=%b" , x,i1,i2,ctrl);
36
37  end
38  endmodule
39
```

Example 11



module mux_4to1 (I0,I1,I2,I3,sel0,sell,OUT);

input I0,I1,I2,I3,sel0,sell;

output OUT;

wire y0,y1,y2,y3,sel0b,sel1b;

wire d0,d1,d2,d3,k0,k1,OUT;

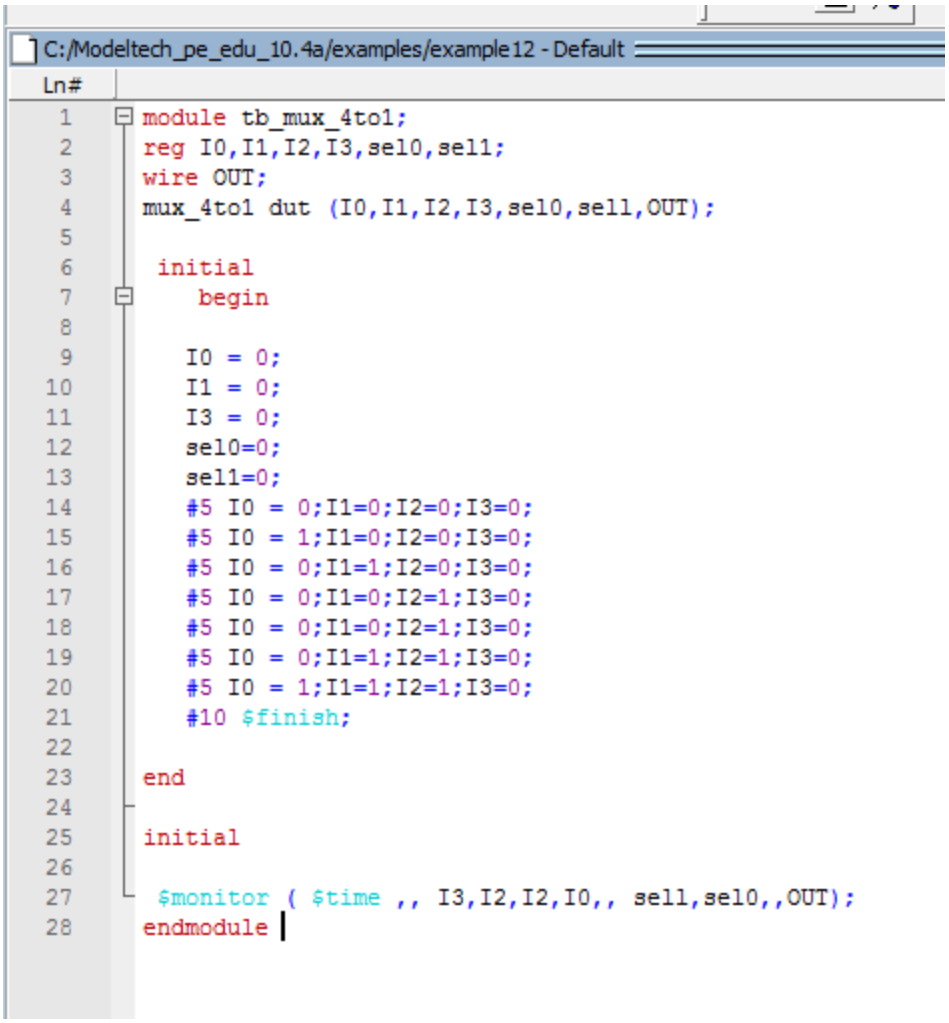
```
not no(Sel0b, Sel0);
not n1(Sel1b, Sel1);
and x0(y0,I0,d0);
and x1(y0,I1,d1);
and x2(y0,I2,d2);
and x3(y3,I3,d3);
and a0(d0,sel,selob);
and a1(d1,I0,sel0);
and a2(d2,I0,sel0b);
and a3(d3,sell,sel0);
or b0 (ko,y0,y1);
or b1 (k1,y2,y3);
or 01 ( OUT ,k0,k1);
endmodule
```

```
`timescale 10ns/100ps

module teststrength1();
```

```
reg A,B;
wire X;

buf (strong1,weak0) g1(X,A);
buf ( weak1,strong0) g2 (X,B);

intial
 begin

 A=1;
 B=1;

$display (" X = %b ,A = %b ,B = %b " , X,A,B);

end
endmodule

module teststrength2();

reg i1,i2,ctrl;
wire X;

bufif0 (strong1,weak0) g1 (X,il,ctrl);
bufifo (strong1, weak0) g2 (X,i2,ctrl);
```

```
intial
begin
  ctrl=1;
il=0;
il=1;
$display (" X =%b , iI =%b ,ctrk =%b,ctrl=%b" , x,i1,i2,ctrl);

end
endmodule
```

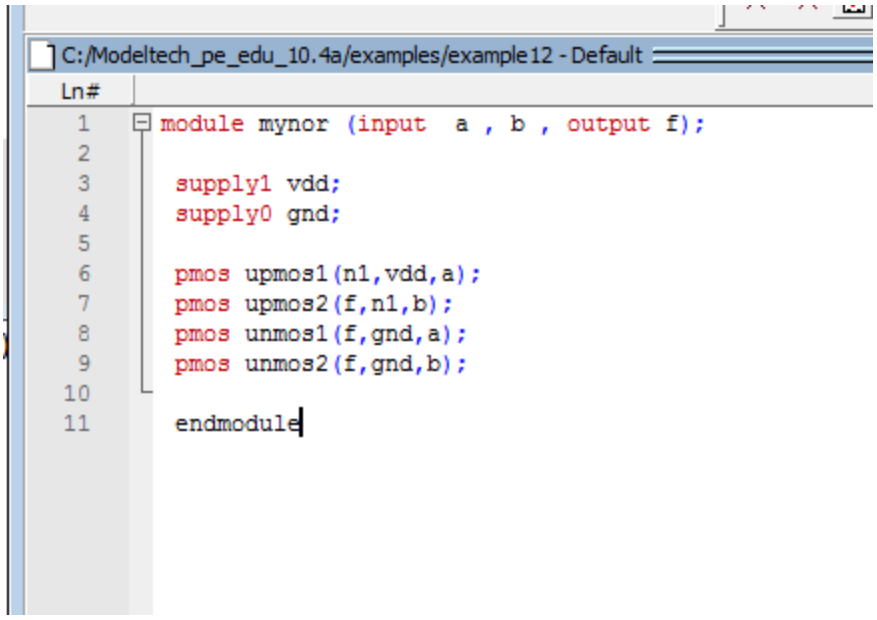
example 12




```
module tb_mux_4to1;
reg I0,I1,I2,I3,sel0,sel1;
wire OUT;
mux_4to1 dut (I0,I1,I2,I3,sel0,sell,OUT);

 initial
   begin

  I0 = 0;
```

```
  I1 = 0;
  I3 = 0;
  sel0=0;
  sel1=0;
  #5 I0 = 0;I1=0;I2=0;I3=0;
  #5 I0 = 1;I1=0;I2=0;I3=0;
  #5 I0 = 0;I1=1;I2=0;I3=0;
  #5 I0 = 0;I1=0;I2=1;I3=0;
  #5 I0 = 0;I1=0;I2=1;I3=0;
  #5 I0 = 0;I1=1;I2=1;I3=0;
  #5 I0 = 1;I1=1;I2=1;I3=0;
  #10 $finish;

end

initial

 $monitor ( $time ,, I3,I2,I2,I0,, sell,sel0,,OUT);
endmodule
```

example 12




```
module mynor (input  a , b , output f);


 supply1 vdd;

 supply0 gnd;


 pmos upmos1(n1,vdd,a);

 pmos upmos2(f,n1,b);

 pmos unmos1(f,gnd,a);

 pmos unmos2(f,gnd,b);


 endmodule
```

test batch :

```
n#
1   `include "answer12.v"
2
3   module test_12();
4
5   reg a_r, b_r;
6
7   wire f_w;
8
9   mynor dut {
10
11              .a(a_r),
12              .b(b_r),
13              .f(f_w)
14
15  );
16
17  initial begin
18
19          a_r=1'b0; b_r=1'b0;
20  #1      a_r=1'b0;b_r =1'b1;
21  #1      a_r=1'b1;b_r =1'b1;
22  #1      a_r=1'b1;b_r =1'b1;
23  #1      $finish;
24
25  end
26  initial begin
27
28      $monitor ("a=%0b,b=%0b,f_w=%0b", a_r,b_r,f_w);
29
30  end
31  endmodule \
```

`include "answer12.v"

module test_12();

reg a_r, b_r;

wire f_w;

mynor dut {

```
        .a(a_r),
        .b(b_r),
        .f(f_w)

);

 initial begin

     a_r=1'b0; b_r=1'b0;
 #1   a_r=1'b0;b_r =1'b1;
 #1   a_r=1'b1;b_r =1'b1;
 #1   a_r=1'b1;b_r =1'b1;
 #1   $finish;

end
initial begin

  $monitor ("a=%0b,b=%0b,f_w=%0b", a_r,b_r,f_w);

end
endmodule \
```