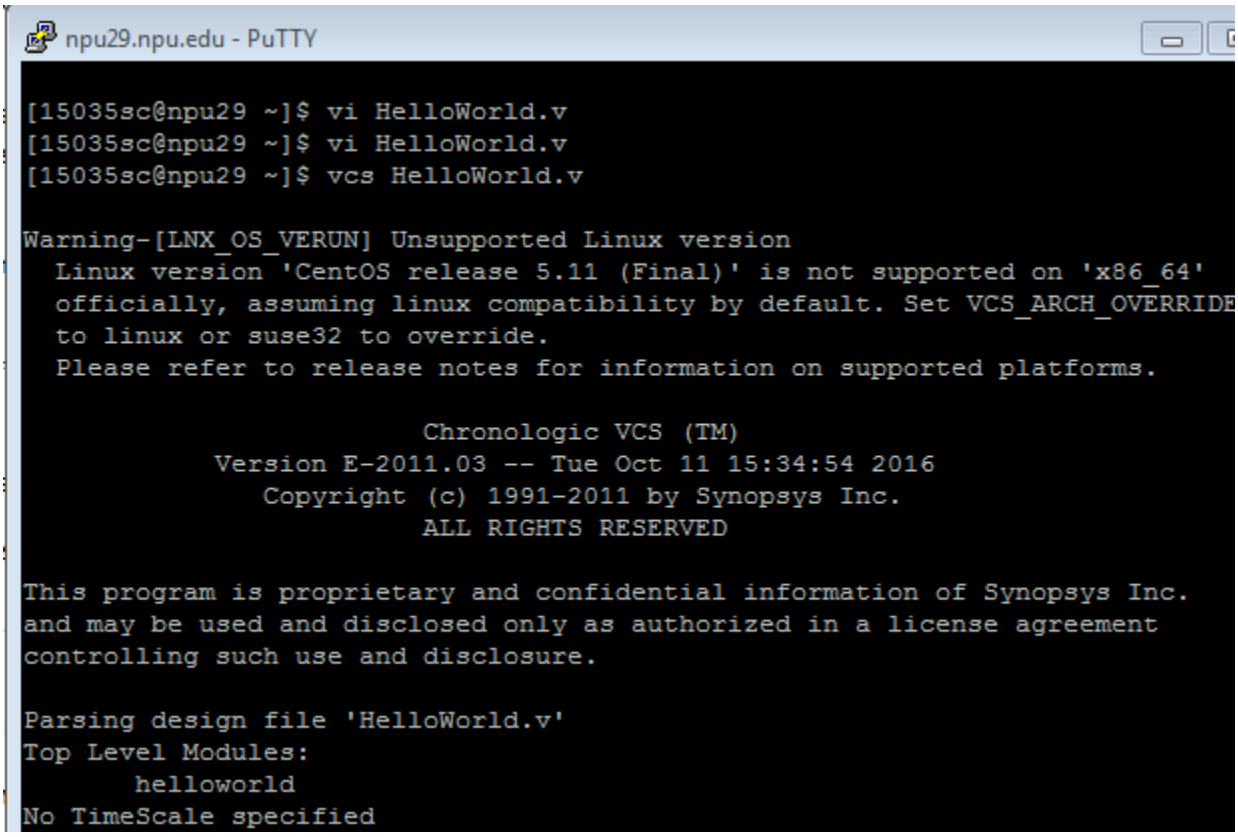
Chiragkumar solanki

15035

1. Write the program to verify whether white space “Carriage Return” and “Formfeed” in “helloWorld.v” work or not, and show the result.



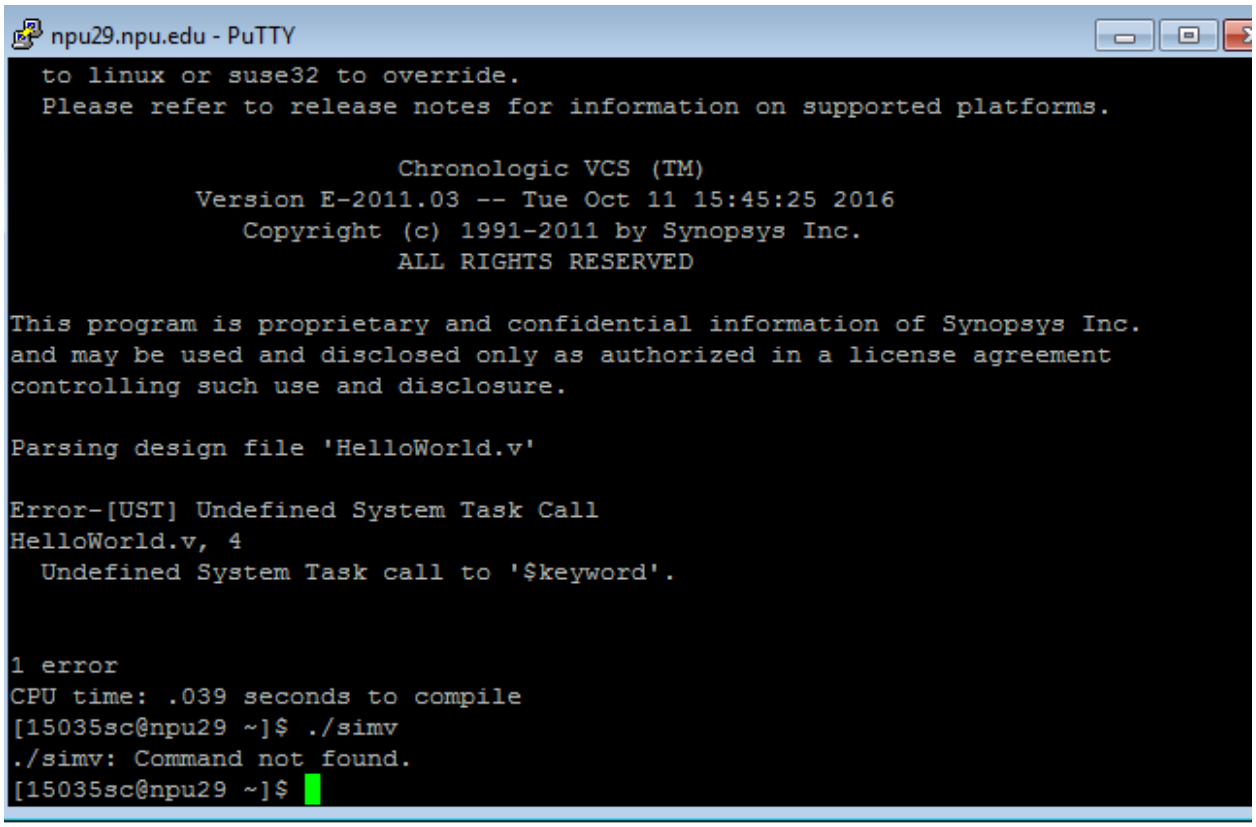
```
This program is proprietary and confidential information of Synopsys Inc.
and may be used and disclosed only as authorized in a license agreement
controlling such use and disclosure.

Parsing design file 'HelloWorld.v'
Top Level Modules:
       helloworld
No TimeScale specified
Starting vcs inline pass...
1 module and 0 UDP read.
recompiling module helloworld because:
        This module or some inlined child module(s) has/have been modified.
if [ -x ../simv ]; then chmod -x ../simv; fi
g++  -o ../simv -melf_i386 -m32   -Wl,-whole-archive    -Wl,-no-whole-archive
vcsobj_1_1.o  5NrI_d.o 5NrIB_d.o SIM_1.o     rmapats_mop.o rmapats.o      /ee/t
ols/synopsys/vcs/E-2011.03/linux/lib/libvirsim.so /ee/tools/synopsys/vcs/E-2011
03/linux/lib/librterrorinf.so /ee/tools/synopsys/vcs/E-2011.03/linux/lib/libsnp
malloc.so     /ee/tools/synopsys/vcs/E-2011.03/linux/lib/libvcsnew.so /ee/tools
synopsys/vcs/E-2011.03/linux/lib/libuclinative.so         /ee/tools/synopsys/vc
/E-2011.03/linux/lib/vcs_save_restore_new.o /ee/tools/synopsys/vcs/E-2011.03/li
```

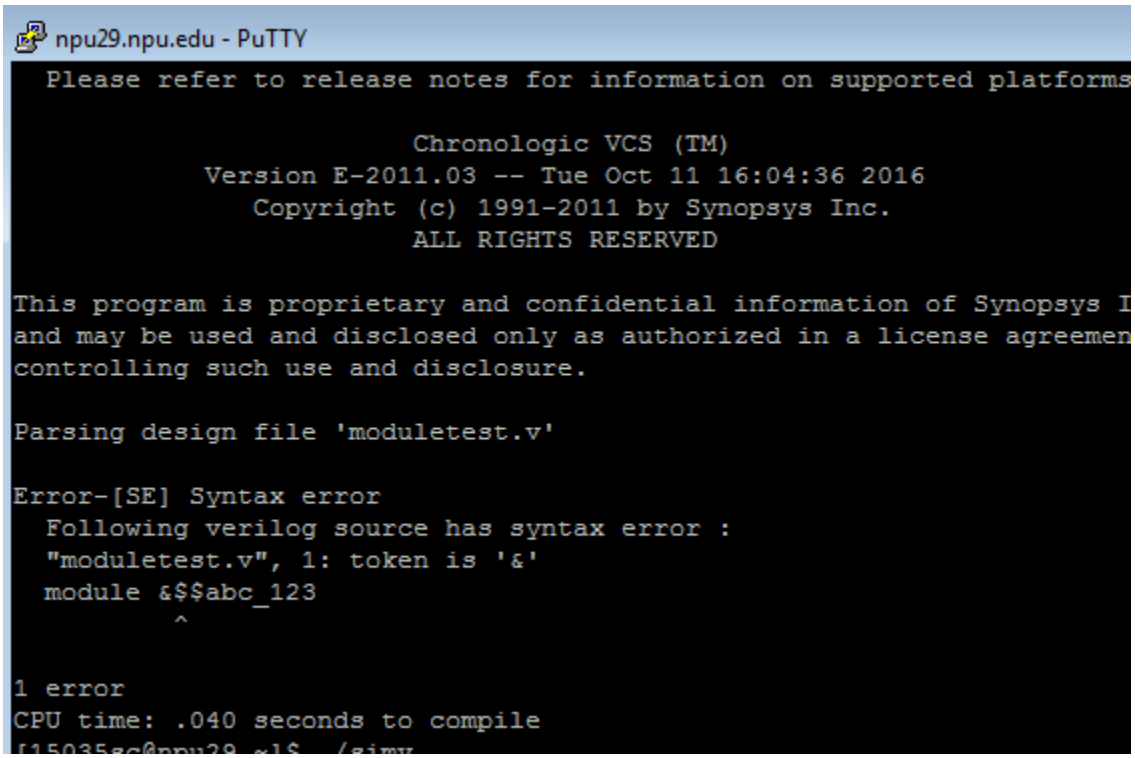
```
[15035sc@npu29 ~]$ ./simv
Chronologic VCS simulator copyright 1991-2011
Contains Synopsys proprietary information.
Compiler version E-2011.03; Runtime version E-2011.03;  Oct 11 15:40 20
hello world
          V C S   S i m u l a t i o n   R e p o r t
Time: 0
CPU Time:      0.480 seconds;       Data structure size:   0.0Mb
Tue Oct 11 15:40:35 2016
```

```
[15035sc@npu29 ~]$ ./simv
Chronologic VCS simulator copyright 1991-2011
Contains Synopsys proprietary information.
Compiler version E-2011.03; Runtime version E-2011.03;  Oct 11 15:42 2016
 Carriage return formfeed
          V C S   S i m u l a t i o n   R e p o r t
Time: 0
CPU Time:      0.470 seconds;       Data structure size:   0.0Mb
Tue Oct 11 15:42:56 2016
[15035sc@npu29 ~]$
```

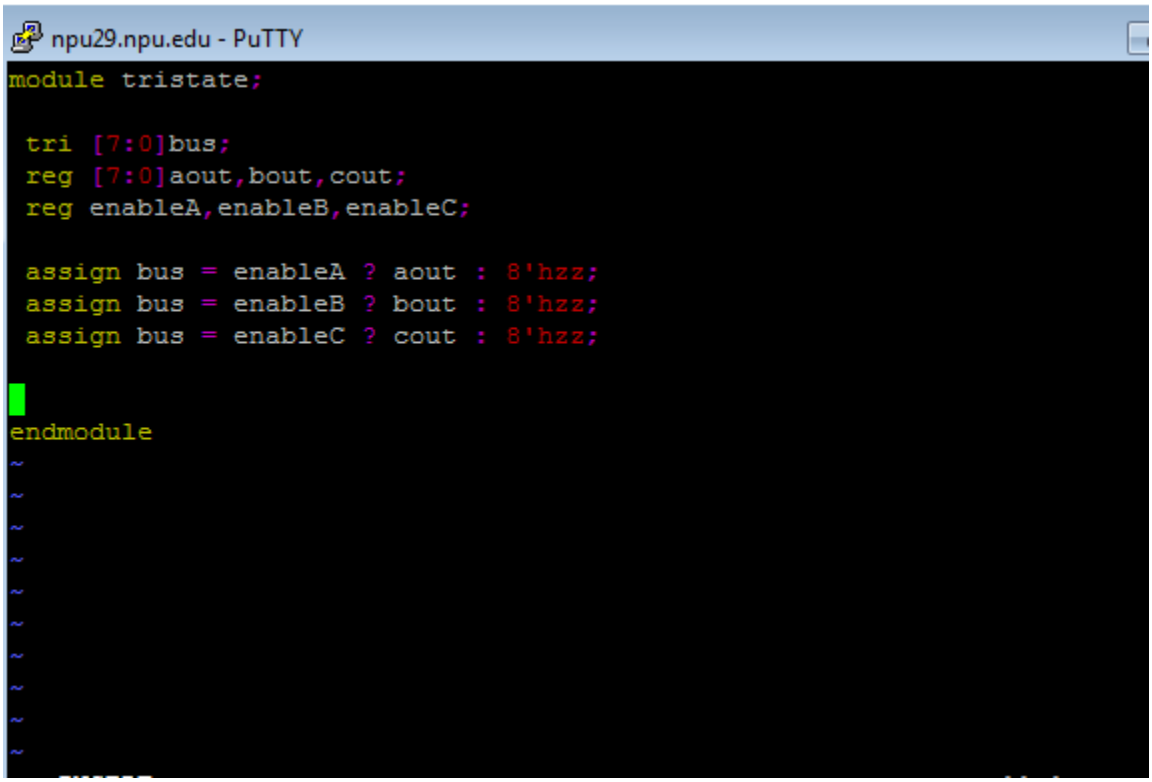
2. If a variable name is defined using a keyword, write a code snippet to look at what will happen and show error/warning information.

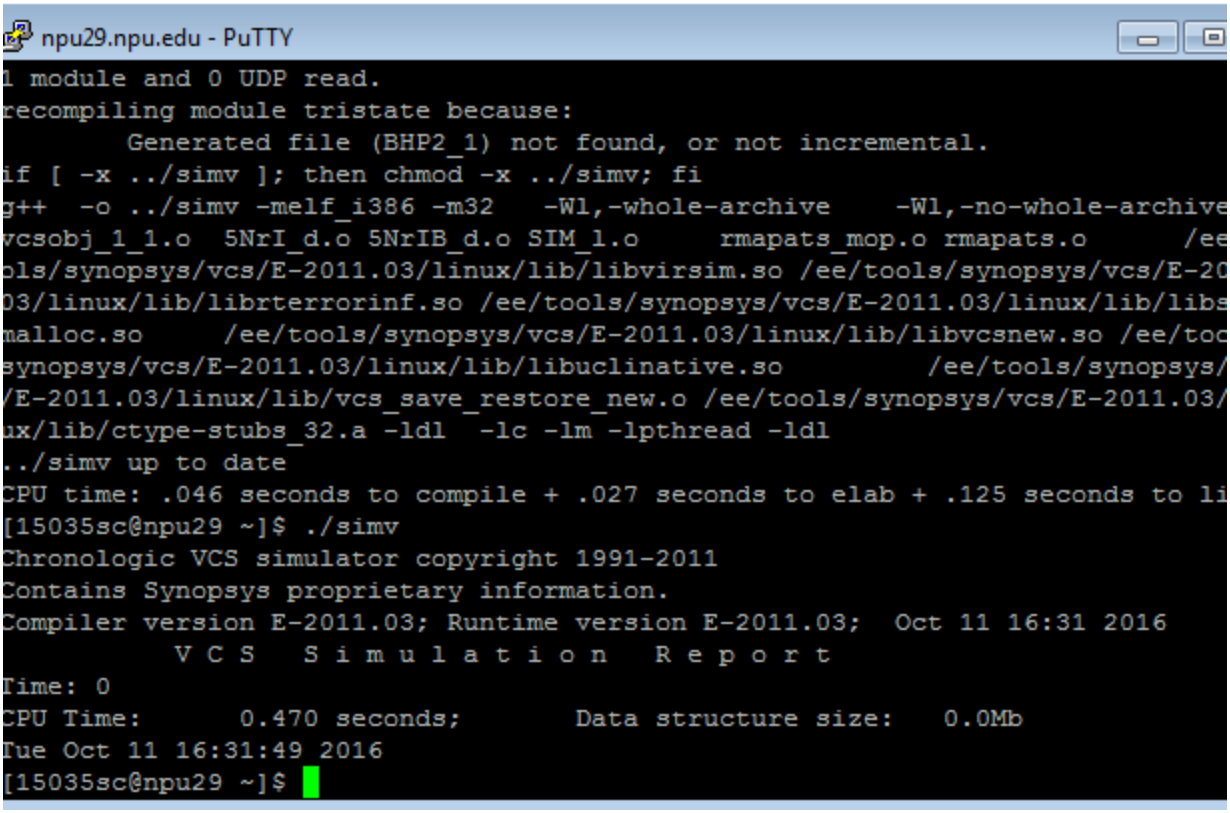


3. When a module name is &$$abc_123, how to make it pass compilation by writing a program to verify?

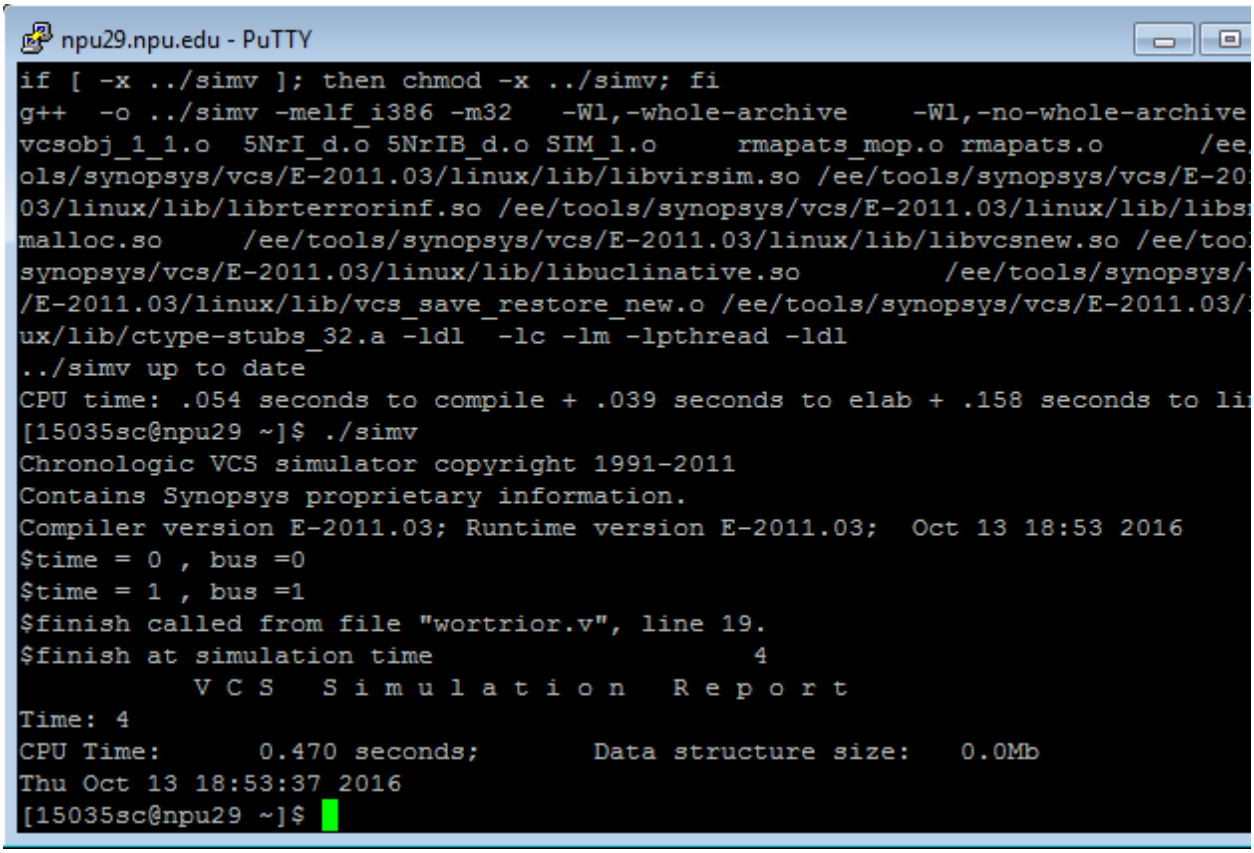


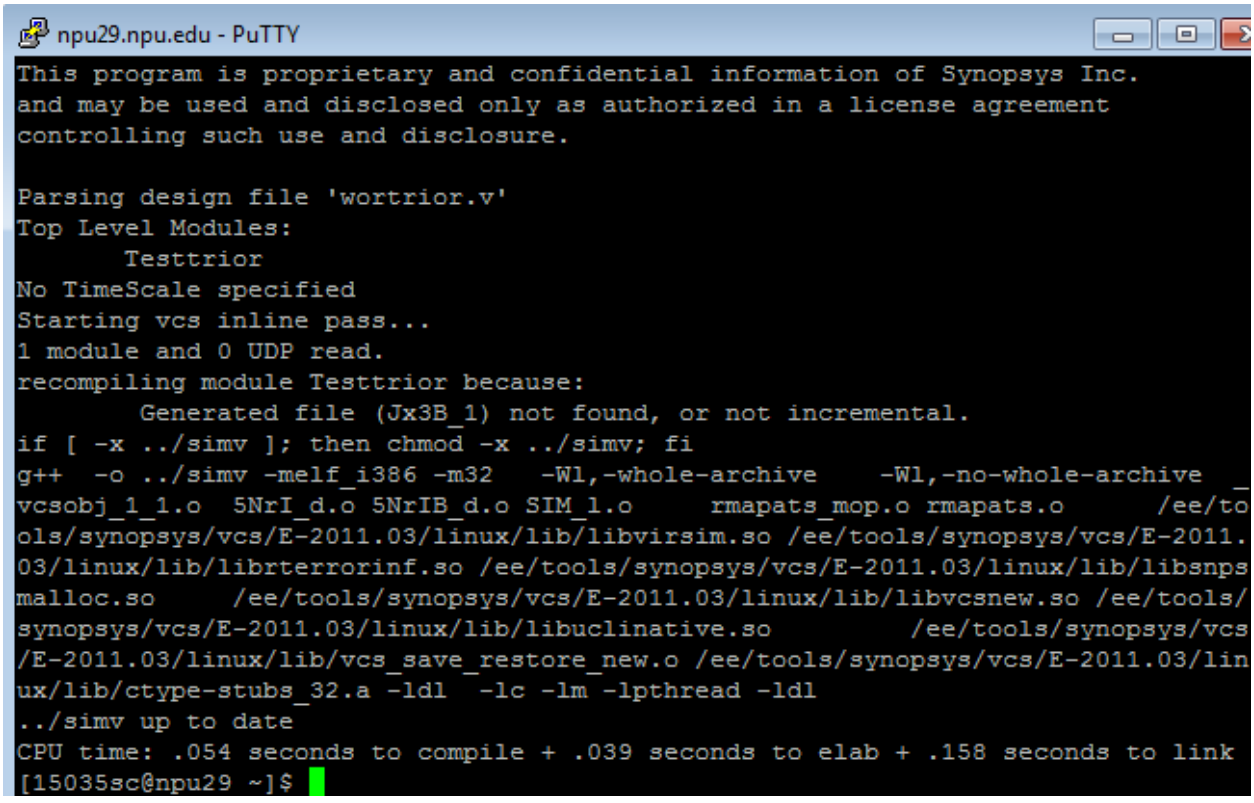
4. Define a variable type “tri”, and make two devices in the same value(e.g. 1, 1) and different value(e.g. z, x) to drive it, what do you get and show running results? Take an example on the handout as reference.

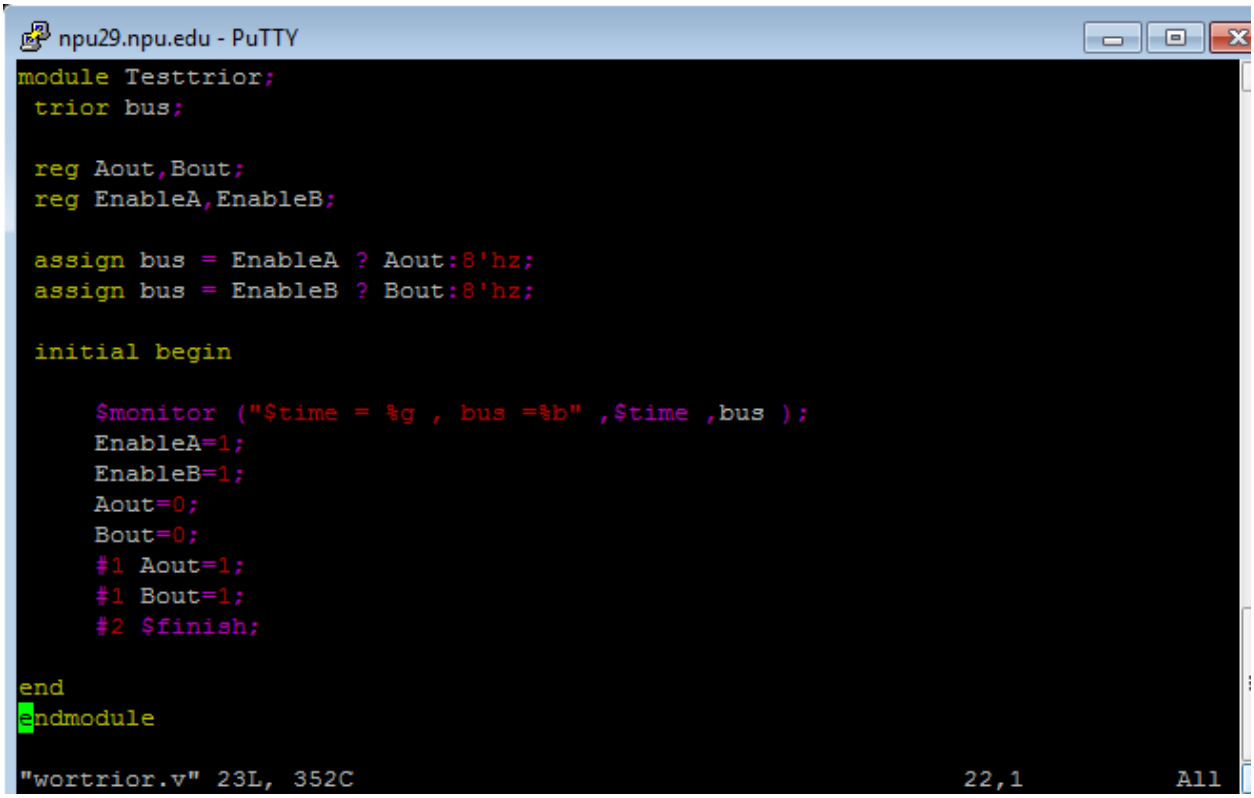


5. 

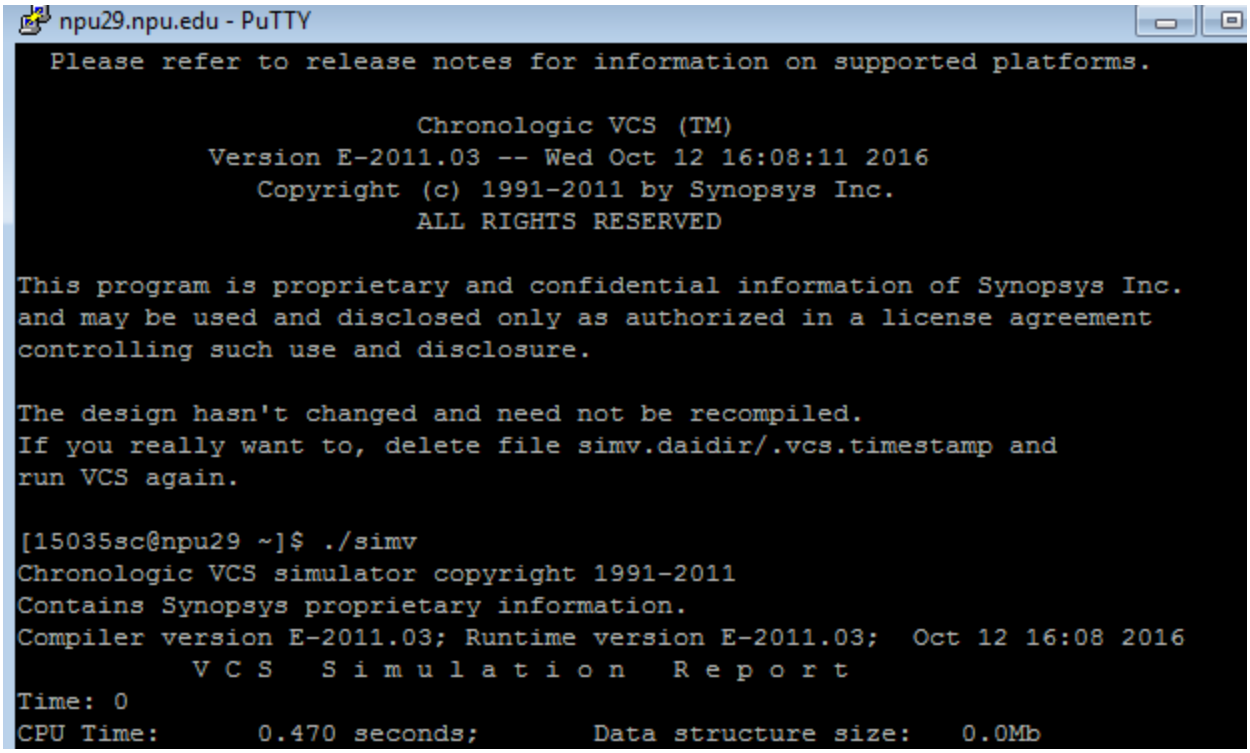
5. Retype “wor/trior ” and “wand/triand” test programs on the handout and assign all 16- combination values to them. Compare the results with the values in truth table. And show results.


npu29.npu.edu - PuTTY
if [-x ../simv]; then chmod -x ../simv; fi
g++ -o ../simv -melf_i386 -m32 -Wl,-whole-archive -Wl,-no-whole-archive
vcsobj_1_1.o 5NrI_d.o 5NrIB_d.o SIM_1.o rmapats_mop.o rmapats.o /ee
ols/synopsys/vcs/E-2011.03/linux/lib/libvirsim.so /ee/tools/synopsys/vcs/E-20
03/linux/lib/librterrorinf.so /ee/tools/synopsys/vcs/E-2011.03/linux/lib/libs
malloc.so /ee/tools/synopsys/vcs/E-2011.03/linux/lib/libvcsnew.so /ee/too
synopsys/vcs/E-2011.03/linux/lib/libuclinative.so /ee/tools/synopsys/
/E-2011.03/linux/lib/vcs_save_restore_new.o /ee/tools/synopsys/vcs/E-2011.03/
ux/lib/ctype-stubs_32.a -ldl -lc -lm -lpthread -ldl
../simv up to date
CPU time: .054 seconds to compile + .039 seconds to elab + .158 seconds to li
[15035sc@npu29 ~]$ ./simv
Chronologic VCS simulator copyright 1991-2011
Contains Synopsys proprietary information.
Compiler version E-2011.03; Runtime version E-2011.03; Oct 13 18:53 2016
$time = 0 , bus =0
$time = 1 , bus =1
$finish called from file "wortrior.v", line 19.
$finish at simulation time 4
V C S S i m u l a t i o n R e p o r t
Time: 4
CPU Time: 0.470 seconds; Data structure size: 0.0Mb
Thu Oct 13 18:53:37 2016
[15035sc@npu29 ~]$

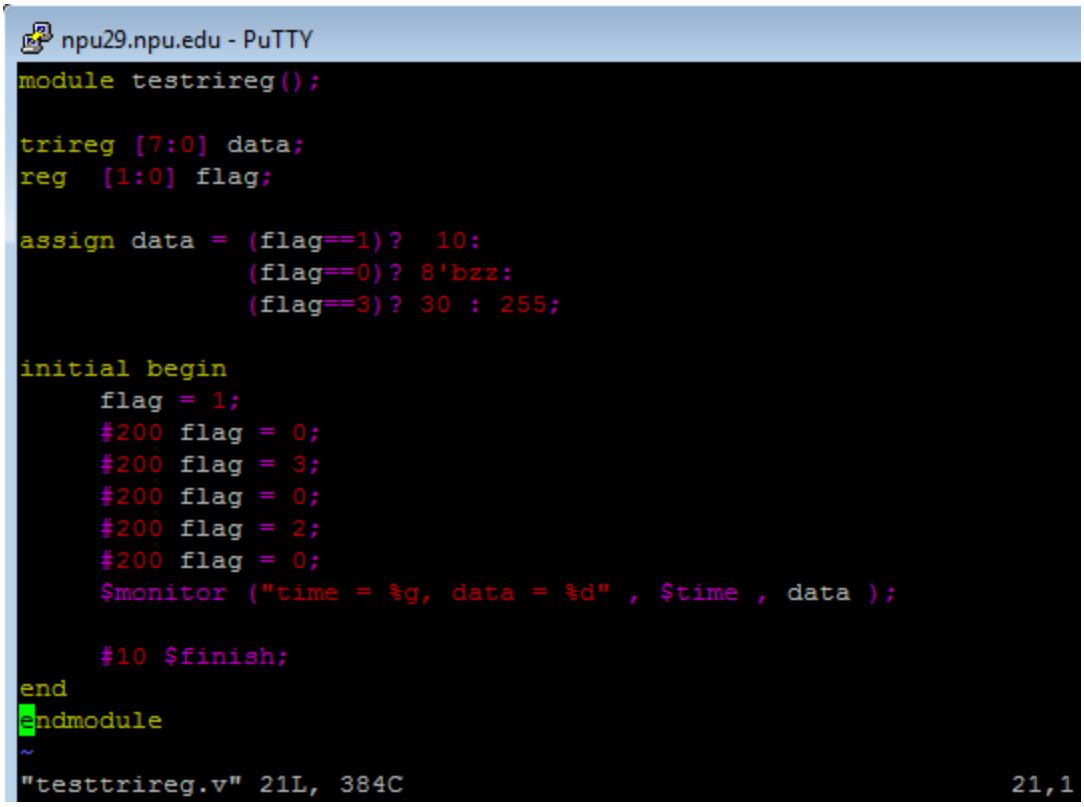

npu29.npu.edu - PuTTY
This program is proprietary and confidential information of Synopsys Inc.
and may be used and disclosed only as authorized in a license agreement
controlling such use and disclosure.
Parsing design file 'wortrior.v'
Top Level Modules:
Testtrior
No TimeScale specified
Starting vcs inline pass...
1 module and 0 UDP read.
recompiling module Testtrior because:
Generated file (Jx3B_1) not found, or not incremental.
if [-x ../simv]; then chmod -x ../simv; fi
g++ -o ../simv -melf_i386 -m32 -Wl,-whole-archive -Wl,-no-whole-archive _
vcsobj_1_1.o 5NrI_d.o 5NrIB_d.o SIM_1.o rmapats_mop.o rmapats.o /ee/to
ols/synopsys/vcs/E-2011.03/linux/lib/libvirsim.so /ee/tools/synopsys/vcs/E-2011.
03/linux/lib/librterrorinf.so /ee/tools/synopsys/vcs/E-2011.03/linux/lib/libsnps
malloc.so /ee/tools/synopsys/vcs/E-2011.03/linux/lib/libvcsnew.so /ee/tools/
synopsys/vcs/E-2011.03/linux/lib/libuclinative.so /ee/tools/synopsys/vcs
/E-2011.03/linux/lib/vcs_save_restore_new.o /ee/tools/synopsys/vcs/E-2011.03/lin
ux/lib/ctype-stubs_32.a -ldl -lc -lm -lpthread -ldl
../simv up to date
CPU time: .054 seconds to compile + .039 seconds to elab + .158 seconds to link
[15035sc@npu29 ~]$

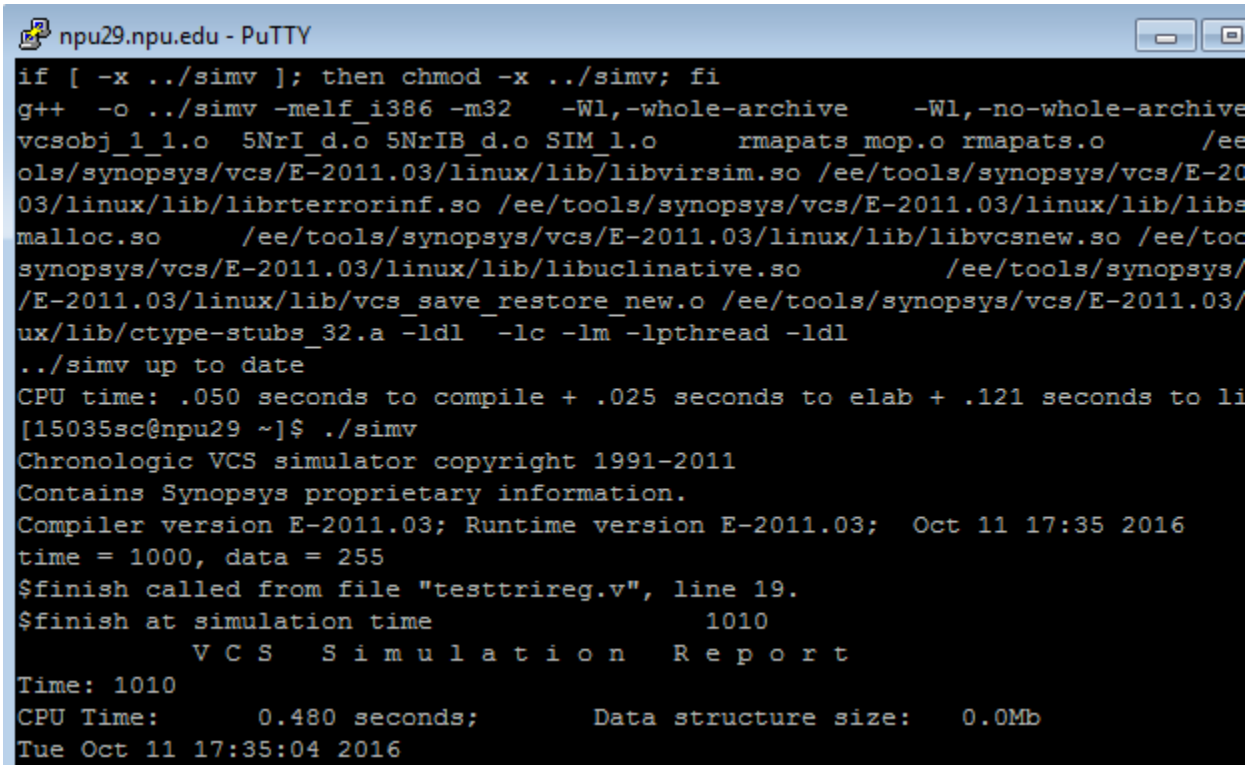


6. Generate variable type “tri0/tri1”, and assign 4 different values (0, 1, X, Z) to observe what you are going to

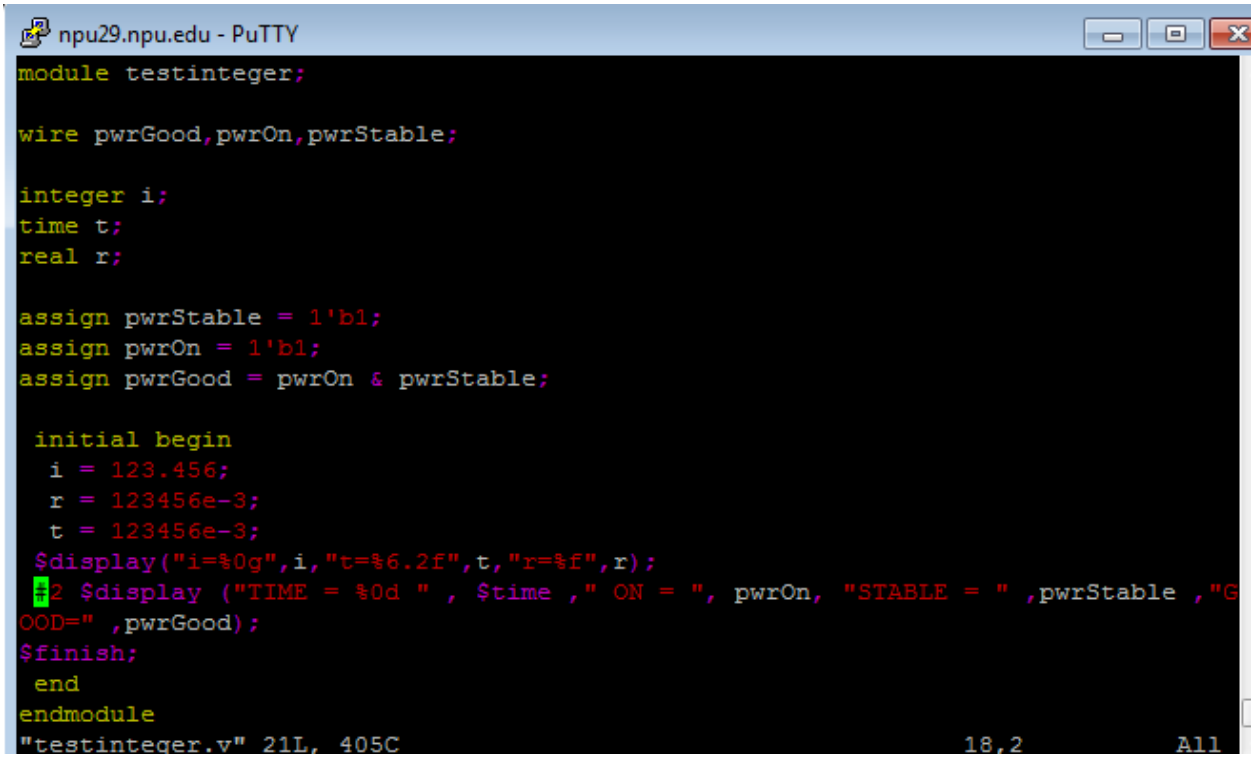


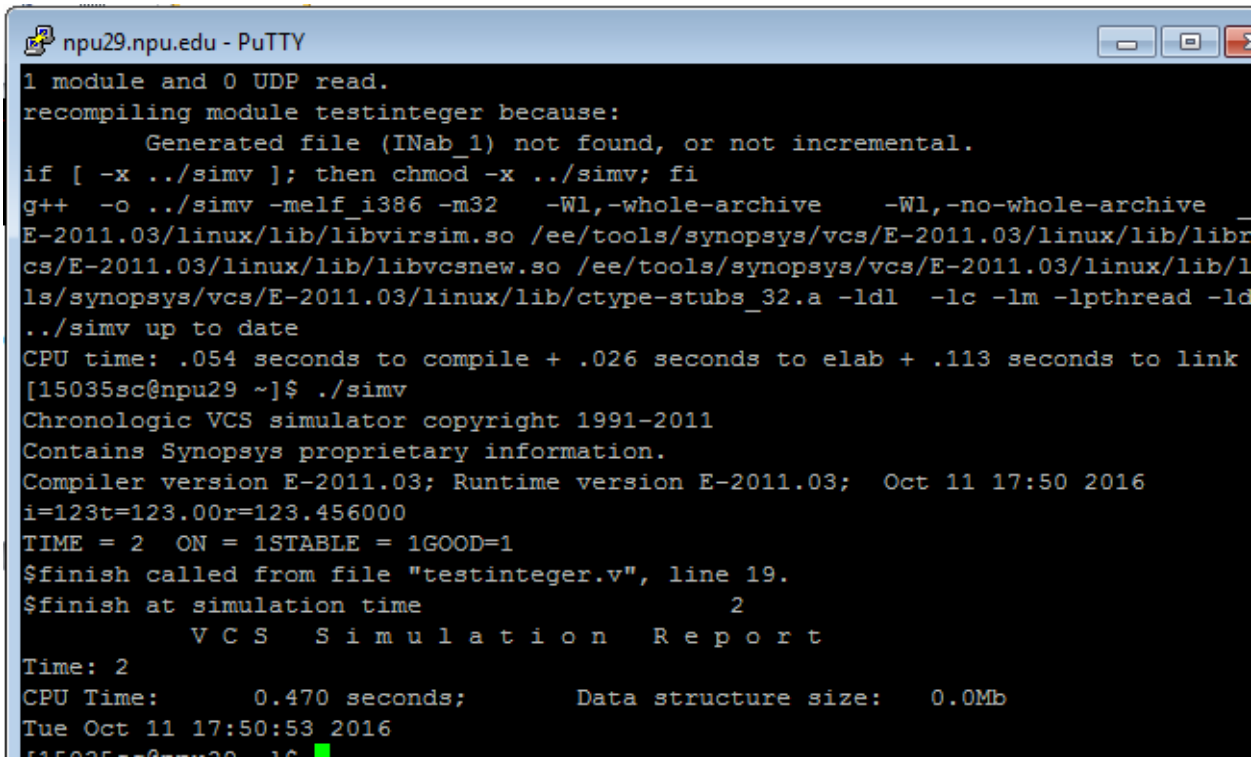
7. Retype “trireg” example code and provide the results.



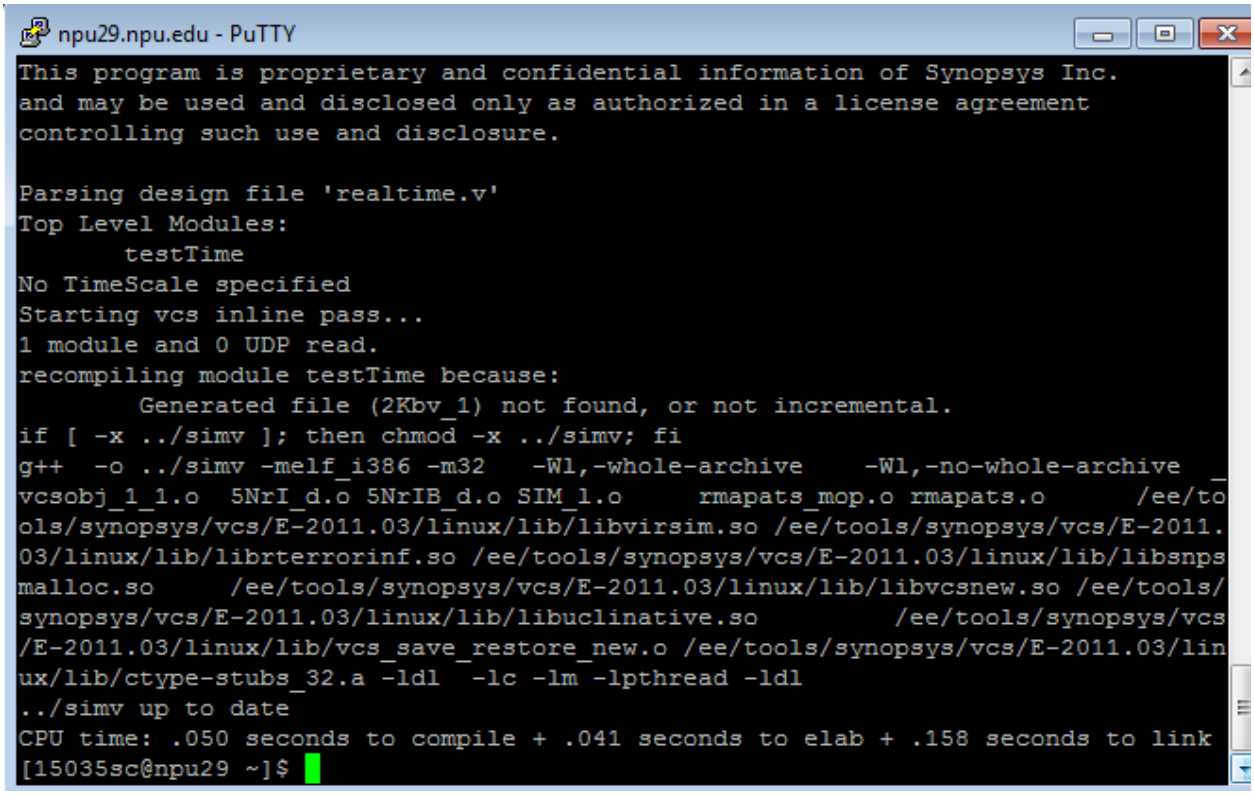


8. Retype “testInteger” program and give the results.

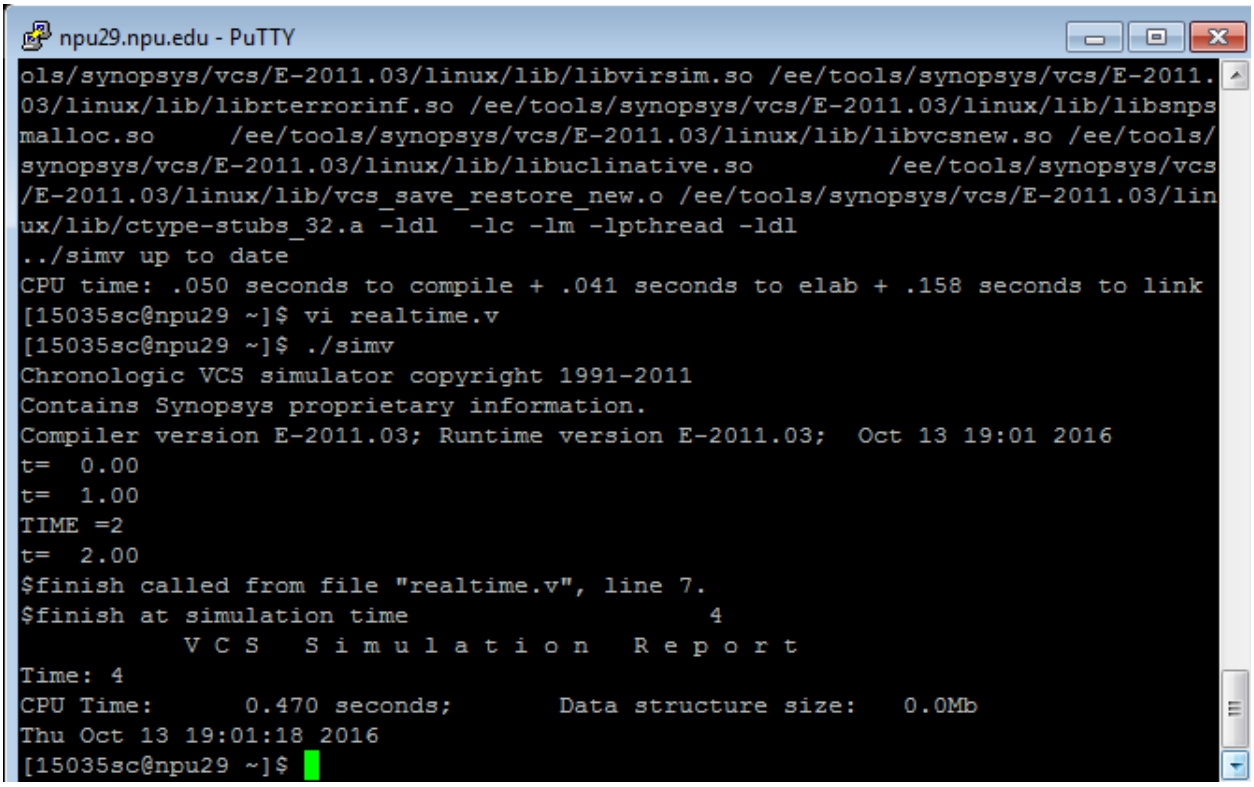




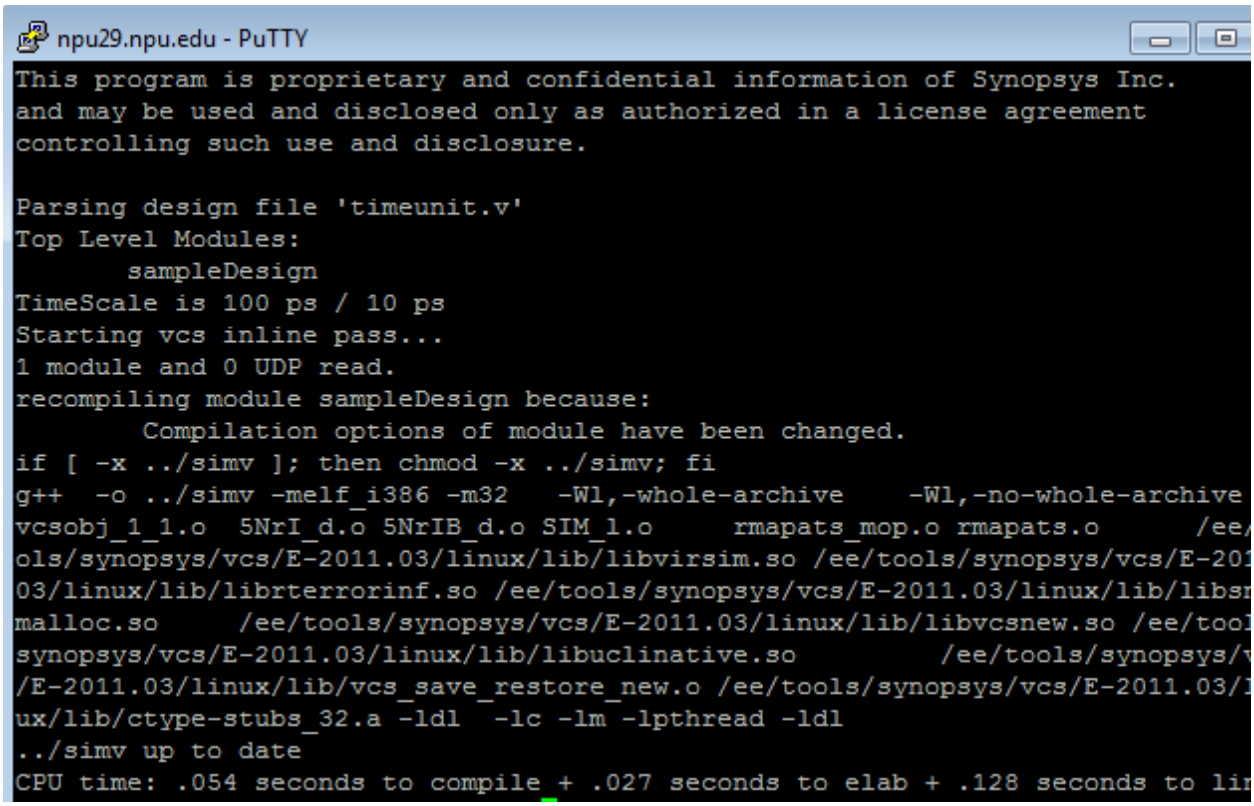
9. Create a “time” variable type and assign it values from $stime and $realtime, what will you get?

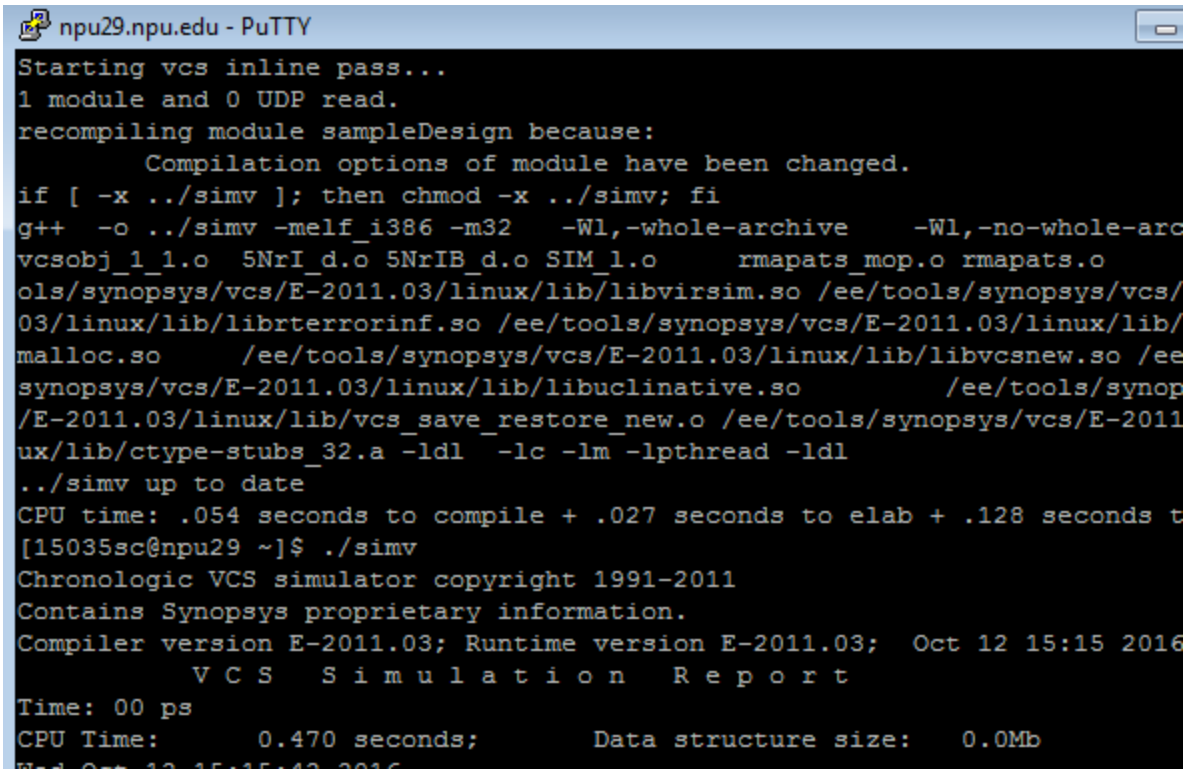

npu29.npu.edu - PuTTY
This program is proprietary and confidential information of Synopsys Inc.
and may be used and disclosed only as authorized in a license agreement
controlling such use and disclosure.
Parsing design file 'realtime.v'
Top Level Modules:
testTime
No TimeScale specified
Starting vcs inline pass...
1 module and 0 UDP read.
recompiling module testTime because:
Generated file (2Kbv_1) not found, or not incremental.
if [-x ../simv]; then chmod -x ../simv; fi
g++ -o ../simv -melf_i386 -m32 -Wl,-whole-archive -Wl,-no-whole-archive _
vcsobj_1_1.o 5NrI_d.o 5NrIB_d.o SIM_1.o rmapats_mop.o rmapats.o /ee/to
ols/synopsys/vcs/E-2011.03/linux/lib/libvirsim.so /ee/tools/synopsys/vcs/E-2011.
03/linux/lib/librterrorinf.so /ee/tools/synopsys/vcs/E-2011.03/linux/lib/libsnps
malloc.so /ee/tools/synopsys/vcs/E-2011.03/linux/lib/libvcsnew.so /ee/tools/
synopsys/vcs/E-2011.03/linux/lib/libuclinative.so /ee/tools/synopsys/vcs
/E-2011.03/linux/lib/vcs_save_restore_new.o /ee/tools/synopsys/vcs/E-2011.03/lin
ux/lib/ctype-stubs_32.a -ldl -lc -lm -lpthread -ldl
../simv up to date
CPU time: .050 seconds to compile + .041 seconds to elab + .158 seconds to link
[15035sc@npu29 ~]$


npu29.npu.edu - PuTTY
module testTime;
time t;
initial begin
t =$time;
#1 t=$time;
#1 t=$time;
#2 $finish;
end
initial begin
$monitor ("t=%6.2f",t);
#2 $display ("TIME =%0d",$time);
end
endmodule
"realtime.v" 15L, 208C
15,1
All

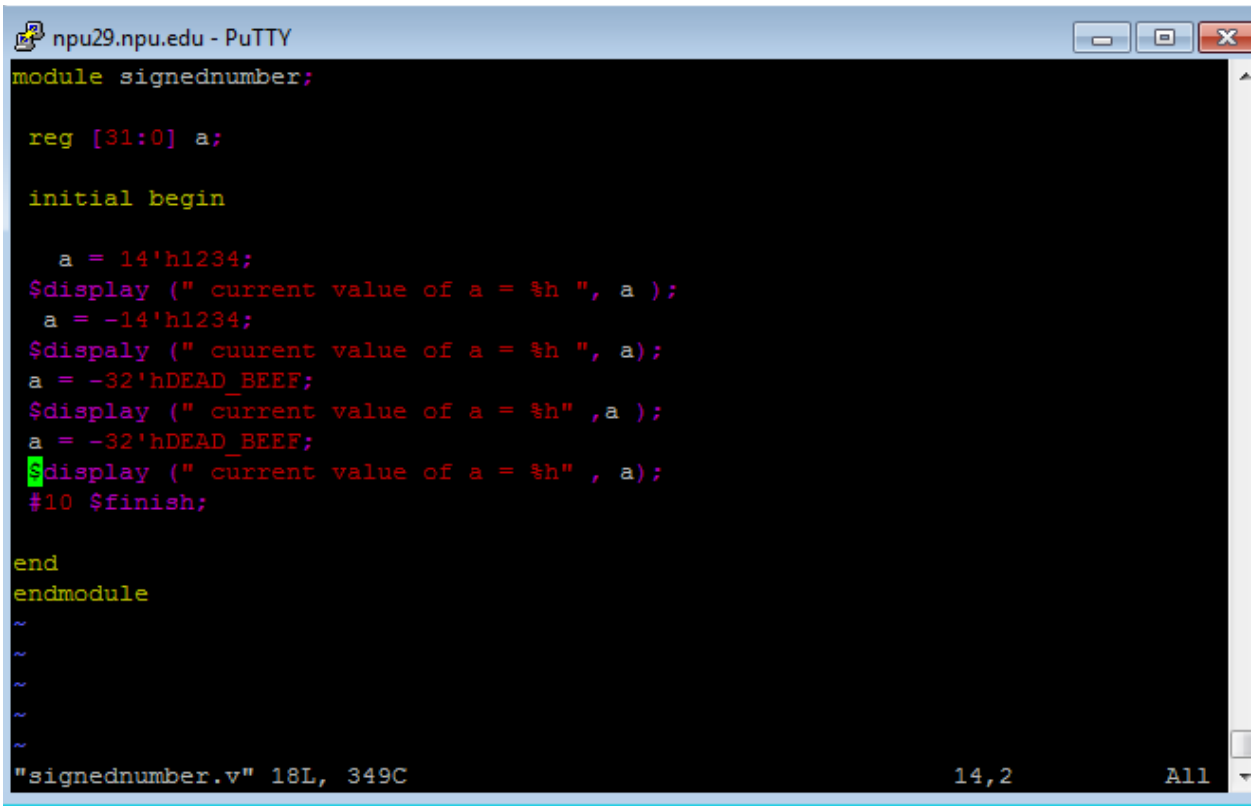


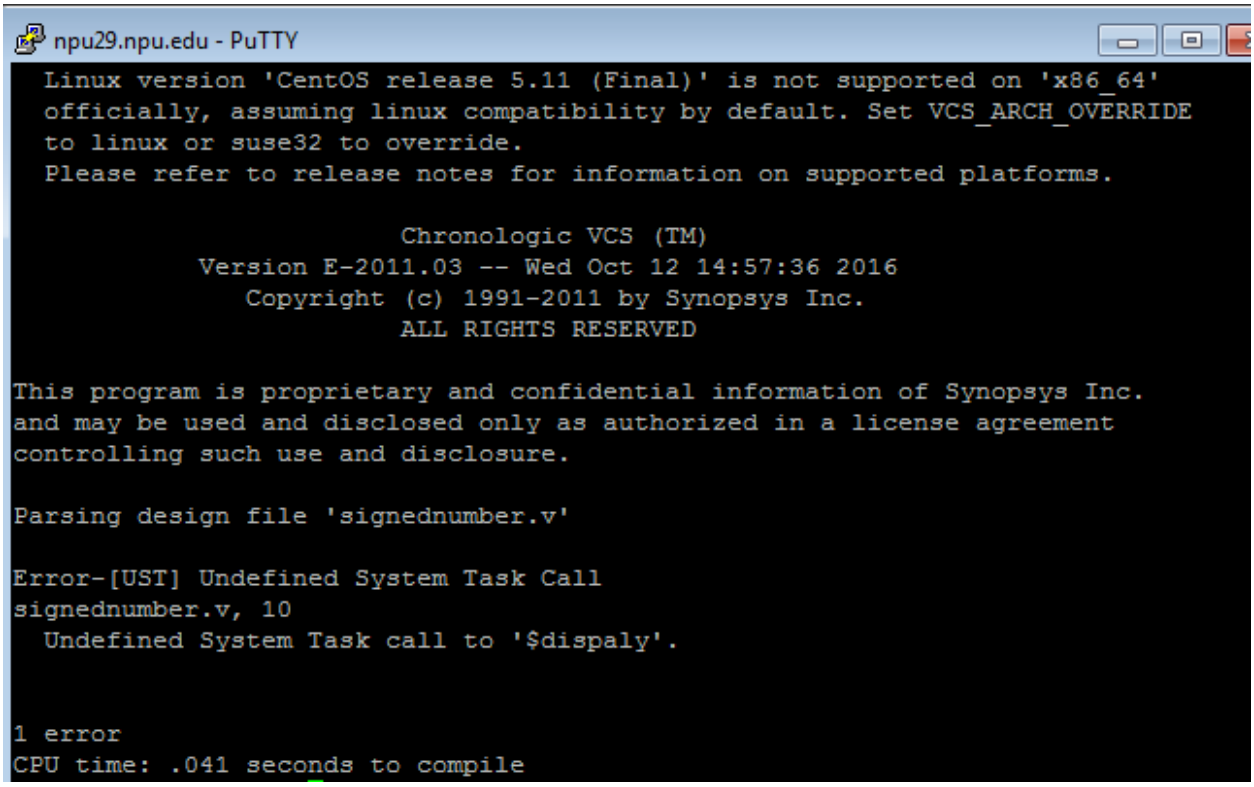
10. Define a time scale like `timescale 10ns/100ps, if a delay is #2.71828, calculate the real delay and compare what the difference between $display result in $time and your calculation is.



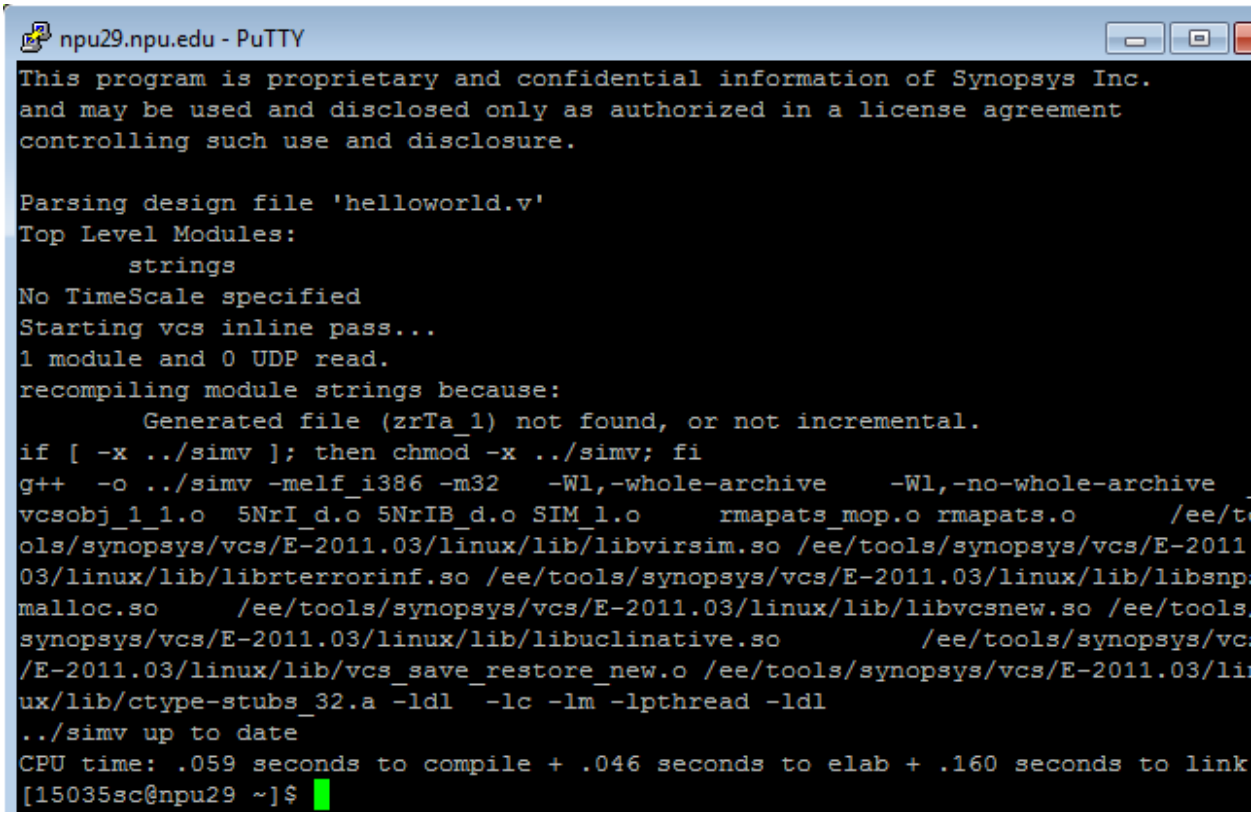


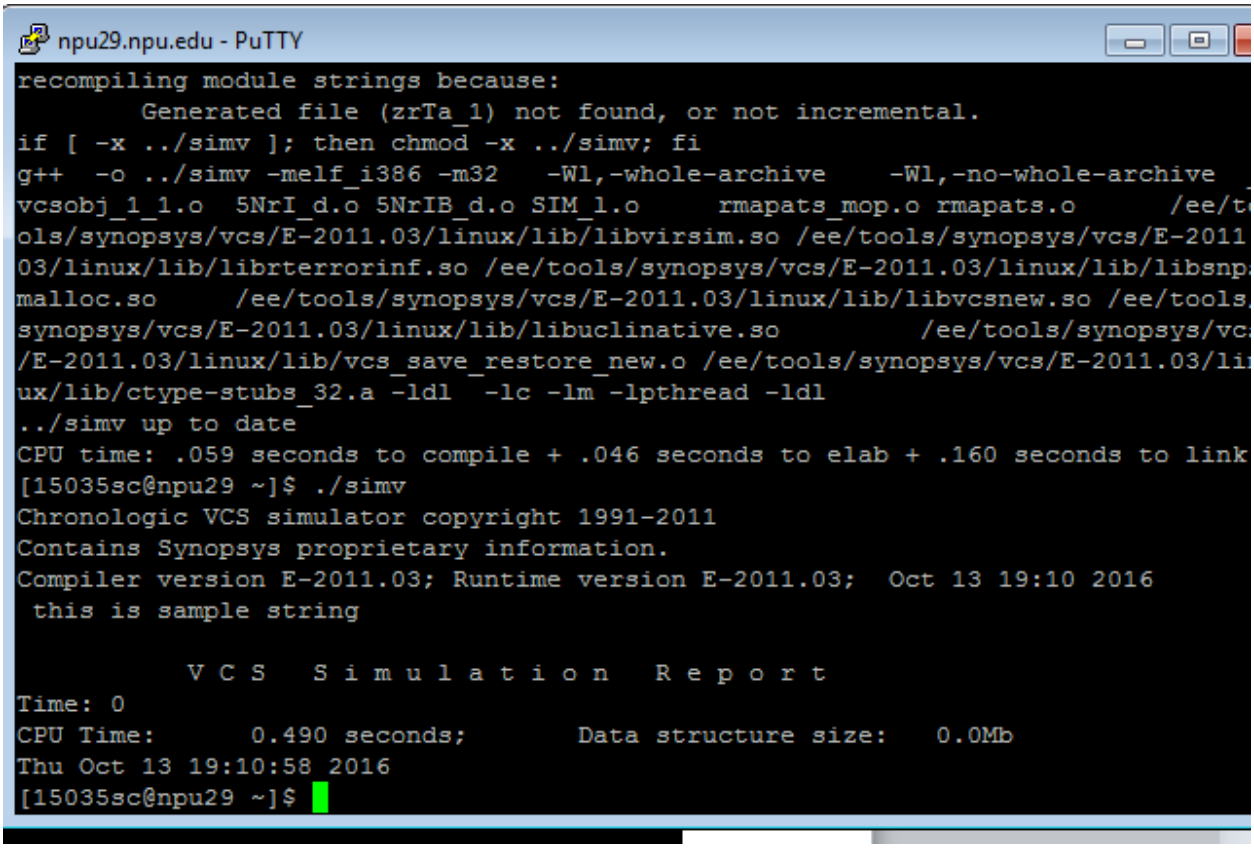
11. Retype “signedNumber” module, and observe the running results.

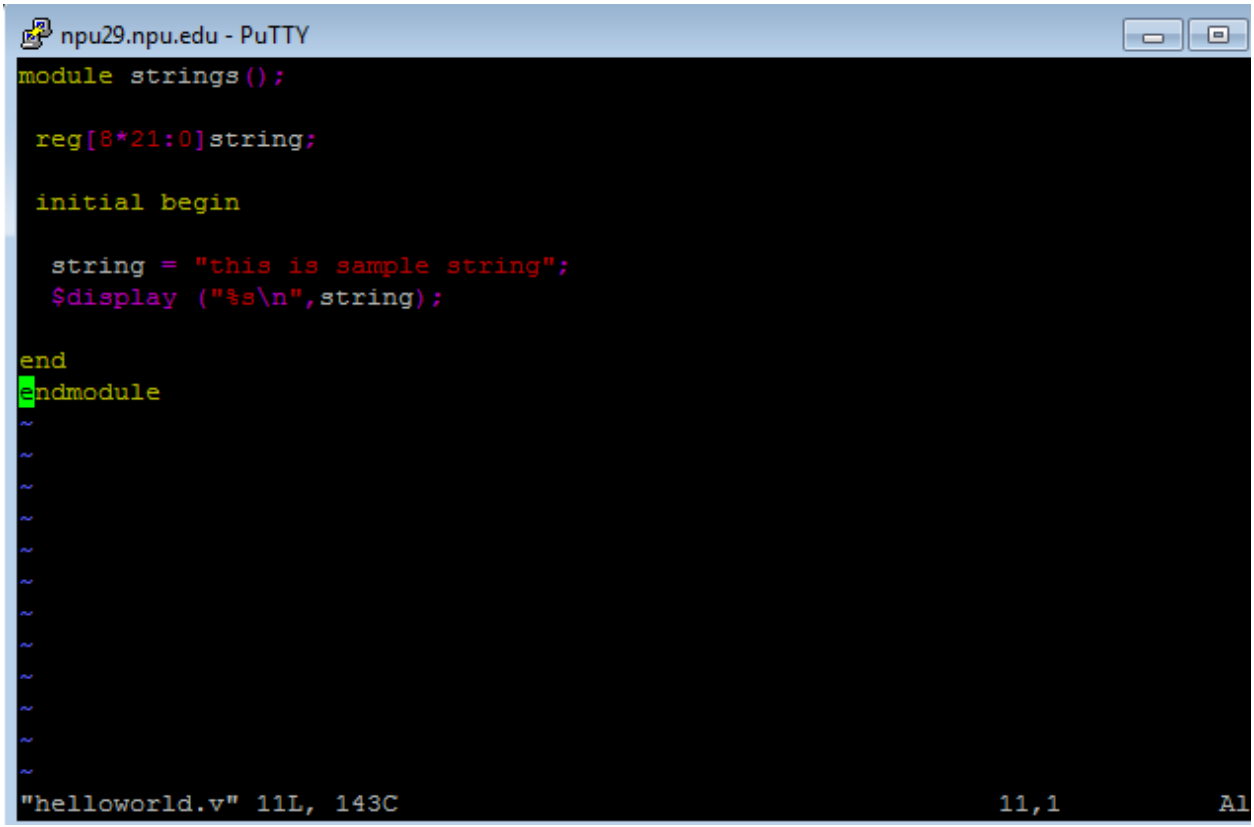




12. Take “helloWorld.v” as an example, write program to print double quote, percent character and @ character in ASCII code number.

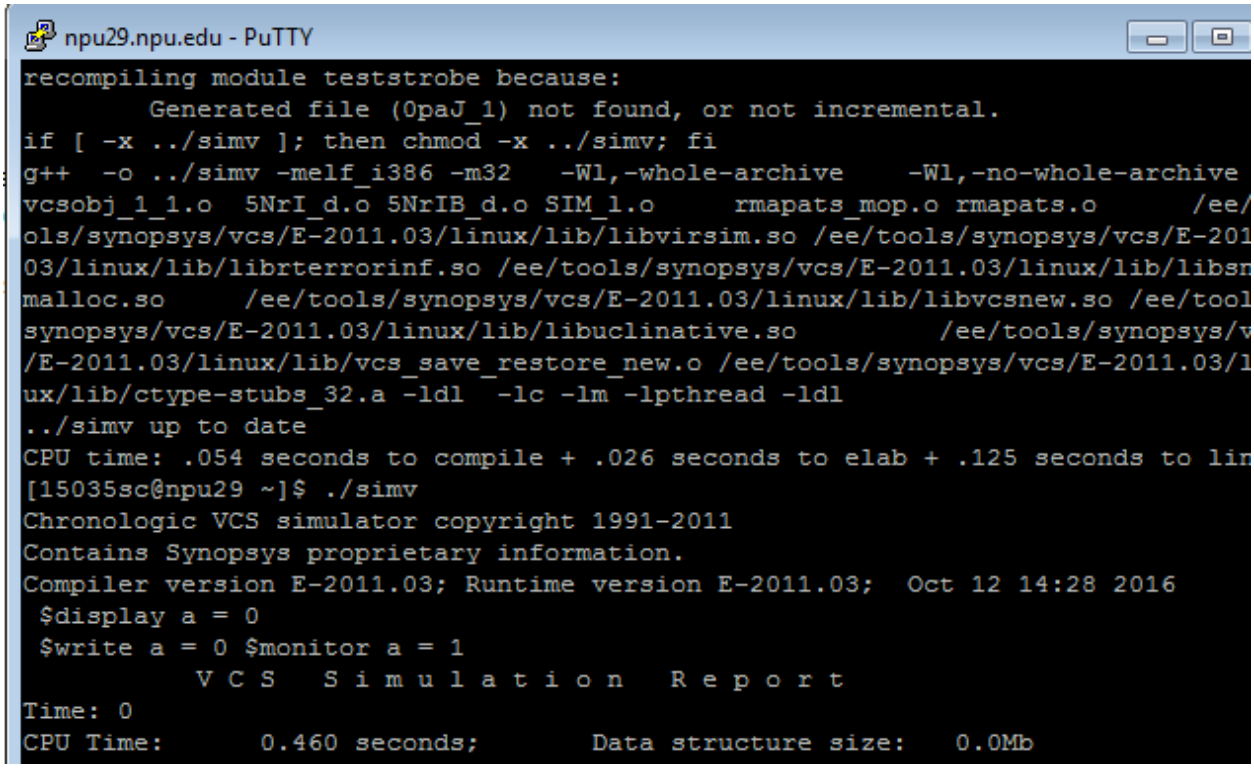

npu29.npu.edu - PuTTY
This program is proprietary and confidential information of Synopsys Inc.
and may be used and disclosed only as authorized in a license agreement
controlling such use and disclosure.
Parsing design file 'helloworld.v'
Top Level Modules:
strings
No TimeScale specified
Starting vcs inline pass...
1 module and 0 UDP read.
recompiling module strings because:
Generated file (zrTa_1) not found, or not incremental.
if [-x ../simv]; then chmod -x ../simv; fi
g++ -o ../simv -melf_i386 -m32 -Wl,-whole-archive -Wl,-no-whole-archive
vcsobj_1_1.o 5NrI_d.o 5NrIB_d.o SIM_1.o rmapats_mop.o rmapats.o /ee/t
ols/synopsys/vcs/E-2011.03/linux/lib/libvirsim.so /ee/tools/synopsys/vcs/E-2011
03/linux/lib/librterrorinf.so /ee/tools/synopsys/vcs/E-2011.03/linux/lib/libsnp
malloc.so /ee/tools/synopsys/vcs/E-2011.03/linux/lib/libvcsnew.so /ee/tools
synopsys/vcs/E-2011.03/linux/lib/libuclinative.so /ee/tools/synopsys/vc
/E-2011.03/linux/lib/vcs_save_restore_new.o /ee/tools/synopsys/vcs/E-2011.03/li
ux/lib/ctype-stubs_32.a -ldl -lc -lm -lpthread -ldl
../simv up to date
CPU time: .059 seconds to compile + .046 seconds to elab + .160 seconds to link
[15035sc@npu29 ~]$

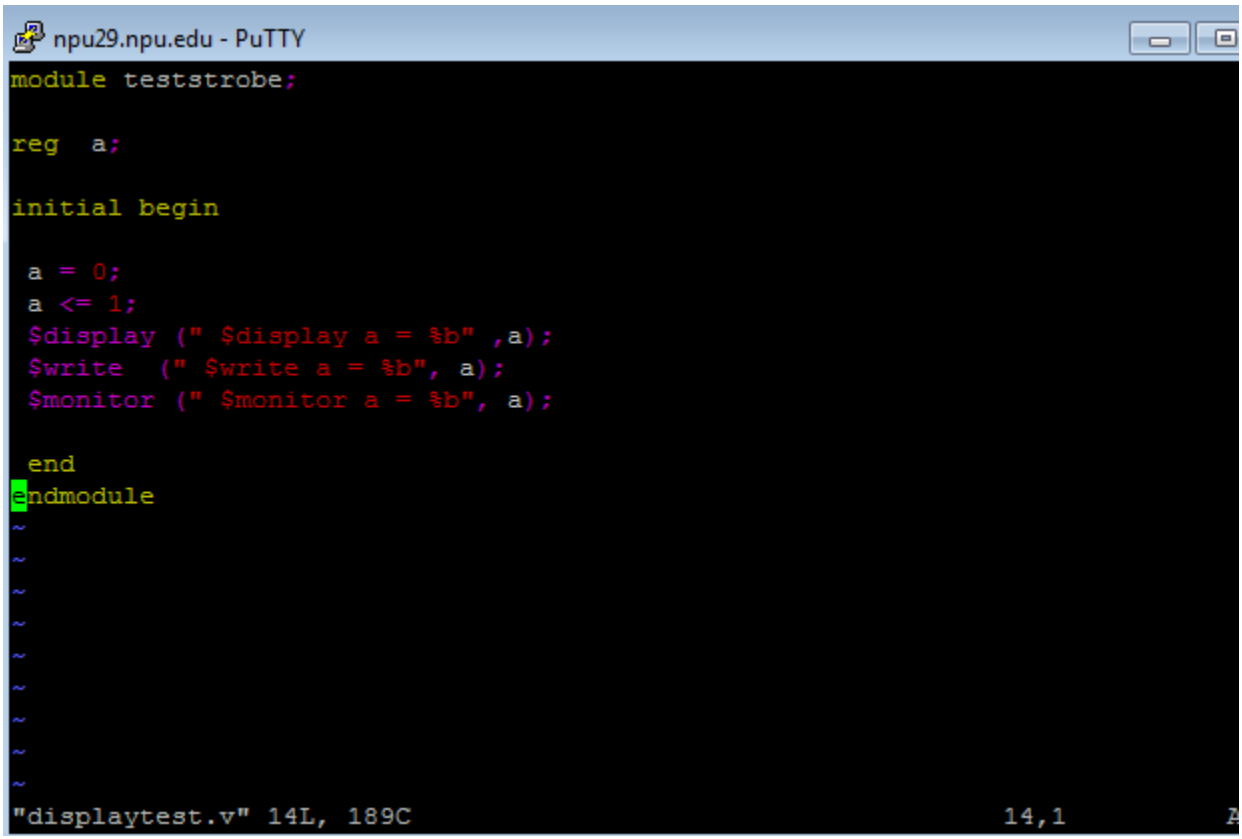

npu29.npu.edu - PuTTY
recompiling module strings because:
Generated file (zrTa_1) not found, or not incremental.
if [-x ../simv]; then chmod -x ../simv; fi
g++ -o ../simv -melf_i386 -m32 -Wl,-whole-archive -Wl,-no-whole-archive
vcsobj_1_1.o 5NrI_d.o 5NrIB_d.o SIM_1.o rmapats_mop.o rmapats.o /ee/t
ols/synopsys/vcs/E-2011.03/linux/lib/libvirsim.so /ee/tools/synopsys/vcs/E-2011
03/linux/lib/librterrorinf.so /ee/tools/synopsys/vcs/E-2011.03/linux/lib/libsnp
malloc.so /ee/tools/synopsys/vcs/E-2011.03/linux/lib/libvcsnew.so /ee/tools
synopsys/vcs/E-2011.03/linux/lib/libuclinative.so /ee/tools/synopsys/vc
/E-2011.03/linux/lib/vcs_save_restore_new.o /ee/tools/synopsys/vcs/E-2011.03/li
ux/lib/ctype-stubs_32.a -ldl -lc -lm -lpthread -ldl
../simv up to date
CPU time: .059 seconds to compile + .046 seconds to elab + .160 seconds to link
[15035sc@npu29 ~]$ ./simv
Chronologic VCS simulator copyright 1991-2011
Contains Synopsys proprietary information.
Compiler version E-2011.03; Runtime version E-2011.03; Oct 13 19:10 2016
this is sample string
V C S Simulation Report
Time: 0
CPU Time: 0.490 seconds; Data structure size: 0.0Mb
Thu Oct 13 19:10:58 2016
[15035sc@npu29 ~]$



13. Write a program to display values of different variables that could cover format like %b, %c, %d, %0d, %e, %f, %6.2f, %g, %h, %o, %s and %t, %00t.

14. Compare $display, $write and $monitor system tasks by a program, and give the running result


npu29.npu.edu - PuTTY
recompiling module teststrobe because:
Generated file (0paJ_1) not found, or not incremental.
if [-x ../simv]; then chmod -x ../simv; fi
g++ -o ../simv -melf_i386 -m32 -Wl,-whole-archive -Wl,-no-whole-archive
vcsobj_1_1.o 5NrI_d.o 5NrIB_d.o SIM_1.o rmapats_mop.o rmapats.o /ee/
ols/synopsys/vcs/E-2011.03/linux/lib/libvirsim.so /ee/tools/synopsys/vcs/E-201
03/linux/lib/librterrorinf.so /ee/tools/synopsys/vcs/E-2011.03/linux/lib/libsn
malloc.so /ee/tools/synopsys/vcs/E-2011.03/linux/lib/libvcsnew.so /ee/tool
synopsys/vcs/E-2011.03/linux/lib/libuclinative.so /ee/tools/synopsys/v
/E-2011.03/linux/lib/vcs_save_restore_new.o /ee/tools/synopsys/vcs/E-2011.03/l
ux/lib/ctype-stubs_32.a -ldl -lc -lm -lpthread -ldl
../simv up to date
CPU time: .054 seconds to compile + .026 seconds to elab + .125 seconds to lin
[15035sc@npu29 ~]$ ./simv
Chronologic VCS simulator copyright 1991-2011
Contains Synopsys proprietary information.
Compiler version E-2011.03; Runtime version E-2011.03; Oct 12 14:28 2016
$display a = 0
$write a = 0 $monitor a = 1
V C S S i m u l a t i o n R e p o r t
Time: 0
CPU Time: 0.460 seconds; Data structure size: 0.0Mb


npu29.npu.edu - PuTTY
module teststrobe;
reg a;
initial begin
a = 0;
a <= 1;
$display (" $display a = %b" ,a);
$write (" $write a = %b", a);
$monitor (" $monitor a = %b", a);
end
endmodule
"displaytest.v" 14L, 189C 14,1