Northwestern Polytechnic University
EE461 Digital Design and HDL

Examples of Logic Synthesis Scripting

I. Examples of Combinational Logic Synthesis in RTL

1. One-Bit Full Adder Design in Continuous Assignment

RTL Level Design (File Name: oneBitFA1.v):

```
module oneBitFA1(
            input wire a_i,
            input wire b_i,
            input wire ci_i,
            output wire sum_o,
            output wire co_o
);
      assign   {co_o,sum_o} = a_i + b_i + ci_i;
endmodule
```

Logic Synthesis:

>> vi oneBitFA1Syn.scr

```
include   /ee/setup/synopsys/synopsys_setup_npu018.inc
read -f verilog oneBitFA1.v
current_design = oneBitFA1
link
compile
create_schematic
plot -output oneBitFA1.ps
write -f verilog -o oneBitFA1.vs -hierarchy
exit
```

>> source /ee/setup/synopsys/setup.cmd

>> dc_shell -f oneBitFA1Syn.scr

> >ls

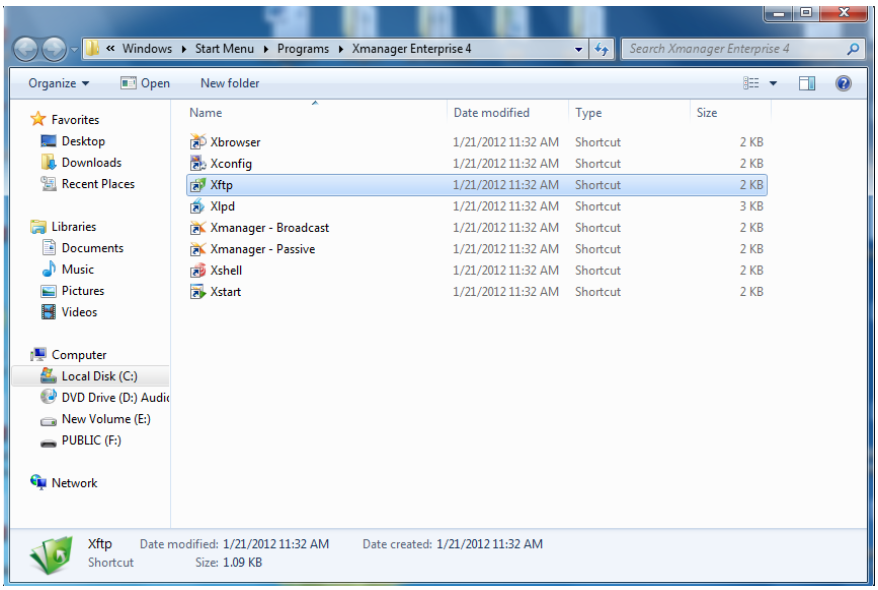
Notes: You will find two files `oneBitFA1.vs` **and** `oneBitFA1.ps`**.** `oneBitFA1.vs` **is Verilog module in gate level (Netlist) after logic synthesis, but** `oneBitFA1.ps` **is a schematic of this synthesized netlist. Convert it to pdf file by**

>> ps2pdf `oneBitFA1.ps`

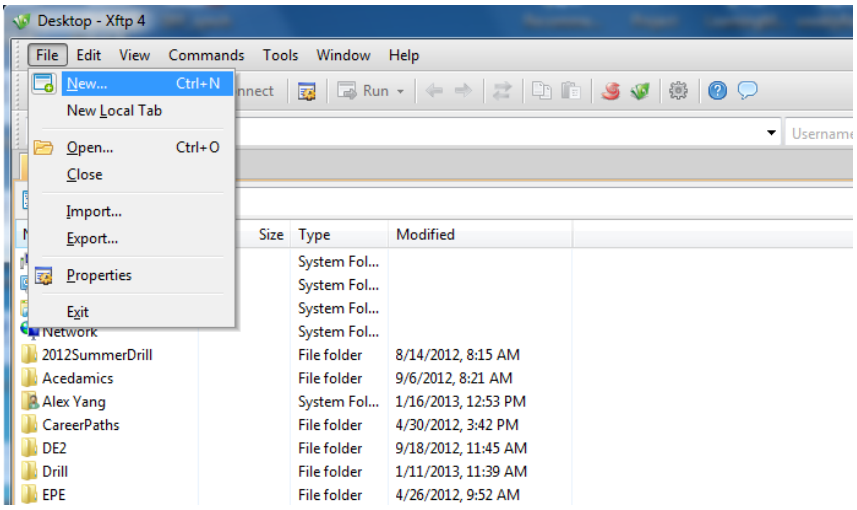
>>**ls**

Congratulations! You've got `oneBitFA1.pdf` file with 1-bit full adder schematic. If you want to move it to your windows system and open it. Please follow the instructions as belows.

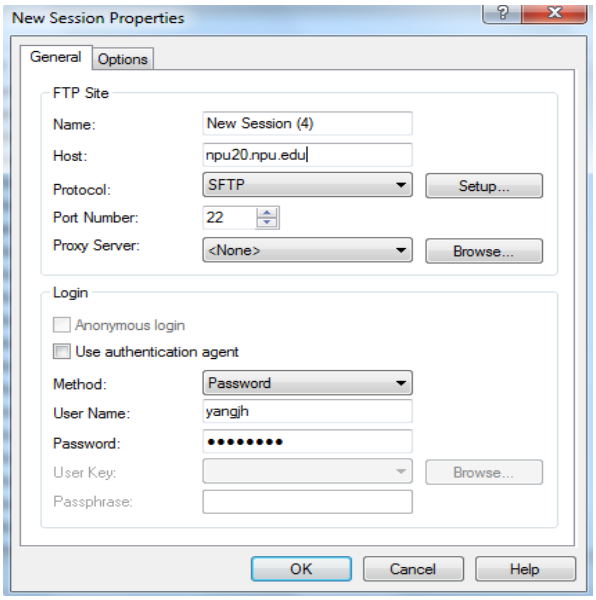
1) **Open "Xmanager", click "Xftp"**



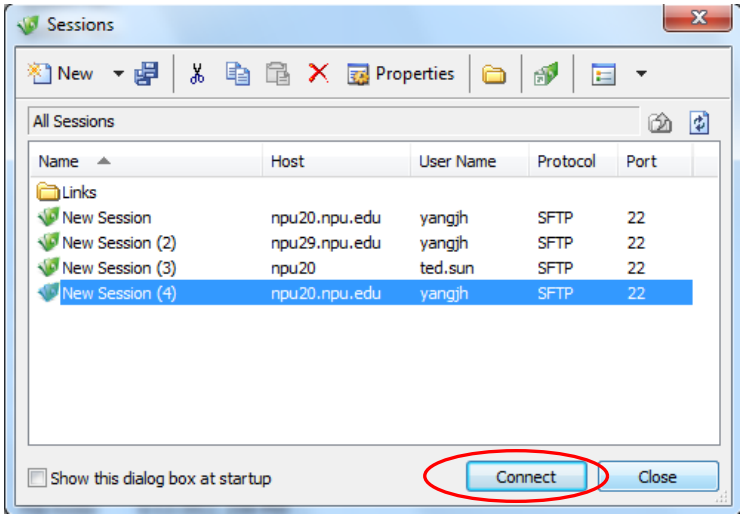
2) Select “File -> New”



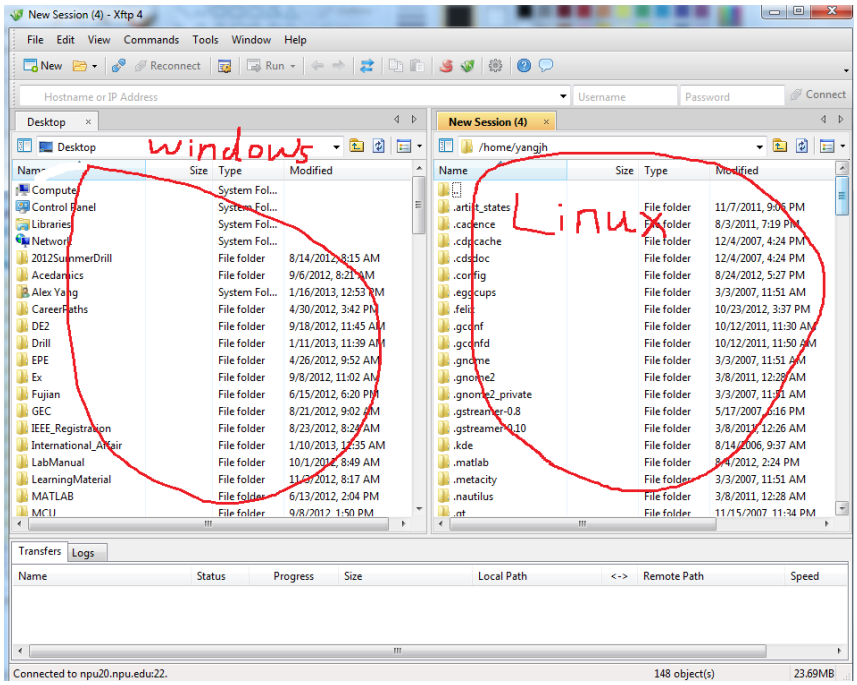
3) Fill in the form as below, and then click OK.



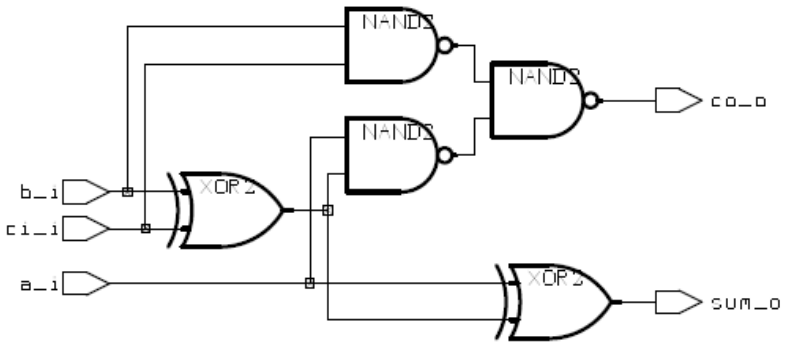
4) **Click "Connect"**



5) **Select the file that you want to move between two systems, and hold & drag from the window to the other.**



6) **Check the schematic by opening pdf file.**



2. One-Bit Full Adder Design in "always" block

RTL Level Design (File Name: oneBitFA2.v):

```
module oneBitFA2(
            input wire a_i,
            input wire b_i,
            input wire ci_i,
            output reg sum_o,
            output reg co_o
);

      always @(a_i, b_i, ci_i)begin
            {co_o, sum_o} = a_i + b_i + ci_i;
      end
endmodule
```

Logic Synthesis:

>> vi oneBitFA2Syn.scr

```
include   /ee/setup/synopsys/synopsys_setup_npu018.inc
read -f verilog oneBitFA2.v
current_design = oneBitFA2
link
compile
create_schematic
plot -output oneBitFA2.ps
write -f verilog -o oneBitFA2.vs -hierarchy
exit
```

>> source /ee/setup/synopsys/setup.cmd
>> dc_shell -f oneBitFA2Syn.scr
> >ls

Open schematic pdf file to compare with example as above.

II. Examples of Sequential Logic Synthesis in RTL

1. Logic Synchronous DFF

RTL Level Design (File Name: DFFSynch.v):

```
module DFFSynch(
                  d_i,
                  rst_i,
                  clk,
                  q_o
);
       input d_i,rst_i,clk;
       output q_o;

       reg q_o;

       always @(posedge clk)begin
            if(rst_i)   q_o <= 0;
            else        q_o <= d_i;
       end
endmodule
```

2. Logic Asynchronous DFF

RTL Level Design (File Name: DFFASynch.v):

```
module DFFAsynch(
                  d_i,
                  rst_i,
                  clk,
                  q_o
);
input d_i,rst_i,clk;
output q_o;
```

```
      reg q_o;

      always @(posedge clk or posedge rst_i)begin
            if(rst_i)   q_o <= 0;
            else        q_o <= d_i;
      end
endmodule
```