Northwestern Polytechnic University

EE461 Verilog-HDL

Lab Assignment #5

Due day: 12/17/2016

Instruction:

1. Print your program for each question in "word" file and paste running results in screen shot on it. Printing results or electrical copies from monitor can't be accepted.
2. Please follow the code style rule like programs on handout.
3. Overdue homework submission could not be accepted.
4. Takes academic honesty and integrity seriously (Zero Tolerance of Cheating & Plagiarism)

1. Draw FSM logic chart to detect bit stream pattern "1011" and design FSM in Verilog to output flag signal.

3. Design FSM in Verilog to detect bit stream which could be divided by 7 and output flag signal.