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15035

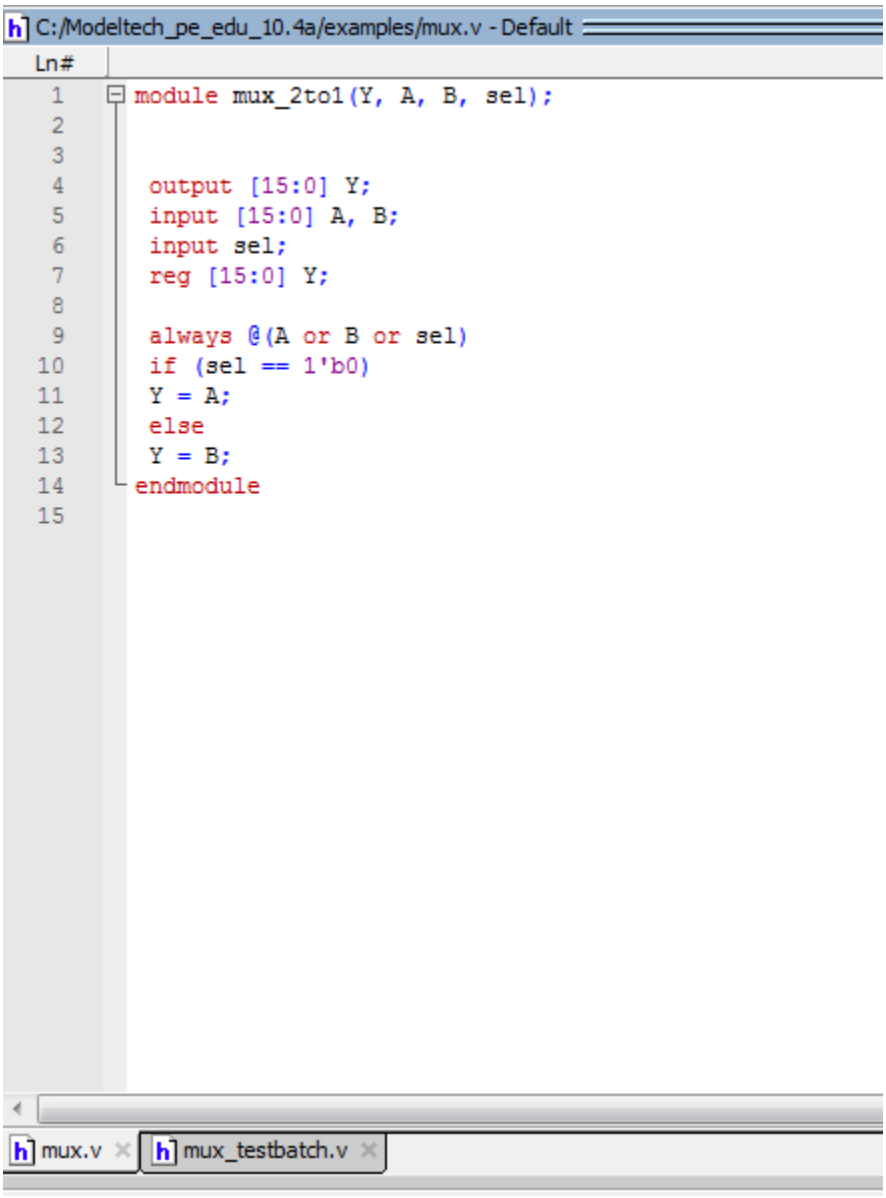
Homework assignment 3

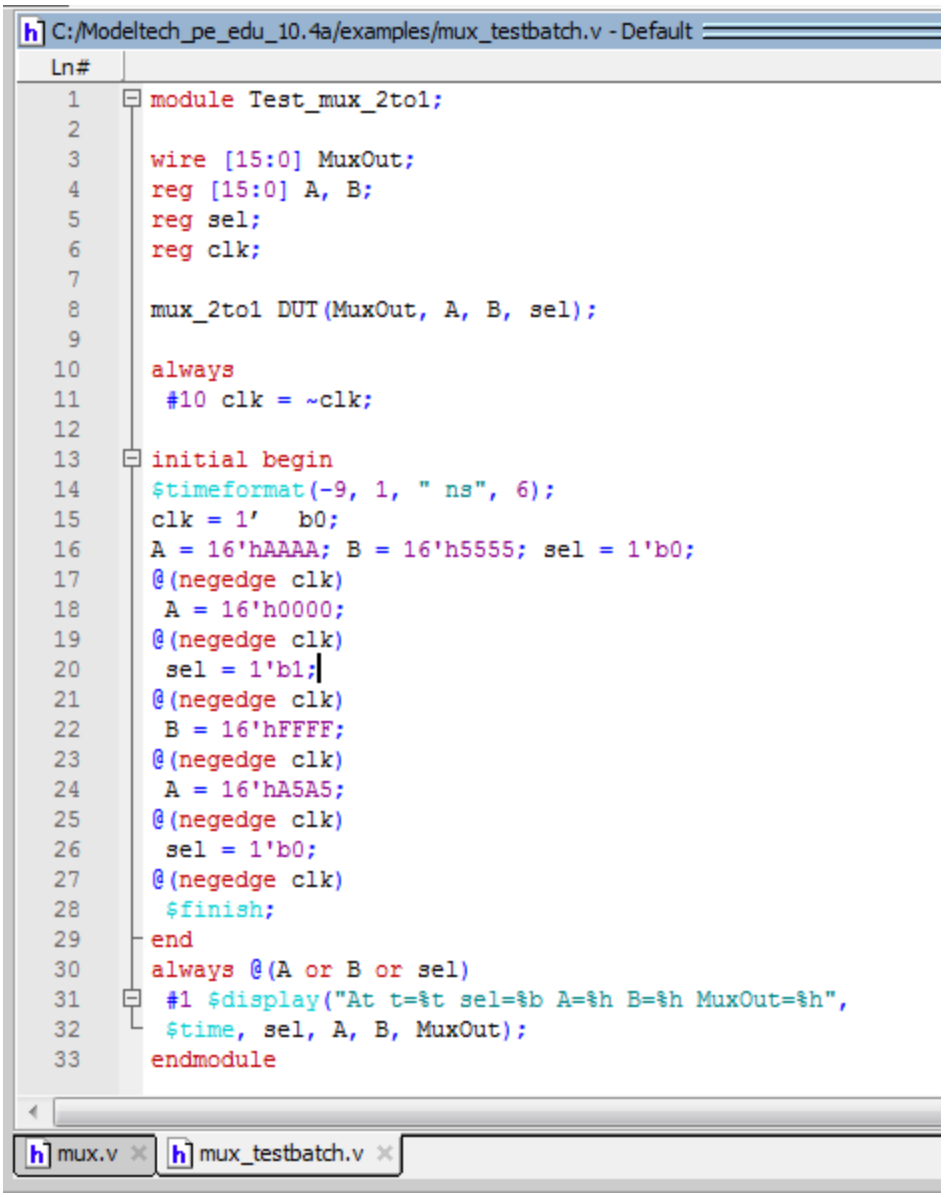
Answer1

C:/Modeltech_pe_edu_10.4a/examples/cmosfun_.v - Default

```
Ln#
 1
 2  module cmos_nand ( input a, b, output y );
 3  wire im1;
 4  supply1 vdd;
 5  supply0 gnd;
 6  pmos #(4, 5)
 7  g1 (y, vdd, a),
 8  g2 (y, vdd, b);
 9  nmos #(3, 4)
10  g3 (im1, gnd, b),
11  g4 (w, im1, a);
12  endmodule
13
```

Answer 2


C:/Modeltech_pe_edu_10.4a/examples/mux.v - Default
Ln#
1 module mux_2to1(Y, A, B, sel);
2
3
4 output [15:0] Y;
5 input [15:0] A, B;
6 input sel;
7 reg [15:0] Y;
8
9 always @(A or B or sel)
10 if (sel == 1'b0)
11 Y = A;
12 else
13 Y = B;
14 endmodule
15
mux.v
mux_testbatch.v


C:/Modeltech_pe_edu_10.4a/examples/mux_testbatch.v - Default
Ln#
1 module Test_mux_2to1;
2
3 wire [15:0] MuxOut;
4 reg [15:0] A, B;
5 reg sel;
6 reg clk;
7
8 mux_2to1 DUT(MuxOut, A, B, sel);
9
10 always
11 #10 clk = ~clk;
12
13 initial begin
14 $timeformat(-9, 1, " ns", 6);
15 clk = 1' b0;
16 A = 16'hAAAA; B = 16'h5555; sel = 1'b0;
17 @(negedge clk)
18 A = 16'h0000;
19 @(negedge clk)
20 sel = 1'b1;
21 @(negedge clk)
22 B = 16'hFFFF;
23 @(negedge clk)
24 A = 16'hA5A5;
25 @(negedge clk)
26 sel = 1'b0;
27 @(negedge clk)
28 $finish;
29 end
30 always @(A or B or sel)
31 #1 $display("At t=%t sel=%b A=%h B=%h MuxOut=%h",
32 $time, sel, A, B, MuxOut);
33 endmodule
mux.v
mux_testbatch.v

Answer 3

C:/Modeltech_pe_edu_10.4a/examples/UDP_.v - Default

```
Ln#
 1  Primitiv MUX (f,a,b,sell);
 2  Endprimitive
 3
 4  Primtive inv (inb,in);
 5  Endprimitive
 6
 7  Primitive or(f,a,b);
 8  Endprimitive
 9
10  module Top(a,b,c,d,out);
11   or u0ro();
12  endmodule
```

## Answer 4

```
primitive crctp (x,A,B,C);
   output x;
   input A,B,C;
//Truth table for x (A,B,C) = Minterms (0,2,4,6,7)
   table
//     A   B   C  :  x  (  this is only a comment)
       0   0   0  :  1;
       0   0   1  :  0;
       0   1   0  :  1;
       0   1   1  :  0;
       1   0   0  :  1;
       1   0   1  :  0;
       1   1   0  :  1;
       1   1   1  :  1;
   endtable
endprimitive
```