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Homework assignment 4

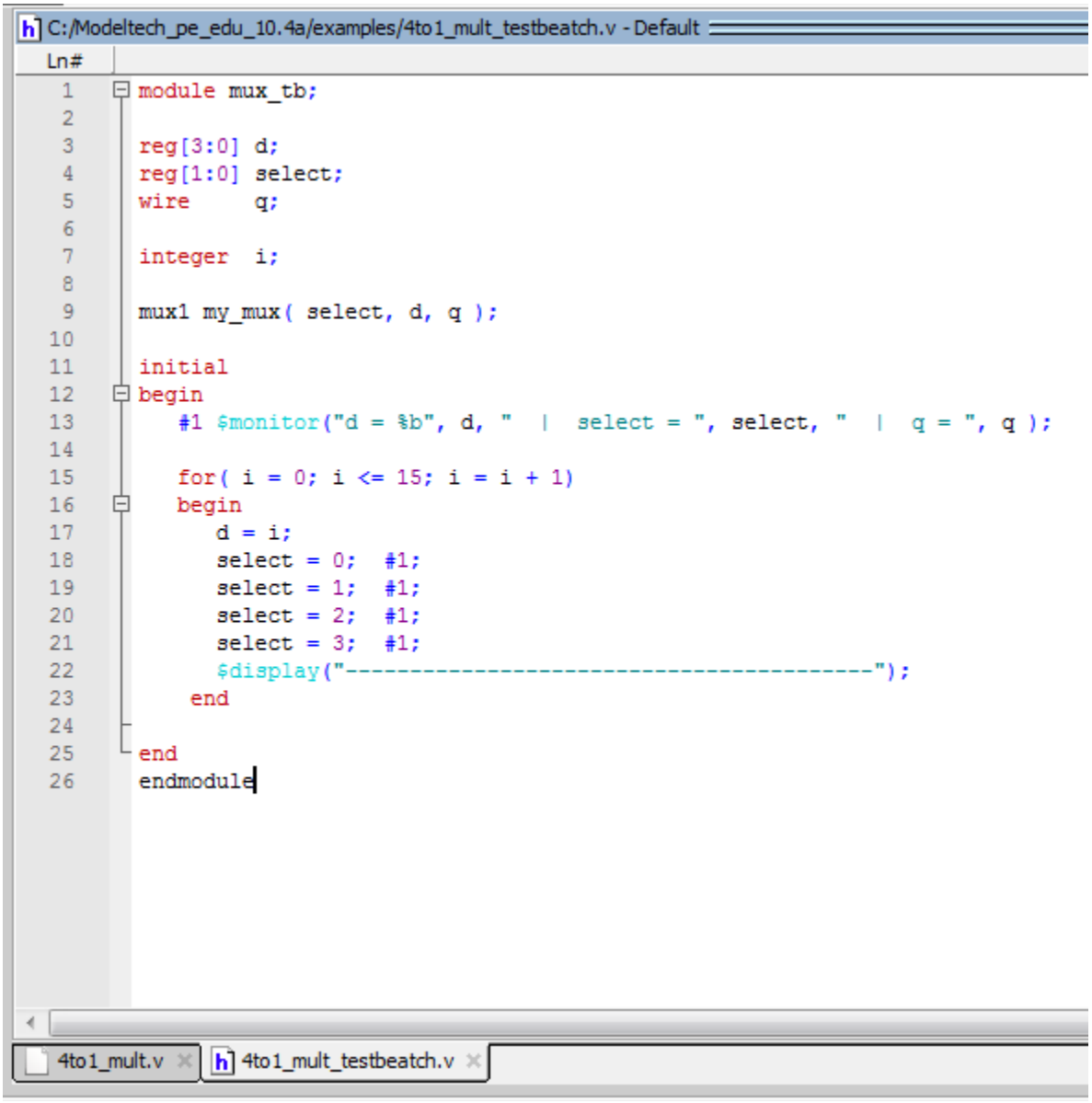
Answer 4

C:/Modeltech_pe_edu_10.4a/examples/4to1_mult.v - Default

```
Ln#
 1  module mux1( select, d, q );
 2
 3  input[1:0] select;
 4  input[3:0] d;
 5  output     q;
 6
 7  wire       q;
 8  wire[1:0] select;
 9  wire[3:0] d;
10
11  assign q = d[select];
12
13  endmodule
14
```

4to1_mult.v | 4to1_mult_testbeatch.v

Test batch


C:/Modeltech_pe_edu_10.4a/examples/4to1_mult_testbeatch.v - Default
Ln#
1 module mux_tb;
2
3 reg[3:0] d;
4 reg[1:0] select;
5 wire q;
6
7 integer i;
8
9 mux1 my_mux(select, d, q);
10
11 initial
12 begin
13 #1 $monitor("d = %b", d, " | select = ", select, " | q = ", q);
14
15 for(i = 0; i <= 15; i = i + 1)
16 begin
17 d = i;
18 select = 0; #1;
19 select = 1; #1;
20 select = 2; #1;
21 select = 3; #1;
22 $display("----------");
23 end
24
25 end
26 endmodule
4to1_mult.v
4to1_mult_testbeatch.v

Answer 5

module mux(a,b,c,d,e,sel,out);
input a,b,c,d,e;
input[2:0] sel;
output out;
reg out

always @(in0 or in1 or in2 or in3 or in4 or in5 or sel)

case (sel)

3’b000 : out = in0;

3’b001 : out = in1;

3’b010 : out = in2;

3’b011 : out = in3;

3’b100 : out = in4;

3’b101 : out = in5;

default : out = 64’bz;

endcase