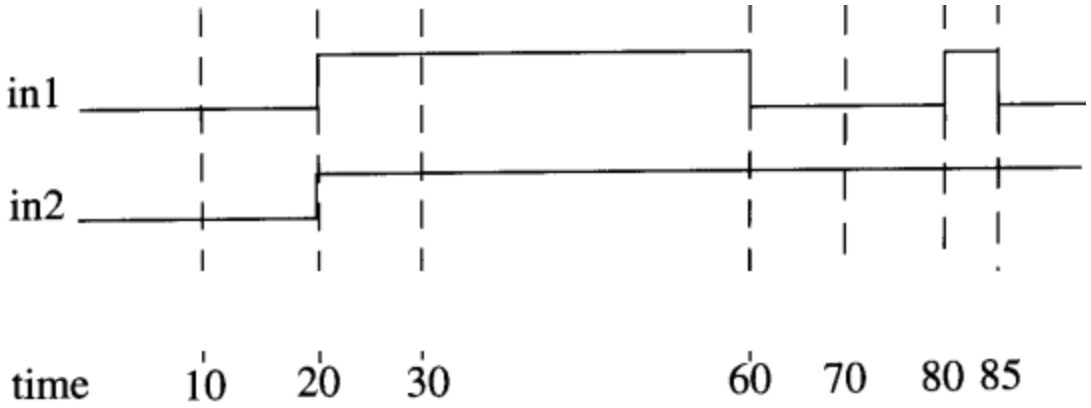
Assignment-3

1. Draw output waveform for “out” if the statement is assign #10 out = (in1 | in2)



2. Implement a full adder verilog module using both assignment statement and always block(2 separate verilog module but both implement full adder).