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15035

Answer 1

counter_4bit.v | tbcounter_4bit.v | run-vlog.do

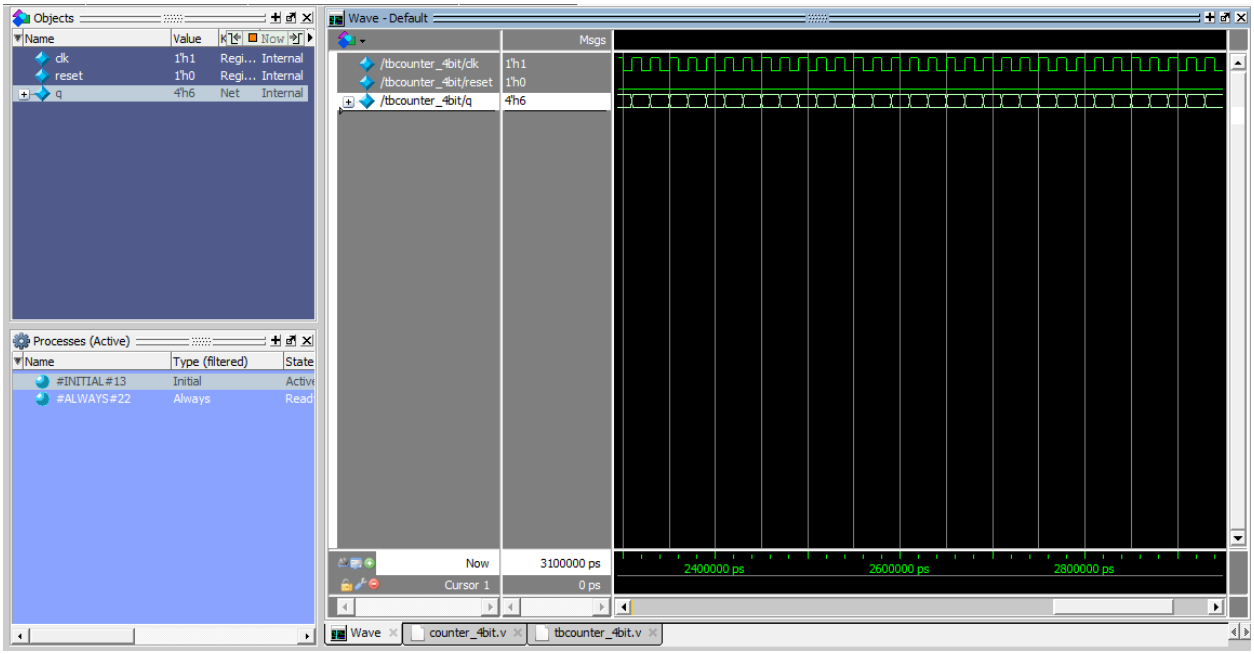
```
1  `timescale 1ns/1ps
2
3  module counter_4bit(clk,reset,q);
4
5  input clk,reset;
6  output [3:0] q;
7
8  reg [3:0] q;
9  wire clk,reset;
10
11
12 always @(posedge clk)
13  begin
14 if (reset)
15    q[3:0]<=4'b0000;
16
17    else
18     q[3:0]<=q+1;
19
20     end
21     endmodule
22
23
```

counter_4bit.v | tbcounter_4bit.v | run-vlog.do

```
1
2   module tbcounter_4bit;
3
4   reg clk,reset;
5   wire [3:0] q;
6
7   counter_4bit dut1(
8                .clk(clk),
9                .reset(reset),
10               .q(q)
11               );
12
13  initial
14    begin
15    $monitor ($time,,"reset=%b,clk=%b,q=%b",reset,clk,q);
16
17    clk=0;
18    reset=1;
19    #100 reset=0;
20    #3000 $stop;
21    end
22    always
23    begin
24    #10 clk =~clk;
25    end
26    endmodule
```

counter_4bit.v | tbcounter_4bit.v | run-vlog.do

```
1  vlib work
2  vlog counter_4bit.v tbcounter_4bit.v
3  vsim -novopt tbcounter_4bit
4  log -r /*
5  do wave.do
6  run -all
```


Objects
Name
Value
clk
1'h1
reset
1'h0
q
4'h6
Processes (Active)
Name
Type (filtered)
#INITIAL#13
Initial
#ALWAYS#22
Always
Wave - Default
Msgs
/tbcounter_4bit/clk
/tbcounter_4bit/reset
/tbcounter_4bit/q
Now
3100000 ps
Cursor 1
0 ps
2400000 ps
2600000 ps
2800000 ps
Wave
counter_4bit.v
tbcounter_4bit.v