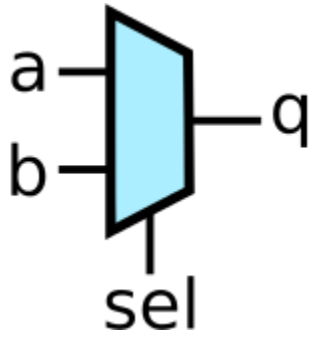
EE461fall semester assignment No-2

1. **Implement a 2:1 Multiplexer circuit using**
   a. **Gate level Verilog HDL Modeling.**



   b. **Verilog HDL Conditional expression.**

2. **Determine the Q and output states of this D-type gated latch, given the following input waveform:**