~~hiral~~ chirag kumar & Solanki 15035

(1)

reg x

wire z

(2) module mydesign(a,b,c,y);

input a,b,c;
output y;
reg y;

assign y = (a^b)|c; // This is wrong case because assign only can be wire not with reg.

end module.

(3) answer

a displays (a):

(5) So b is is 1. b is X.

(4) module FLIP FLOP (a,b, r, q);
input a,b, clk rst;
output q;

assign r = a&b
always @ (posedge clk or posneg rst)
if (rst)
q <= 0;
else
q <= r;

end modul