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Assignment of 13 week

Answer 1

C:/Modeltech_pe_edu_10.4a/examples/moorestate.v - Default

```
Ln#
 1
 2  module moore_mac
 3  (
 4          input   clk, data_in, reset,
 5          output reg [1:0] data_out
 6  );
 7          reg             [1:0]state;
 8
 9
10          parameter S0 = 0, S1 = 1, S2 = 2, S3 = 3;
11
12
13          always @ (state) begin
14                  case (state)
15                          S0:
16                                  data_out = 2'b01;
17                          S1:
18                                  data_out = 2'b10;
19                          S2:
20                                  data_out = 2'b11;
21                          S3:
22                                  data_out = 2'b00;
23                          default:
24                                  data_out = 2'b00;
25                  endcase
26          end
27
28
```

```
28
29          always @ (posedge clk or posedge reset) begin
30                  if (reset)
31                          state <= S0;
32                  else
33                          case (state)
34                                  S0:
35                                          state <= S1;
36                                  S1:
37                                          if (data_in)
38                                                  state <= S2;
39                                          else
40                                                  state <= S1;
41                                  S2:
42                                          if (data_in)
43                                                  state <= S3;
44                                          else
45                                                  state <= S1;
46                                  S3:
47                                          if (data_in)
48                                                  state <= S2;
49                                          else
50                                                  state <= S3;
51                          endcase
52          end
53
54  endmodule
55
```

Test batch :

C:/Modeltech_pe_edu_10.4a/examples/mooreTB.v - Default *

```
Ln#
 1  module mooreTB;
 2
 3  reg clk,rst,wr_en;
 4
 5  reg [2:0] Din;
 6  reg [2:0] ADDR;
 7  wire[2:0] DOUT;
 8
 9  sp_raw sp1 ( .clk (CLK),
10               .rst (RESET),
11               .wr_en (WR_EN),
12               .Din (DIN),
13                .Addr (ADDR),
14                .dout (DOUT),
15  );
16  initial
17      begin
18         CLK=0 , ADDR =0;
19         RESET = 1, DIN =8'h00;
20         WR _EN = 0;
21        #100 RESET =0;
22        #10  WR_EN = 1;
23         #160 WR_EN = 0;
24         #200 $stop;
25
26     always @(negede clk )
27
28         if ( WR_EN ) begin
29         ADDR = ADR +1;
30         DIN  = $random;
31         end
32  else
33        ADDR = $random;
34  endmodule
```

moorestate.v | mooreTB.v *

Code :

Function :

```
module moore_mac
(
	input	clk, data_in, reset,
	output reg [1:0] data_out
);
	reg	[1:0]state;


	parameter S0 = 0, S1 = 1, S2 = 2, S3 = 3;


	always @ (state) begin
		case (state)
			S0:
				data_out = 2'b01;
			S1:
				data_out = 2'b10;
			S2:
				data_out = 2'b11;
```

```
            S3:
                data_out = 2'b00;
            default:
                data_out = 2'b00;
        endcase
end


always @ (posedge clk or posedge reset) begin
        if (reset)
            state <= S0;
        else
            case (state)
                S0:
                    state <= S1;
                S1:
                    if (data_in)
                        state <= S2;
                    else
```

```
                    state <= S1;
            S2:
                if (data_in)
                    state <= S3;
                else
                    state <= S1;
            S3:
                if (data_in)
                    state <= S2;
                else
                    state <= S3;
        endcase
    end

endmodule
```

Test batch:

```
module mooreTB;

reg clk,rst,wr_en;
```

```
reg [2:0} Din;
reg [2:0} ADDR;
wire[2:0} DOUT;

sp_raw sp1 ( .clk (CLK),
             .rst (RESET),
             .wr_en (WR_EN),
             .Din (DIN),
              .Addr (ADDR),
              .dout (DOUT),
);
initial
   begin
      CLK=0 , ADDR =0;
      RESET = 1, DIN =8'h00;
      WR _EN = 0;
     #100 RESET =0;
     #10  WR_EN = 1;
```

```
        #160 WR_EN = 0;
        #200 $stop;

    always @(negede clk )

        if ( WR_EN ) begin
        ADDR = ADR +1;
        DIN  = $random;
        end
else
       ADDR = $random;
endmodule
```

Answer 2

C:/Modeltech_pe_edu_10.4a/examples/mealy.v - Default

```
Ln#
 1  module mealyfsm(rst,clk,din,y);
 2
 3  parameter s0=2'b00;
 4  parameter s1=2'b01;
 5  parameter s2=2'b11;
 6
 7  input rst ,clk,din;
 8  output y;
 9  reg y;
10
11  reg[1:0] ps;
12  reg[1:0] ns;
13
14  always @ (posedge clk )
15   if (rst)
16     ps <= s0;
17   else
18     ps <= ns;
19
20  always @ (ps or din )
21   y = 0;
22   ns= s0;
23   s0:if (din ==0 )
24       else
25          ns =s0;
26   s1:if(din ==0)
27      else
28         ns =s1;
29   s2:if(din ==0)
30      else begin
31         ns =s2;
32         y = 1;
33         end
34  default
35  endcase
```

Code :

module mealyfsm(rst,clk,din,y);

parameter s0=2'b00;

parameter s1=2'b01;

parameter s2=2'b11;

```
input rst ,clk,din;
output y;
reg y;

reg[1:0] ps;
reg[1:0] ns;

always @ (posedge clk )
 if (rst)
   ps <= s0;
 else
   ps <= ns;

always @ (ps or din )
 y = 0;
 ns= s0;
 s0:if (din ==0 )
     else
```

```
        ns =s0;
 s1:if(din ==0)
    else
        ns =s1;
 s2:if(din ==0)
    else begin
        ns =s2;
        y = 1;
        end
default
endcase
endmodule
```