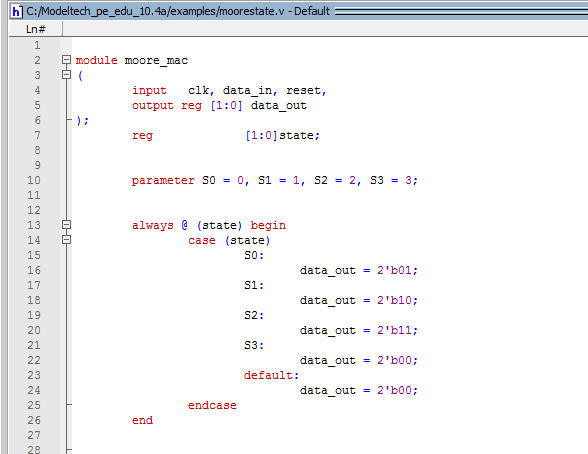
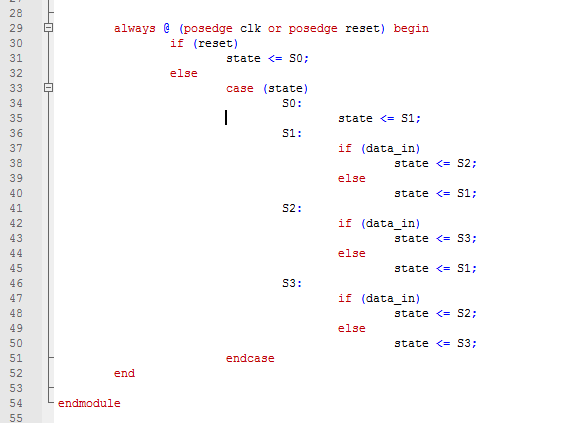
Chirag solanki

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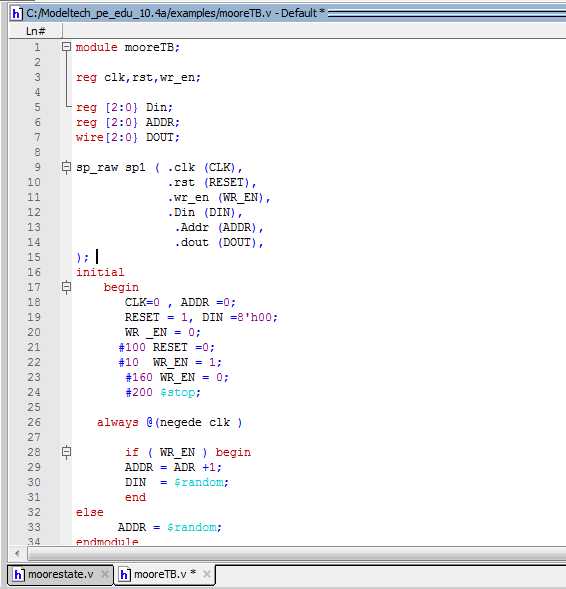
Assignment of 13 week

Answer 1





Test batch :



Code :

Function :

module moore\_mac

(

input clk, data\_in, reset,

output reg [1:0] data\_out

);

reg [1:0]state;

parameter S0 = 0, S1 = 1, S2 = 2, S3 = 3;

always @ (state) begin

case (state)

S0:

data\_out = 2'b01;

S1:

data\_out = 2'b10;

S2:

data\_out = 2'b11;

S3:

data\_out = 2'b00;

default:

data\_out = 2'b00;

endcase

end

always @ (posedge clk or posedge reset) begin

if (reset)

state <= S0;

else

case (state)

S0:

state <= S1;

S1:

if (data\_in)

state <= S2;

else

state <= S1;

S2:

if (data\_in)

state <= S3;

else

state <= S1;

S3:

if (data\_in)

state <= S2;

else

state <= S3;

endcase

end

endmodule

Test batch:

module mooreTB;

reg clk,rst,wr\_en;

reg [2:0} Din;

reg [2:0} ADDR;

wire[2:0} DOUT;

sp\_raw sp1 ( .clk (CLK),

.rst (RESET),

.wr\_en (WR\_EN),

.Din (DIN),

.Addr (ADDR),

.dout (DOUT),

);

initial

begin

CLK=0 , ADDR =0;

RESET = 1, DIN =8'h00;

WR \_EN = 0;

#100 RESET =0;

#10 WR\_EN = 1;

#160 WR\_EN = 0;

#200 $stop;

always @(negede clk )

if ( WR\_EN ) begin

ADDR = ADR +1;

DIN = $random;

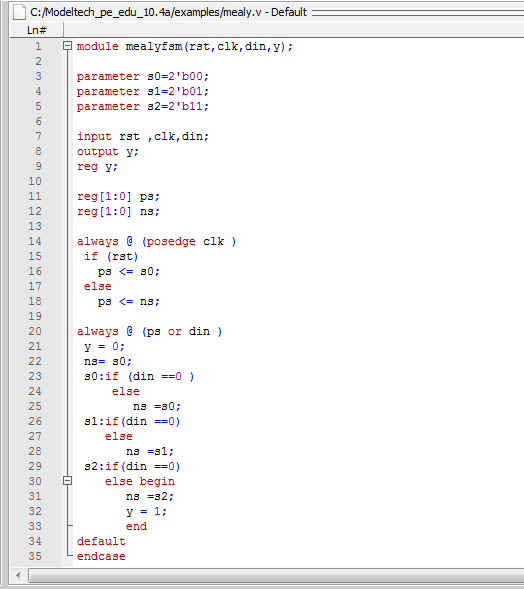
end

else

ADDR = $random;

endmodule

Answer 2



Code :

module mealyfsm(rst,clk,din,y);

parameter s0=2'b00;

parameter s1=2'b01;

parameter s2=2'b11;

input rst ,clk,din;

output y;

reg y;

reg[1:0] ps;

reg[1:0] ns;

always @ (posedge clk )

if (rst)

ps <= s0;

else

ps <= ns;

always @ (ps or din )

y = 0;

ns= s0;

s0:if (din ==0 )

else

ns =s0;

s1:if(din ==0)

else

ns =s1;

s2:if(din ==0)

else begin

ns =s2;

y = 1;

end

default

endcase

endmodule