Computer-Aided VLSI System Design (EEE5022)

Department of EE & GIEE, NTU

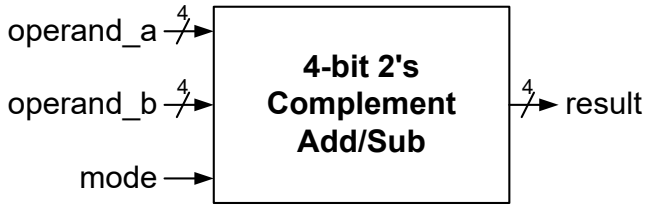
Lecturer: Prof. Chia-Hsiang Yang

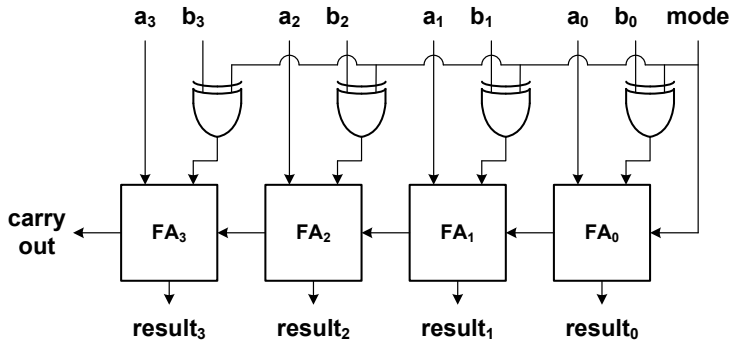
2025.9.2

VLSI Design and Implementation

Digital IC Design Flow

1. Concept/Application
2. Function/Spec. definition
3. Algorithm exploration
4. Architecture design
   - Divide-and-conquer
   - Sub-module design
   - Design verification
5. System prototyping
   - RTL design
   - Cell-based IC design flow

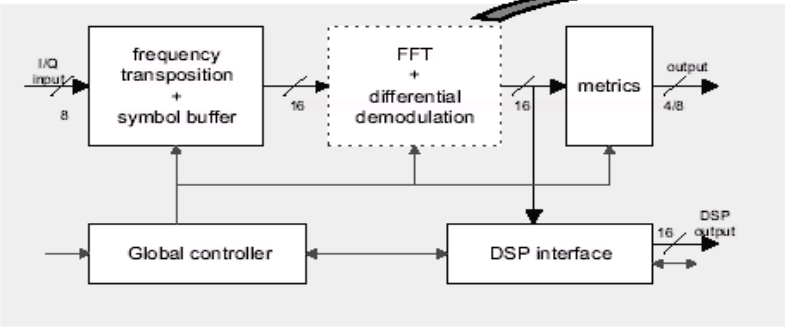





```
module  Add_Sub_Unit( result, operand_a, operand_b, mode, detect );

  input   [3:0] operand_a, operand_b;
  input         mode;
  output  [3:0] result;
  output        detect; // for question 3

  wire    [3:0] xor_b;

  xor g0 ( xor_b[0], operand_b[0], mode );
```

Algorithm Mapping

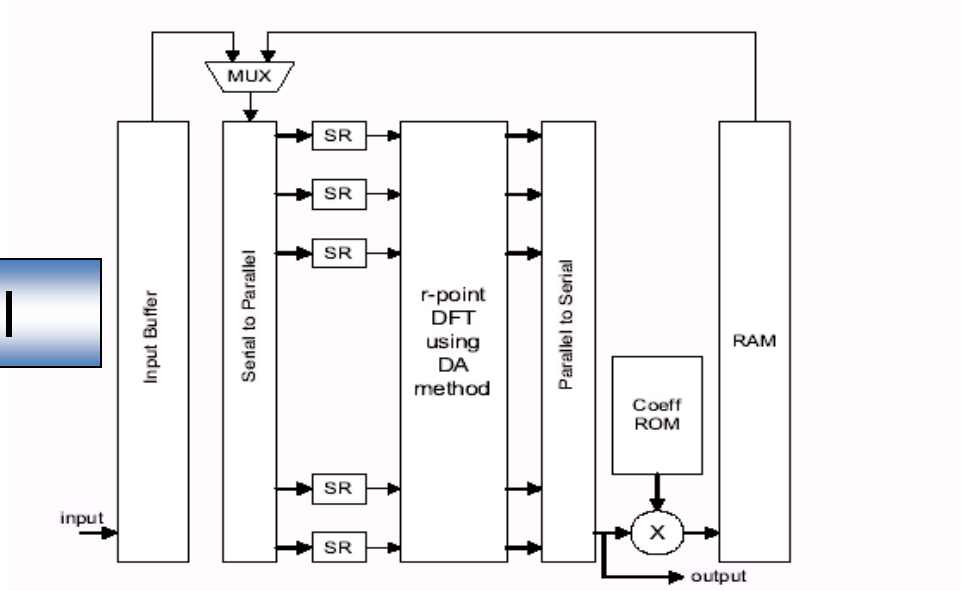
System/Algorithm Level



$$X(k) = \sum_{n=0}^{N-1} x(n) W_N^{nk} \qquad k = 0,1,\ldots,N-1$$

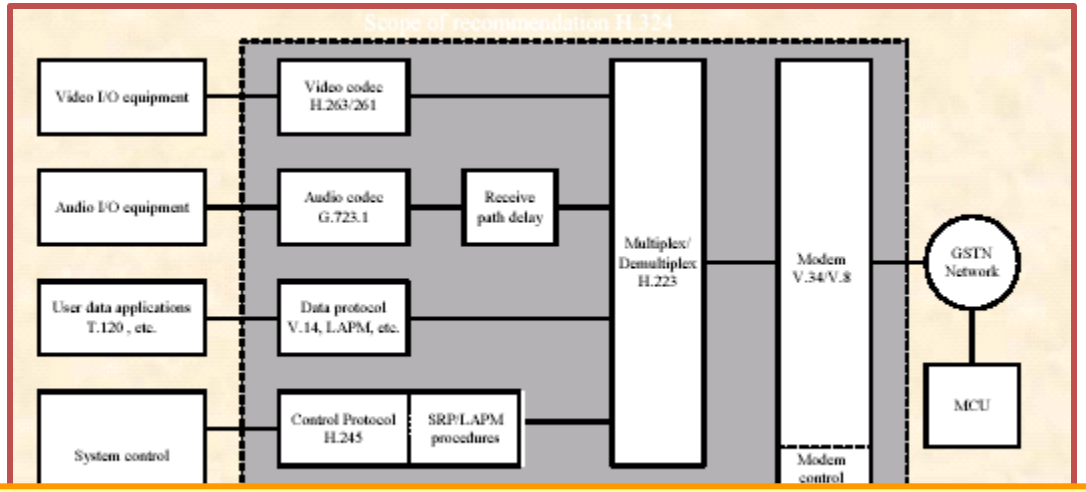
$$X(k) = \sum_{n=0}^{N/2-1} x(2n) W_{N/2}^{nk} + W_N^k \sum_{n=0}^{N/2-1} x(2n+1) W_{N/2}^{nk}$$

RTL Level



System Specifications

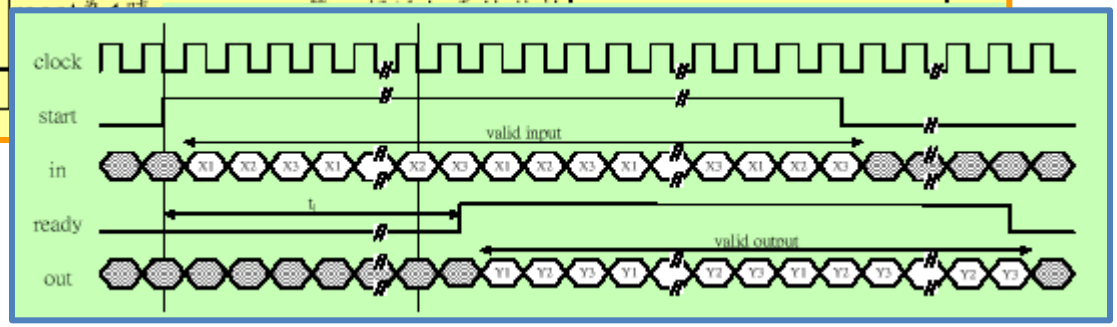
Partition



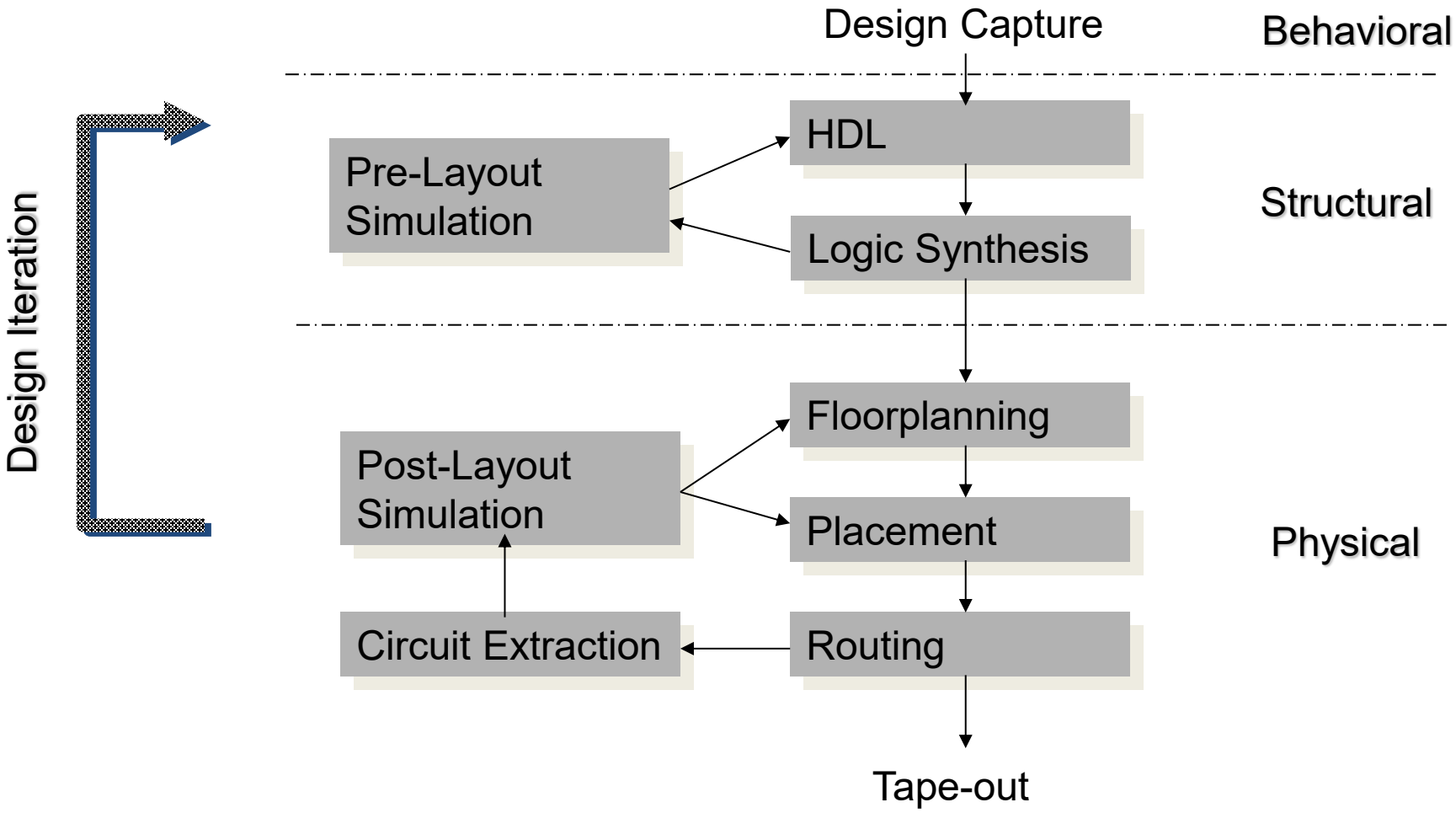
IO Spec.

腳位名稱		描述	Drive Strength/Output Load
clk	輸入	系統時脈	assume infinite
reset	輸入	系統重置訊號，high active	1 ns/pf
din	輸入	每個clock cycle輸入一個16-bit 正整數	1 ns/pf
ready	輸出		
dout	輸出		

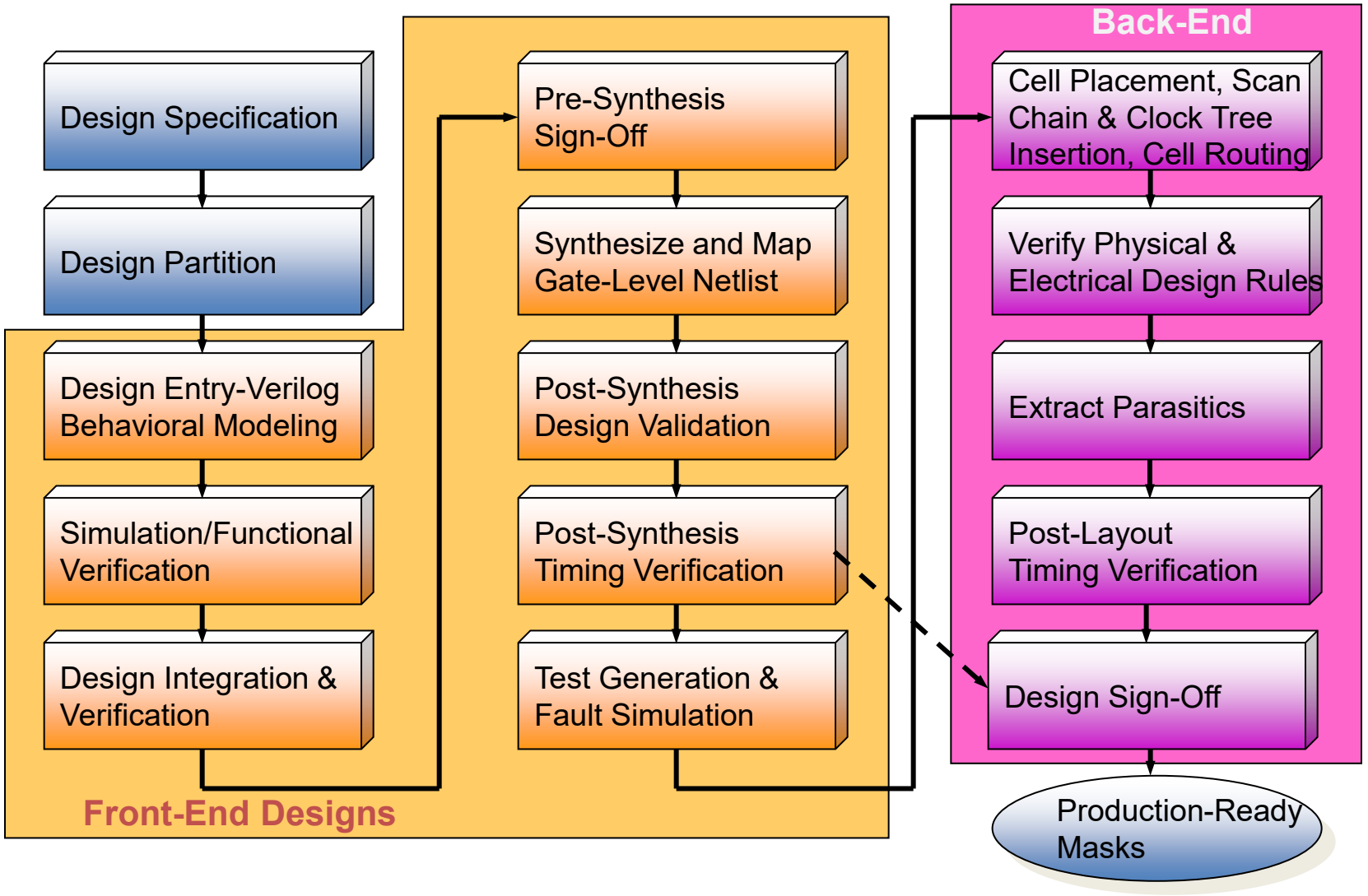
IO Timing Spec.



Cell-based Design Flow



Digital IC Design Flow



Overview of CVSD

- Objective
  - Students will learn how to design VLSI circuits and systems following a **standard VLSI system design flow**, where various **electronic design automation (EDA) tools** will be used extensively in the semester

- Course content
  1. Verilog-HDL
  2. Synthesis
  3. Static Timing Analysis
  4. Placement and Routing
  5. Verification
  6. High-level synthesis
  7. Design Rule Check, Layout versus Schematic, Layout Parasitic Extraction

Course Schedule (1)

Week	Date	Lecture	Speaker	Place	Lab	HW assign	HW due
01	09/02	Introduction	楊家驤教授	**MD205**	Lab0		
02	09/09	Verilog-HDL (1)	徐以帆	Online			
03	09/16	Verilog-HDL (2)	徐以帆	Online	Lab1	HW1	
04	09/23	Verilog-HDL (3)	孫振庭	Online			
05	09/30	Verilog-HDL (4)	孫振庭	Online	Lab2	HW2	HW1
06	10/07	Synthesis (1)	王傑立	Online	Lab3		
07	10/14	Synthesis (2)	王傑立	Online		HW3	HW2
08	10/21	Static Timing Analysis	Minh Khoa Tran	Online	Lab4		
09	10/28	**Midterm**		**MD205**			
10	11/04	**Midterm Review/ Project Announcement**	TA	**MD205**		HW4	HW3

Course Schedule (2)

Week	Date	Lecture	Speaker	Place	Lab	HW assign	HW due
11	11/11	APR (1)	蔡岳峰	Online	Lab5		
12	11/18	APR (2)	蔡岳峰	Online	Lab6	HW5	HW4
13	11/25	APR (3)	蔡岳峰	Online	Lab7		
14	12/02	Formal Verification	Cadence	Online	Lab8		HW5
15	12/09	High-Level Synthesis	Cadence	Online	Lab9		
16	12/16	PVS/DRC/LVS	Cadence	Online	Lab10		
17	12/23	**Project Presentation**	-	Online			

Acknowledgment:

- Formal verification, HLS, PVS: 益華科技 cadence®

TSRI NARLabs 國家實驗研究院 台灣半導體研究中心 Taiwan Semiconductor Research Institute

Online Course Link

- Google Meet:
  https://meet.google.com/pqf-czma-vhr
- Please log in using “[StudentID]-[Name]” for TA to verify your identity.
- Your microphone is set to be muted by default. If you have any questions, please use the chatroom to ask.

TA Contact

Lead TA & Final Project	陳柏任	d13943013@ntu.edu.tw
TA	張均豪	r12k41024@ntu.edu.tw
Lecture: Verilog-1	徐以帆	r13943005@ntu.edu.tw
Lecture: Verilog-2	孫振庭	f12k41031@ntu.edu.tw
Lecture: Synthesis	王傑立	d13943012@ntu.edu.tw
Lecture: STA	Minh Khoa Tran	r12k41036@ntu.edu.tw
Lecture: APR	蔡岳峰	f12943014@ntu.edu.tw
Lab	黃佳穎	r13943003@ntu.edu.tw
HW1	曾柏豪	r13943123@ntu.edu.tw
HW2	顏子茗	r13943119@ntu.edu.tw
HW3	吳璨霖	r13943017@ntu.edu.tw
HW4	江承恩	r13943008@ntu.edu.tw
HW5	楊耀凱	r12943121@ntu.edu.tw

Course Information

- Course materials
  - Lecture notes
  - Technical documents
- Course website
  - https://cool.ntu.edu.tw/courses/50618

Grading Policy

- Participation (Lab): 5%
- Homework: 30%
  - Submission to NTU COOL
  - Deadline: Tuesday afternoon (13:59 pm)
- Midterm Exam: 30%
  - Closed-book written exam
- Final Project: 35%
  - A team of 2 students
  - VLSI design (from RTL to GDS)
- No late submissions (unless for special cases)

Enrollment Announcement

Course Registration Priority:

1. **GIEE ICS/EDA and GSAT ICDA Students:** You can directly get an authorization code for enrollment.
2. **Research Requirement:** If this course is required for your research and your advisor asks you to take this course, please email me and copy your advisor
3. **Other Students with Verilog Experience:** If there are any remaining seats, please sign up first and the authorization codes will be allocated through lottery

❖**Auditing:** The course is open for auditing (with limited quota). To be added to the audit list, please sign up or email the lead TA

TSRI Membership Application (for Enrolled Students)

- https://www.tsri.org.tw/main.jsp

Deadline: 9/9 23:59

Important Notice:

需於會員資料中填寫指導教授並確認通過

You must fill in your research/teaching advisor's information in the membership profile and ensure approval.

EE2-231 Server Account (for Enrolled Students)

- https://reurl.cc/Ny1kk9

Deadline: 9/9 23:59

IC設計實驗室伺服器帳號申請表

實驗室規則：

1. 請勿任意 reboot 主機，破壞系統或做出對系統有害之行為，或將帳號借予他人使用，否則
若經查獲，立即刪除帳號，並交由教授處理。
2. 硬碟使用空間以大學部 1G、碩士班 5G、博士班 10G 為限。
3. 個人資料請隨時自行備份，並於隔年9/1前將個人目錄下的檔案清理乾淨，不保證檔案完整性。
4. 帳號預設期限為一學年，每年9/1將停止上學年申請之帳號，新的學年度請重新申請。
5. 其它注意事項請參閱本實驗室內的實驗室公布欄與實驗室網頁 http://cad.ee.ntu.edu.tw。
6. 本伺服器帳號需使用"校內IP"登入, 如果是校外IP, 請參考 https://ccnet.ntu.edu.tw/vpn。